Module 1: Introduction and Background
Lecture 1.3: Taxonomy of ICs

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Outline

• **Background**
  – Taxonomy of ICs
  – Levels of design abstraction

• **Key topics in SoC design**
  – HW/SW Partitioning
  – Behavioral synthesis
  – On-chip communication architecture
  – SoC modeling and co-simulation
Taxonomy of Integrated Circuits

- By scope of use

**ICs**

- **Application Specific IC (ASIC)**
  - Designed for one end system
  - E.g., Chips used in Digital Cameras, Printers

- **Application Specific Standard Product (ASSP)**
  - Re-used across multiple end-systems, but optimized for a single application
  - E.g., Mobile baseband processors

- **Domain Specific**
  - Designed for an application domain
  - E.g., DSPs, Network processors, GPUs

- **General Purpose**
  - Usable across a wide range of end-systems and applications
  - E.g., Microprocessors, Memory, FPGAs

Increasing volume
Increasing generality
Taxonomy of Integrated Circuits

- By degree of design customization

ICs
- Full-custom
- Semi-custom
  - Cell-based
    - Standard Cell
  - Array-based
    - Macro Cell
    - Mask programmable
    - Field programmable

Increasing design cost
More scope for optimization
Full-Custom Design

- Complete design-specific customization down to layout
- High design effort, maximum efficiency

Intel 4004
Cell Based Design

- A cell library is constructed, with each cell (gate/latch/flip-flop) carefully designed and characterized.
- Ensures that all the gates will work when connected in the prescribed way.
- Ensures that the timing models are clean and well understood by the designer/EDA tools.
- Standard cells must have the same height
  - Macro cells do not have this restriction.
Gate Array / Sea-of-gates

- An uncommitted cell or gate is formed by two or more N-channel and P-channel transistors.
- The digital logic function is realized by connecting these gates using metal or poly interconnect.
- Routing may be performed through dedicated channels or over the gates (additional metal layers).
Field Programmable Gate Arrays (FPGAs)

- FPGAs consist of Configurable Logic Blocks (CLBs) and Programmable Interconnect
Configurable Logic Block

- Lookup table (LUT), arithmetic circuit, flip-flop(s), and multiplexers
- LUT stores truth table of logic function to be implemented

Stratix V Adaptive Logic Module (Source: Altera)
FGPA: Contemporary Architecture

- Modern FPGAs contain hardwired circuits for arithmetic, memory, I/O, and even microprocessors

Stratix V FPGA architecture (Source: Altera)