Module 1: Introduction and Background
Lecture 1.4: Levels of Design Abstraction

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Levels of Abstraction in IC Design
Design Gap

Potential Design Complexity and Designer Productivity

- Logic Tr./Chip
- Tr./S.M.

68%/Yr
Complexity growth rate

21%/Yr
Productivity growth rate

<table>
<thead>
<tr>
<th>Year</th>
<th>Technology</th>
<th>Chip Complexity</th>
<th>Frequency</th>
<th>Staff</th>
<th>Staff Cost*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1997</td>
<td>250 nm</td>
<td>13 M Tr.</td>
<td>400 MHz</td>
<td>210</td>
<td>90 M</td>
</tr>
<tr>
<td>1998</td>
<td>250 nm</td>
<td>20 M Tr.</td>
<td>500</td>
<td>270</td>
<td>120 M</td>
</tr>
<tr>
<td>1999</td>
<td>180 nm</td>
<td>32 M Tr.</td>
<td>600</td>
<td>360</td>
<td>160 M</td>
</tr>
<tr>
<td>2002</td>
<td>130 nm</td>
<td>130 M Tr.</td>
<td>800</td>
<td>800</td>
<td>360 M</td>
</tr>
</tbody>
</table>

* @ $ 150 k / Staff Yr. (In 1997 Dollars)

Source: SEMATECH
Levels of Abstraction in IC Design

• How do you attack the challenging problem of IC design?

• Divide-and-conquer: Break the problem down and address it in steps
  – Trade-off optimality for feasibility
Evolution of IC Design Abstraction

- **Source**: Frank Schirrmieister, Synopsys
  - [http://blogs.synopsys.com/viewfromtop/files/2008/05/abstractions.jpg](http://blogs.synopsys.com/viewfromtop/files/2008/05/abstractions.jpg)
Y-Chart Representation of IC Design

- Proposed by Gajski and Kuhn in 1983
- Three different domains or dimensions of modeling
  - Behavior, Structure, Geometry
- IC design can be viewed as an iterative “spiral” refinement along these three domains

Prof. Dan Gajski, UC Irvine
IC Design: Levels of Abstraction

- Abstraction: Hiding detail
IC Design: Levels of Abstraction

Architecture algorithm of barcode is

```
ARCHITECTURE algorithm OF barcode IS

LOOP
  IF video = vh THEN
    white := white + 1;
    IF flag = bh THEN
      flag := vh; black := 0; data <= white;
    ELSE
      black := black + 1;
    END IF;
  END LOOP;
  addr <= actnum;
  EXIT WHEN (white = limit) OR (black = limit); END LOOP;
```

Behavioral description (VHDL)

```
ARCHITECTURE scheduled OF barcode IS

BEGIN
  CASE state IS
    WHEN s3 =>
      IF (video = vh) THEN
        white := white + 1;
        IF (flag = bh) THEN
          flag := vh; black := 0; data <= white;
        ELSE
          black := black + 1;
        END IF;
        state <= s4;
      END IF;
    ELSE
      black := black + 1;
      state <= s5;
    END CASE;
  END CASE;
END scheduled;
```

Structural RTL

Functional RTL

Gate-level netlist
Why design at the higher levels?

- Greater designer productivity
- Much greater impact on the quality of the design (performance/power)
- Quick / early design iterations

![Diagram showing performance/power improvement and simulation/analysis iteration times across different design levels.](image)

- System level: 10-20X performance/power improvement, seconds - minutes simulation/analysis iteration times
- Behavior level: 2-5X performance/power improvement, minutes - hours simulation/analysis iteration times
- Register-transfer level: 20 - 50% performance improvement, hours - days simulation/analysis iteration times