ECE 695R: SYSTEM-ON-CHIP DESIGN

Module 2: HW/SW Partitioning
Lecture 2.9: HW/SW Co-Synthesis

Anand Raghunathan
raghunathan@purdue.edu

Fall 2014, ME 1052, T Th 12:00PM-1:15PM
Lecture 2.9

- **HW/SW co-synthesis**
  - Automatically performing various steps involved in design and use of HW accelerators
  - Move HW/SW partitioning from an art to a science

- **Key question:** Which computations to implement as HW accelerators?

Diagram:

1. Select Function(s) to Accelerate
2. Implement HW for Selected Function(s)
3. Interface to HW
4. Integrate with SW
5. Evaluate (performance, power, area)
HW/SW Co-synthesis

- What can be automated?
  - Selection of functions to accelerate
  - Generation of hardware and software
  - Generation of HW-SW interfaces
  - Estimation of performance, power, hardware size, memory, ...

Diagram:
- Program Specification
- Partitioning
- Hardware Synthesis
- Interface Synthesis
- Compilation
- Estimation (Performance, Power, ...)

Diagram flow:
- Program Specification → Partitioning
- Partitioning → Hardware Synthesis
  - Hardware Synthesis → HW/SW architecture
  - Hardware Synthesis → Interface Synthesis
  - Interface Synthesis → Estimation (Performance, Power, ...)
- Partitioning → Compilation
- Hardware Synthesis → Hardware
- Interface Synthesis → Software
- Compilation → Software
Before you automate...

• Require a clear definition of the inputs & outputs
  – Program specification and Architectural template
Input for Partitioning

• The algorithm / program to be partitioned can be specified in many ways
  – Sequential Program
    • Function Call Graph + Control-Flow Graph
  – Concurrent Program
    • Process Network (Communicating Sequential Processes, Kahn Process Networks, Petri Nets, ...)
    • Task Graph
Function Call Graph

Nodes: Functions
Edges: Function calls

EXAMPLE: MPEG2 Decoder
Task Graph

• Nodes: Tasks
  – Functions/sub-programs that execute once

• Edges: Control/data dependencies between nodes
Target Architectural Template

• A well-defined architectural template consists of a specific processor, interconnect structure, and communication semantics between SW and HW

• Enables accurate estimation of performance, power, area of alternative partitions