Module 2: HW/SW Partitioning
Lecture 2.14: Application Specific Instruction Processors (ASIPs)
• Application-specific Instruction Processors (ASIPs)
  – ASIPs as a building block for SoCs
  – ASIP design approaches
  – Extensible Processors: A practical approach to ASIP design
HW/SW Partitioning: Two Approaches

- Fundamental differences arise from
  - Whether the ISA changes
  - How the custom HW is integrated with the programmable HW

![Diagram showing HW/SW Partitioning]

- **ISA**
- **GPP**
- **HW Accel.**
- **Software**
- **Memory-mapped I/O + interrupts**
- **ASIP**
- **Custom HW**
- **Extensions to ISA**
Architectural Alternatives

• Important questions:
  – Is there a (Turing-complete) instruction set?
  – Is the instruction set tailored to an application or domain?

• Application-specific Hardware: No “instruction set”

• GPP: Instruction Set is not tailored towards a specific application or application domain

• DoSP: Instruction Set is tailored to a domain
  – Graphics, Digital Signal Processing, Network Processing

• ASIP: Instruction Set customized to a specific application
A functional view of an SoC: Control Plane and Data Plane Processing

Source: Grant Martin, Tensilica
## Control and Data Plane Processing Tasks

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<tr>
<th>Application</th>
<th>Control Plane Processing Tasks</th>
<th>Dataplane Processing Tasks</th>
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<td>Policy Application&lt;br&gt;Network Management&lt;br&gt;Signaling&lt;br&gt;Topology Management</td>
<td>Queuing&lt;br&gt;Scheduling&lt;br&gt;Routing&lt;br&gt;Classification&lt;br&gt;Encryption/Decryption</td>
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<td>Advanced Set-Top Box (ASTB)</td>
<td>Configuration Management&lt;br&gt;User Interface</td>
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<td>Audio Codecs&lt;br&gt;Video Codecs&lt;br&gt;Wireless PHY and Link Layers</td>
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</table>

Source: Grant Martin, Tensilica
SoC Based on HW Accelerators - TI OMAP 44XX
Moving the DPU from Custom HW to an ASIP

Custom HW based Design

ASIP-based Design

Q: What is the benefit of doing this?

Source: Grant Martin, Tensilica
ASIP as a building block for SoCs (Example 1: 6 ASIPs + 1 GPP)

- Epson Realoid Printer SoCs
- Heterogeneous, asymmetric, 7 core design with very little app. specific HW
- 90nm process technology, 288 MHz clock rate, >7M gate-count complexity, Less than 2.5W power

Epson PM-T990  Epson PM-A970  Epson PM-D870  Epson PM-A920  Epson Stylus Photo R380

Source: Grant Martin, Tensilica
What are all those ASIPs for?

Each processing block runs at whatever clock rate is needed for that block, which saves energy.

Source: Grant Martin, Tensilica
ASIP as a building block for MPSOCs
(The processor is the new gate!)

Cisco’s Silicon Packet Processor
192 Xtensa processor cores per chip – 0.5 sq-mm each, 18M gates, 0.13 micron
All data moved via intelligent DMA channels without a common bus (not SMP)

Cisco ASR 1000
Aggregation Services Router family

Cisco CRS-1 Terabit Router

Source: Grant Martin, Tensilica