Module 4: On-chip Communication Architecture
Lecture 4.1: Overview

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On-chip Communication Architecture: Outline

- On-chip communication architecture is a first-class citizen of the SoC
- Bus-based on-chip communication architecture basics
- Advanced bus-based on-chip communication
- Networks-on-chip

- Reference material for this module
  - “On-chip communication architectures: System-on-chip interconnect,” Pasricha and Dutt, Morgan Kaufmann
    - Available in Potter Engineering Library
    - Available online through Purdue library website
On-chip Communication Architecture: An Analogy
Interconnect Scaling Trends

- Global wires scale slower than transistors/gates
  - Why?

- In nano-scale technologies, interconnects greatly impact performance and power consumption of SoCs!
Interconnect Scaling Trends

- Interconnect delay and power impacted by cross-coupling

C.N. Taylor, Y. Zhao, S. Dey, “Modeling and minimization of interconnect energy dissipation in nanometer technologies”, DAC’01
# Interconnect Scaling Trends

<table>
<thead>
<tr>
<th>Operation</th>
<th>Delay (0.13um)</th>
<th>Delay (0.05um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32b ALU Operation</td>
<td>650ps</td>
<td>250ps</td>
</tr>
<tr>
<td>32b Register Read</td>
<td>325ps</td>
<td>125ps</td>
</tr>
<tr>
<td>Read 32b from 8KB RAM</td>
<td>780ps</td>
<td>300ps</td>
</tr>
<tr>
<td>Transfer 32b across chip (10mm)</td>
<td>1400ps</td>
<td>2300ps</td>
</tr>
<tr>
<td>Transfer 32b across chip (20mm)</td>
<td>2800ps</td>
<td>4600ps</td>
</tr>
</tbody>
</table>

2:1 global on-chip comm to operation delay
9:1 in 2010

Source: W. J. Dally, DAC 2009 keynote
System-level Trends

- Increasing scales of integration
  - Manifests as increasing number of SoC components
System-level Trends

- Heterogeneity among components that need to be interconnected
- Increasing volume and diversity of traffic
The Communication Architecture is more than a set of Wires!

• Complexity of logic can easily compare to a small microprocessor!
Impact of Communication Architecture on SoC Power

<table>
<thead>
<tr>
<th>System Component</th>
<th>Part Name</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Embedded Processor</td>
<td>ARM946E-S¹</td>
<td>60</td>
</tr>
<tr>
<td>Memory Controller</td>
<td>DW_ahb_memctl²</td>
<td>29.1</td>
</tr>
<tr>
<td>On-Chip Bus</td>
<td>DWamba²</td>
<td>22.6</td>
</tr>
<tr>
<td>Cache</td>
<td>ARM946E-S¹</td>
<td>36</td>
</tr>
<tr>
<td>Interrupt Controller</td>
<td>DW_ahb_ictl²</td>
<td>2.6</td>
</tr>
<tr>
<td>UART</td>
<td>DW_apb_uart²</td>
<td>4.1</td>
</tr>
</tbody>
</table>

Power breakdown for AMBA AHB (NEC 0.15um)

Power Analysis of System-Level On-Chip Communication Architectures
Impact of Communication Architecture on SoC Performance

• Example: TCP/IP Network Interface Card’s Checksum Subsystem

37% variation in cycles/packet

Protocols (Priorities, burst size…)

Lajolo, Raghunathan, Dey, Lavagno, Sangiovanni-Vincentelli, CODES’98
**Evolution of SoC Design Methodology**

**I**

**Computation-centric system design**
- Focus: optimizing computation (e.g., HW/SW partitioning)
- Standard communication architecture

**Communication-aware system design**
- Incorporate communication architecture into design process
- Evolutionary changes to comm. architecture

**Communication-centric system design**
- Extensive effort on optimizing communication

**II**

**Communication Arch. Design**