ECE 695R:
SYSTEM-ON-CHIP DESIGN

Module 4: On-chip Communication Architecture
Lecture 4.3: AMBA 2.0 – AHB & APB

Anand Raghunathan
raghunathan@purdue.edu

Fall 2014, ME 1052, T Th 12:00PM-1:15PM
On-chip Buses: AMBA

Additional information:
ARM’s AMBA on-chip Bus

- What is AMBA?
  - Advanced Microcontroller Bus Architecture specification
  - An on-chip communication standard for ARM’s processors and IP cores

Evolution of AMBA Standards

Source: ARM Ltd.
AMBA 2.0

**AMBA AHB**
- High performance
- Pipelined operation
- Multiple bus masters
- Burst transfers
- Split transactions

**AMBA ASB**
- High performance
- Pipelined operation
- Multiple bus masters

**AMBA APB**
- Low power
- Latched address and control
- Simple interface
- Suitable for many peripherals
AHB Architecture

- Centralized arbitration / decode

- 1 unidirectional address bus (HADDR)
- 2 unidirectional data buses (HWDATA, HRDATA)
  - Only 1 active at any time
AHB Basic Transfer

- Split ownership of Address and Data bus lines
AHB Basic Transfer

- Data transfer with slave wait states
AHB Pipelining

- Transaction pipelining increases bus bandwidth
AHB Arbitration

- Arbitration protocol is specified, but the arbitration policy / algorithm is NOT
Cost of Arbitration in AHB

Time for arbitration

Time for handshaking
AHB Burst Transfers

- Bursts cut down on arbitration and handshaking time, improving performance
### AHB Burst Types

**Fixed length bursts**

<table>
<thead>
<tr>
<th>HBURST[2:0]</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>SINGLE</td>
<td>Single transfer</td>
</tr>
<tr>
<td>001</td>
<td>INCR</td>
<td>Incrementing burst of unspecified length</td>
</tr>
<tr>
<td>010</td>
<td>WRAP4</td>
<td>4-beat wrapping burst</td>
</tr>
<tr>
<td>011</td>
<td>INCR4</td>
<td>4-beat incrementing burst</td>
</tr>
<tr>
<td>100</td>
<td>WRAP8</td>
<td>8-beat wrapping burst</td>
</tr>
<tr>
<td>101</td>
<td>INCR8</td>
<td>8-beat incrementing burst</td>
</tr>
<tr>
<td>110</td>
<td>WRAP16</td>
<td>16-beat wrapping burst</td>
</tr>
<tr>
<td>111</td>
<td>INCR16</td>
<td>16-beat incrementing burst</td>
</tr>
</tbody>
</table>

- Incremental bursts access sequential locations
  - e.g. 0x64, 0x68, 0x6C, 0x70 for INCR4, transferring 4 byte data
- Wrapping bursts “wrap around” address if starting address is not aligned to total no. of bytes in transfer
  - e.g. 0x64, 0x68, 0x6C, 0x60 for WRAP4, transferring 4 word data
AHB Control Signals

- Transfer direction
  - HWRITE – write transfer when high, read transfer when low

- Transfer size
  - HSIZE[2:0] indicates the size of the transfer

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8 bits</td>
<td>Byte</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>16 bits</td>
<td>Halfword</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>32 bits</td>
<td>Word</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>64 bits</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>128 bits</td>
<td>4-word line</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>256 bits</td>
<td>8-word line</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>512 bits</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1024 bits</td>
<td></td>
</tr>
</tbody>
</table>

The transfer size set by HSIZE must be less than or equal to the width of the data bus.
AHB Control Signals

- Protection control
  - HPROT[3:0], provide additional information about a bus access

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0</td>
<td>Opcode fetch</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>Data access</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>0</td>
<td>-</td>
<td>User access</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>Privileged access</td>
</tr>
<tr>
<td>-</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>Not bufferable</td>
</tr>
<tr>
<td>-</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>Bufferable</td>
</tr>
<tr>
<td>0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Not cacheable</td>
</tr>
<tr>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Cacheable</td>
</tr>
</tbody>
</table>
**AHB Bus Matrix Topology**

- In addition to single shared bus and hierarchical bus, AHB can be implemented as a bus matrix.

Q: Why does this help?
Q: How does this compare to Avalon?
AHB-APB Bridge

High performance

AHB signals

System bus slave interface

Read data

Reset

Clock

PREADTA

PRESETn

PCLK

PSEL1

PSEL2

\ldots

PSELn

PENABLE

PADDR

PWRITE

PWDATA

Selects

Strobe

Address and control

Write data

Low power (and low performance)
• No bursts, no pipelined transfers
AMBA 3.0 / 4.0

• Introduced AXI high performance protocol
  – Channel-based architecture
  – Enhanced burst mode
  – Out of order (OO) transaction completion

• Miscellaneous
  – Advanced cache support
    • Specify if transaction is cacheable/bufferable
    • Specify attributes such as write-back/write-through
  – Enhanced protection support
    • Secure/non-secure transaction specification
  – Exclusive access (for semaphore operations)
  – Register slice support for high frequency operation