Essentials of MOSFETs

Unit 1: Transistors and Circuits

Lecture 1.4: MOSFET Device Metrics

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On current scales with MOSFET width

Currents will be quoted in milliamps per micrometer of width (or microamps per micrometer).
1) On-current

Output characteristic:

\[ I_D \text{ vs. } V_{DS} \text{ at fixed } V_{GS} \]

\[ V_{GS} = V_{DD} > V_T \]

\[ I_{ON} = I_D \left( V_{GS} = V_{DS} = V_{DD} \right) \]
On current is an important device metric for digital electronics because it determines the maximum speed of the circuit.

\[ I_{ON} = I_D \left( V_{GS} = V_{DS} = V_{DD} \right) \]

\[ \tau_{cir} \propto \frac{C_{sw} V_{DD}}{I_{ON}} \]

circuit speed
2) Off-current

The off-current transfer characteristic is defined as:

\[ V_D = V_{DD} \]

\[ I_D = I_{ON} \quad (\text{mA/\mu m}) \]

\[ V_G = 0 \]

The diagram illustrates the off-current (I_D) vs. V_GS at fixed V_DS, showing the transition from sub-threshold to above threshold. The transfer characteristic is described as the relationship between I_D and V_GS at fixed V_DS.
Off-current

transfer characteristic on a semi-log plot:

\[ V_{DS} = V_{DD} \]

\[ I_{OFF} = I_D \left( V_{GS} = 0; V_{DS} = V_{DD} \right) \]
The off-current metric

\[ I_{OFF} = I_D \left( V_{GS} = 0; V_{DS} = V_{DD} \right) \]

Off-current is an important device metric for static power.

\[ P_{static} = N_G I_{OFF} V_{DD} \]
3) Subthreshold Swing

transer characteristics:

\[ \log_{10} I_D (A/\mu m) \]

\[ V_{DS} = V_{DD} \]

\[ I_{ON} \]

subthreshold swing:

\[ (mV/\text{decade}) \]
Higher SS increases off-current (exponentially)

\[ \log_{10} I_D \]

\[(A/\mu m)\]

\[ SS_2 > SS_1 \]

\[ V_{DS} = V_{DD} \]

\[ V_T \]

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SS, $V_{DD}$, and Power

$P_{\text{static}} = N_G I_{\text{OFF}} V_{\text{DD}}$

$P_{\text{dynamic}} = \alpha f C_{\text{sw}} V_{\text{DD}}^2$

- Static power is controlled by the off-current.

- The SS determines the off-current.

- To minimize dynamic power dissipation at a given frequency, we should use the lowest power supply voltage possible.

- The SS determines the minimum power supply.
Reducing $V_T$ increases off-current (exponentially)
The SS metric

\[ SS = \left( \frac{\partial \left( \log_{10} I_D \right)}{\partial V_{GS}} \right)^{-1} = \text{mV/decade} \]

The number of mV that the gate voltage must increase to increase the drain current by a factor of 10.

SS must be minimized to minimize off-current.

SS must be minimized to minimize \( V_{DD} \).

In a MOSFET, SS > 60 mV/decade at T = 300 K.
Effect of the drain voltage

**Question:** How does the drain voltage affect $I_D$?

**Answer:** In several different ways that are related to the same underlying physics.
In the linear region $I_D \sim V_{DS}$

This is an intrinsic effect present in ideal and real MOSFETs, but there are other non-ideal effects.

**Output characteristic:**

$I_D$ vs. $V_{DS}$ at fixed $V_{GS}$

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Effect of $V_{DS}$ in the saturation region

Ideal MOSFETs have an infinite output resistance.

Real MOSFETs have a finite output resistance.

\[ r_o = \left[ \left( \frac{dI_D}{dV_{DS}} \right)_{V_{GS}} \right]^{-1} (\Omega - \mu m) \]

output characteristic:

$I_D$ vs. $V_{DS}$ at fixed $V_{GS}$
Effect of $V_{DS}$ on transfer characteristic

$V_G : 0 \rightarrow V_{DD}$

$V_D = 0.05$

$V_D = V_{DD}$

$V_{TSAT} < V_{TLIN}$

$V_{DS} = V_{DD}$

$V_{DS} = 0.05 \text{ V}$

threshold voltage in saturation region

threshold voltage in linear region
Effect of $V_{DS}$ in subthreshold transfer characteristics:

$DIBL = \frac{\text{change in } V_G}{\text{change in } V_D}$ at the same $I_D$ (in the subthreshold region). Units are mV/V.
Drain voltage non-idealities

All of these non-ideal effects:

- threshold voltage dependence on $V_{DS}$
- non-infinite output resistance
- DIBL

Are due to the same physics. A single metric is used to assess the magnitude of all these effects.

**DIBL**: Drain Induced Barrier Lowering
4) The DIBL metric

\[ \text{DIBL} = \left. \frac{\partial V_{GS}}{\partial V_{DS}} \right|_{I_D} = \frac{\text{mV}}{\text{V}} \]

DIBL = change in \( V_G \) / change in \( V_D \) at the same \( I_D \) (in the subthreshold region). Units are mV/V.

The higher the DIBL, the more sensitive the threshold voltage is to the drain voltage (and the lower the output resistance).
Key Figures of Merit for digital applications

1) On current
2) Off-current
3) Subthreshold swing
4) DIBL
Example: 32 nm N-MOS technology

\[ I_{ON} \approx 1.55 \, \mu A/\mu m \]
\[ I_{OFF} \approx 10^{-7} \, A/\mu m \]
\[ SS \approx 105 \, mV/\text{decade} \]
\[ DIBL \approx 160 \, mV/V \]
N-channel vs. P-channel MOSFET

**n-MOSFET**

\[ V_S = 0 \quad V_G > V_T \quad V_D > 0 \]

n-Si

S

“channel”

D

p-type silicon

side view

**p-MOSFET**

\[ V_S = 0 \quad V_G < V_T \quad V_D < 0 \]

n-Si

p-Si

S

“channel”

D

n-type silicon

side view

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Example: 32 nm P-MOS technology
Analog device metrics

\[ A_v(\text{max}) = -g_m r_o \]

g_m and r_0 are important analog device metrics

(also \(f_T\), \(f_{\text{max}}\), linearity, noise, mismatch, etc.)
Analog device metrics

\[ r_o = \left[ \left( \frac{dI_D}{dV_{DS}} \right)_{V_{GS}=V_{DD}} \right]^{-1} \quad \Omega - \mu m \]

\[ V_{GS} = V_{DD} \]

\[ g_m = \frac{dI_G}{dV_{GS}} \bigg|_{V_{DS}=V_{DD}} \quad (\text{mS/}\mu m) \]

\[ V_{GS} = V_{DD} - \Delta V_G \]

\[ I_D (\text{mA/}\mu m) \]

\[ V_{DS} \]

\[ V_{DSAT} \]

\[ V_{DD} \]

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Self-gain for 65 nm technology

\[ g_m \approx \frac{0.2 \text{ mA/\mu m}}{0.2 \text{ V}} = 1 \text{ mS/\mu m} \]

\[ r_o \approx \frac{1.2 \text{ V}}{0.18 \text{ mA/\mu m}} \approx 7 \text{ k}\Omega \cdot \mu\text{m} \]

\[ |A_v (\text{max})| = g_m r_o \approx 7 \]
$g_m = 2.5 \text{ mS/\mu m}$ $r_0 \approx 2.2 \text{ k\Omega - \mu m}$ $|A_v(\text{max})| = g_m r_0 \approx 5.5$
Recap

Given the measured characteristics of a MOSFET, you should be able to determine:

1. on-current: $I_{ON}$
2. off-current: $I_{OFF}$
3. subthreshold swing, $SS$
4. drain induced barrier lowering: DIBL
5. output resistance: $r_o$
6. transconductance: $g_m$

threshold voltage: $V_T$(lin) and $V_T$(sat)
drain saturation voltage: $V_{DSAT}$

*Our goal in this course is to understand these device metrics and parameters.*
Summary

Key device metrics for digital applications are on-current, off-current, SS, and DIBL.

Key device metrics for analog applications are small signal transconductance, output resistance, and self-gain.

Given a set of IV characteristics, you should be able to extract these metrics.

Our focus is this course is to relate these device metrics to the underlying physics.
Device metrics help device engineers and circuit design engineers to relate, in a general way, device performance to circuit performance.

Actual circuit design requires more. The next lecture is a short introduction to compact circuit models.