Essentials of MOSFETs

Unit 3 Homework Problems

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1) In an MOS capacitor, **everything depends on the bandbending in the semiconductor**. If $\psi_S$ is the potential at the surface, and $\psi = 0$ is the potential in the bulk, then $-q\psi_S$ is the total bandbending in the semiconductor. A negative $\psi_S$ means the bands bend up, and a positive $\psi_S$ means the bands bend down. This question helps familiarize you with surface potential and bandbending. Assume a Si MOS capacitor at room temperature.

1a) Assume $N_A = 10^{17} \text{ cm}^{-3}$ and compute $E_i - E_F$ and the related potential, $\psi_B = (E_i - E_F)/q$, which plays an important role in MOS electrostatics.

1b) Assume $\psi_S = \psi_B$ and sketch the energy band diagram and the charge density, $\rho(x)$ vs. position in the semiconductor.

1c) Assume $\psi_S = -\psi_B$ and sketch the energy band diagram and the charge density, $\rho(x)$ vs. position in the semiconductor.

1d) Assume $\psi_S = 0$ and sketch the energy band diagram and the charge density, $\rho(x)$ vs. position in the semiconductor.

1e) Assume $\psi_S = 2\psi_B$ and sketch the energy band diagram and the charge density, $\rho(x)$ vs. position in the semiconductor.

2) Get a feel for the magnitudes of important quantities by answering the following questions for a room temperature MOS capacitor with $N_A = 10^{18} \text{ cm}^{-3}$ and an oxide thickness of 2 nm with $\kappa_{ox} = 3.9$.

2a) Compute $\psi_B = (E_i - E_F)/q$

2b) Compute the depletion layer thickness, $W_D$, when $\psi_S = 2\psi_B$.

2c) Compute the electric field at the surface, $E_S$, when $\psi_S = 2\psi_B$.

2d) Compute the threshold voltage, $V_T$, assuming no metal-semiconductor work function difference. (This is the gate voltage needed to make $\psi_S = 2\psi_B$ and create an inversion layer in the semiconductor.)
3) Answer the following questions about the energy band diagram sketched below. Assume that the zero for electrostatic potential is in the semiconductor bulk, at large $x$ and that there is no metal-semiconductor work function difference. Also assume that the relative dielectric constant of the oxide is $\kappa_{\text{ox}} = 3.9$.

3a) What is the surface potential, $\psi_s$?
3b) What gate voltage, $V_G$, is applied?
3c) What is the voltage across the oxide, $\Delta V_{\text{ox}}$?
3d) What is the doping density, $N_D$?
3e) What is the width of the depletion region, $W_D$?
3f) What is the thickness of the oxide?

4) A high-frequency MOS capacitance vs. voltage characteristic is sketched below. Answer the following question assuming that the semiconductor is silicon at room temperature.

4a) Is the semiconductor N-type or P-type? Explain your answer.
4b) What is the thickness of the oxide?
4c) What is the thickness of the depletion layer in inversion?
4d) Explain how you could calculate the doping density of the semiconductor.
5) In modern MOSFETs, the gate oxide SiO$_2$ has been replaced with a higher dielectric constant material. Different oxides are compared to SiO$_2$ in terms of the “Equivalent Oxide Thickness” (EOT). EOT is the thickness of SiO$_2$ that would give the same capacitance per unit area. (Capacitance Equivalent Thickness, CET, is another quantity; CET also incorporates the effect of the finite semiconductor capacitance in inversion.) What is the EOT of 4 nm of hafnium dioxide, HfO$_2$, which has a relative dielectric constant of 25?

6) The body effect coefficient, $m = \left(1 + C_S / C_{ox}\right)$, is an important MOS parameter. Typical values are said to be $1 < m < 1.4$, but since $m$ varies with gate bias, we should ask what bias these typical numbers refer to. Consider an MOS capacitor with a gate oxide 1.2 nm thick. The Si substrate doping is $N_A = 10^{18}$ cm$^{-3}$ and answer the following questions. (Assume room temperature conditions).

6a) Compute $m$ for below threshold conditions. Assume that the depletion layer width is $W_D(\Psi_S) = W_D(2\Psi_B) = W_T$.

6b) Compute $m$ for above threshold, strong inversion conditions. Assume that the sheet density of electrons in the inversion layer is $n_S = 10^{13}$ cm$^{-2}$ and that

$|Q_n| = qn_S \approx \sqrt{2\kappa_S e_0 k_B T n_i^2 / N_A} e^{+q\Psi_s/2k_BT}$.

6c) Use the results from 6a) and 6b) to explain why the surface potential is easy to change with a gate voltage below threshold but hard to change above threshold.

7) This problem concerns an MOS capacitor that consists of a metal electrode, a 2 nm thick silicon dioxide layer with $\kappa_{ox} = 3.9$, and a silicon substrate ($\kappa_S = 11.8$) that begins at $x = 0$. The electric field in the semiconductor is shown below. Assume that there is no charge at the oxide-Si interface, and no charge in the oxide.

Answer the following questions.
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7a) What is the surface potential, $\psi_s$? (Assume that the potential is zero deep in the semiconductor.
7b) What is the doping density in the semiconductor?
7c) What is the electric field in the oxide?
7d) What is the voltage drop across the oxide?
7e) What is the electrostatic potential in the metal gate?

8) The energy band diagram for an MOS capacitor is sketched below. Assume $T = 300$ K and an oxide thickness of $t_{ox} = 1.1$ nm, and an intrinsic carrier concentration of $n_i = 1 \times 10^{10}$ cm$^{-3}$. Answer the following questions using the depletion approximation as needed. (Note that $E_F = E_i$ at the oxide-silicon interface.)

8a) What is the surface potential?
8b) Sketch the electrostatic potential vs. position inside the semiconductor. Label the surface potential on your sketch.
8c) Sketch the electric field vs. position inside the oxide and semiconductor
8d) Do equilibrium conditions apply inside the semiconductor? Explain
8e) Sketch the hole concentration vs. position inside the semiconductor.
8f) What is the hole concentration in the bulk?
8g) What is the hole concentration at the surface?
8h) What is the gate voltage?
8i) What is the voltage drop across the oxide?
9) Consider an MOS capacitor with a gate oxide 1.2 nm thick. The Si substrate doping is $N_A = 10^{18}$ cm$^{-3}$. The gate voltage is selected so that the sheet density of electrons in the inversion layer is $n_S = 10^{13}$ cm$^{-2}$. Assume room temperature and that

$$|Q_n| = qn_S \approx \sqrt{2\kappa_S e_0 k_B T n_i^2/N_A} e^{+q\psi_s/k_B T} \text{ C/cm}^2.$$ 

Answer the following questions.

9a) What is the surface potential? Compare it with $2\psi_B$.
9b) How much does the surface potential need to increase to double the inversion layer density?
9c) How much does the gate voltage need to increase to double the inversion layer density?
9d) Explain in words why it is difficult to increase the surface potential for an MOS capacitor above threshold.

10) Gate work functions must be chosen to produce the desired threshold voltage. If there is a difference between the metal gate and the semiconductor, then the flat-band voltage is not zero. Consider the “mid-gap” work function shown below and assume that the semiconductor is silicon at room temperature with $N_C = 3.23 \times 10^{19}$ cm$^{-3}$ and $N_V = 1.83 \times 10^{19}$ cm$^{-3}$.

10a) If the semiconductor is N-type with $N_D = 10^{18}$ cm$^{-3}$, then what is the flat-band voltage? \textbf{Explain} the sign of the flat-band voltage.
10b) If the semiconductor is P-type with $N_A = 10^{18}$ cm$^{-3}$, then what is the flat-band voltage? \textbf{Explain} the sign of the flat-band voltage.
11) Assume an MOS capacitor on a P-type Si substrate with the following parameters:

\[ N_A = 2.7 \times 10^{18} \text{ cm}^{-3} \text{ for the bulk doping} \]
\[ Q_F = 0 \text{ (no charge at the oxide-Si interface)} \]
\[ t_{ox} = 1.1 \text{ nm} \]
\[ \kappa_{ox} = 3.9 \]
\[ T = 300 \text{ K} \]
\[ V_{G} = 1 \text{ V} \]

Also assume that the structure is ideal with no metal-semiconductor work function difference. When working MOS problems, it is easiest to assume a surface potential, and then calculate the gate voltage that produced it, but in practice, we only have access to the gate terminal. In this problem, you are given the gate voltage and will be asked to find the surface potential. You may assume the depletion approximation, but you must check to be sure that it is valid.

Find the surface potential, \( \psi_S \).

12) Until recently, the gate electrode of an MOS capacitor was usually a heavily doped layer of polycrystalline silicon with the Fermi level located at \( E_F \approx E_C \) for an n+ polysilicon gate and \( E_F \approx E_V \) for a p+ polysilicon gate. Sketch the following four equilibrium energy band diagrams:

12a) An n-type Si substrate with an n+ polysilicon gate
12b) An n-type Si substrate with a p+ polysilicon gate
12c) A p-type Si substrate with an n+ polysilicon gate
12d) A p-type Si substrate with a p+ polysilicon gate