Unit 1: Transistor Fundamentals

Lecture 1.3: MOSFET Device Metrics

Mark Lundstrom

lundstro@purdue.edu
Electrical and Computer Engineering
Birck Nanotechnology Center
Purdue University, West Lafayette, Indiana USA

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MOSFET IV characteristics

common source

\[ I_{DS}(V_G, V_S, V_D) \]

\[ I_{DS}(V_{GS}) \text{ at a fixed } V_{DS} \text{ transfer} \]

\[ I_{DS}(V_{DS}) \text{ at a fixed } V_{GS} \text{ output} \]
Output characteristics

\[ V_D : 0 \rightarrow V_{DD} \]

\[ V_G : 0 \rightarrow V_{DD} \]

n-channel enhancement mode MOSFET

\[ I_{DS} \quad V_G = V_{DD} \]
\[ V_{G3} > V_{G2} \]
\[ V_{G2} > V_{G1} \]
\[ V_{G1} \]
\[ V_{G0} < V_{G1} \]

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Output characteristic at a specific $V_{GS}$

n-channel enhancement mode MOSFET

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Output characteristics

Above threshold: $V_{GS} > V_T$

Below threshold: $V_{GS} < V_T$

Linear region: $V_D < V_{DSAT}$

Saturation region: $V_D > V_{DSAT}$

Drain saturation voltage: $V_{DSAT}$

Output resistance: $r_o$

**Drain-Source resistance:** $R_{SD}$
MOSFET device metrics (i)

- **Output resistance:**
  \[ r_o \ (\Omega - \mu m) \]

- **On-current (μA/μm):**
  \[ I_{DS}(V_{GS} = V_{DS} = V_{DD}) \]

- **Transconductance:**
  \[ g_m = \left. \frac{\Delta I_{DS}}{\Delta V_{GS}} \right|_{V_{DS}} \ (\mu S/\mu m) \]
Output vs. **transfer** characteristics

output characteristics

\[ I_{DS} \]
\[ V_{GS} \]
\[ V_{DSAT} \]

Fix **gate** voltage then sweep the **drain** voltage

transfer characteristics

\[ I_{DS} \]
\[ V_{DS1} \]
\[ V_T \]
\[ V_{GS} \]

Fix **drain** voltage then sweep the **gate** voltage
Transfer characteristics

$V_{DS2} = V_{DD} > V_{DS1}$

$V_{DS1} = 0.05 \, \text{V}$

"threshold voltage"
MOSFET transfer characteristics

\[ I_{DS} \] (mA/\( \mu \)m)

\[ V_{GS} \]

\[ V_{DS} = V_{DD} \]

\[ V_{DS} = 0.05 \text{ V} \]

\[ V_{TSAT} \]

\[ V_{TLIN} \]

\[ V_{DD} \]

threshold voltage
MOSFET device metrics (ii)

\[ \log_{10} I_{DS} \quad \text{(mA/\mu m)} \]

Transfer characteristics:

- Off-current

- Subthreshold swing: \( (\text{mV/decade}) \)

- \( V_{DS} = V_{DD} \)

- \( I_{ON} \)

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MOSFET device metrics (iii)

transfer characteristics:

\[ \log_{10} I_{DS} \]

\( (\text{mA/}\mu\text{m}) \)

\[ V_{DS} = V_{DD} \]

\[ V_{DS} = 0.05 \text{ V} \]

DIBL (drain-induced barrier lowering) \( (\text{mV/V}) \)

\[ I_{ON} \]

\[ V_{GS} \]

\[ V_{DD} \]

\[ V_{T} \]
Summary

Given the measured characteristics of a MOSFET, you should be able to determine:

1. on-current: \( I_{ON} \)
2. off-current: \( I_{OFF} \)
3. subthreshold swing, SS
4. drain induced barrier lowering: DIBL
5. threshold voltage: \( V_T (\text{lin}) \) and \( V_T (\text{sat}) \)
6. Drain to source resistance: \( R_{DS} \)
7. drain saturation voltage: \( V_{DSAT} \)
8. output resistance: \( r_o \)
9. transconductance: \( g_m \)

Our goal is to understand these device metrics.
Example: 32 nm N-MOS technology

Answers

\[
\begin{align*}
I_{ON} & \approx 1.55 \text{ mA/\mu m} \\
I_{OFF} & \approx 0.1 \text{ \mu A/\mu m} \\
SS & \approx 95 \text{ mV/decade} \\
\text{DIBL} & \approx 110 \text{ mV/V} \\
R_{DS} & \approx 200 \text{ \Omega-\mu m} \\
r_o & \approx 2.5 \text{ K\Omega-\mu m} \\
g_m & \approx 3 \text{ mS/\mu m} \quad \text{(in the on-state)} \\
V_T & \approx 0.3 - 0.4 \text{ V} \\
V_{DSAT} & \approx 0.4 \text{ V} \quad \text{(for } V_{GS} = V_{DD})
\end{align*}
\]

(These values were read off of the plots on the previous slide and are only rough estimates.)
N-channel vs. P-channel MOSFET

n-MOSFET

\[ V_S = 0 \quad V_G > V_T \quad V_D > 0 \]

p-MOSFET

\[ V_S = 0 \quad V_G < V_T \quad V_D < 0 \]

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Example: 32 nm P-MOS technology

Lecture 1.3 Wrap-up

We have learned how to extract some key device parameters (e.g. threshold voltage, drain saturation voltage) and device performance metrics (e.g. on-current and off-current).

Most of the course is about understanding the $IV$ characteristics of nanoscale MOSFETs – qualitatively and quantitatively.

But in the next lecture, we’ll discuss some of the reasons for the device metrics (e.g. why is a high on-current important?).