Fundamentals of Nanotransistors

Unit 2: MOS Electrostatics

Lecture 2.7: 2D MOS Electrostatics

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Lundstrom: Nanotransistors 2015
Bulk MOSFETs

We have been discussing electrostatics normal to the channel.

MOSFET operation is determined by the 2D energy bands, which vary in space according to the 2D electrostatic potential: \( \psi(x, y) \)
Effect of 2D electrostatics on $I_{DS}$ vs. $V_{GS}$

1) DIBL increases with decreasing $L$ and increasing $V_{DS}$
2) SS may increase with decreasing $L$ and increasing $V_{DS}$
3) “Punchthrough” is a severe 2D effect.
2D Poisson equation

\[ \nabla \cdot \vec{D}(x,y) = \rho(x,y) \]

\[ \vec{D}(x,y) = \varepsilon_s \vec{\mathcal{E}}(x,y) \]

\[ \vec{\mathcal{E}}(x,y) = -\nabla \psi(x,y) \]

\[ \frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon_s} \]
2D Poisson equation

1) 1D MOS Capacitor:

\[ \frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho}{\varepsilon_S} = \frac{qN_A}{\varepsilon_S} \quad \text{(below } V_T \text{)} \]

2) 2D MOSFET:

\[ \frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A}{\varepsilon_S} \quad \text{(below } V_T \text{)} \]

“gradual channel approximation”

\[ \frac{\partial^2 \psi}{\partial y^2} \gg \frac{\partial^2 \psi}{\partial x^2} \quad \text{(long channel)} \]
Understanding $V_T$ reduction

1) Short channel MOSFET below threshold:

\[
\frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A}{\varepsilon_S} - \frac{\partial^2 \psi}{\partial x^2}
\]

\[
\frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A|_{\text{eff}}}{\varepsilon_S}
\]

\[
N_A|_{\text{eff}} < N_A
\]

\[
V_T = V_{FB} + \frac{\sqrt{2qN_A\varepsilon_S(2\psi_B)}}{C_{ox}} + 2\psi_B
\]

(Lecture 2.3) Lundstrom: Nanotransistors 2015
Barrier lowering view

Ideally, only the gate controls the barrier height

\[ I_{DS} \sim e^{-E_B/k_BT} \]

\[ E_B = q(V_{bi} - \psi_S) \]

current does not change

\[ q(V_{bi} - \psi_S) \]

low \( V_{DS} \)

high \( V_{DS} \)

drain depletion layer expands

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No barrier lowering $\Rightarrow$ no DIBL

\[
\log I_{DS} = e^{(V_{GS} - V_T)/mk_BT_L}
\]

$V_{DS} = 1.0 \text{ V}$

$V_{DS} = 0.05 \text{ V}$

no DIBL
Barrier lowering

\[ E_C(x, y = 0) \]

\[ \Delta E_B \]

\[ q(V_{bi} - \psi_S) \]

Drain-Induced Barrier Lowering (DIBL)

\[ I_{DS} \sim e^{-E_B/k_BT} \]

\[ \frac{\Delta I_{DS}}{I_{DS}} = e^{\Delta E_B/k_BT} \]

low \( V_{DS} \)

high \( V_{DS} \)

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Barrier lowering increases current

\[ \log I_{DS} \]

\[ V_{DS} = 1.0 \text{ V} \]
\[ V_{DS} = 0.05 \text{ V} \]

\[ \Delta I_{DS} = I_{DS}e^{\Delta E_B/k_B T} \]

SS is still independent of \(|V_{DS}|\).
Punchthrough

\[
\log I_{DS} = e^{(V_{GS}-V_T)/mk_BT}
\]

\[
V_{DS} = 1.0 \text{ V}
\]

\[
V_{DS} = 0.05 \text{ V}
\]

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Punchthrough

\[ N_A \text{ (min)} : \text{punch through} \]

\[ W_S + W_D < L \]
A “well-tempered MOSFET”

(Dimitri Antoniadis, MIT)

The height of the barrier should be controlled by the gate voltage; the drain voltage should have only a small effect.
Controlling 2D electrostatics
(also known as “short channel effects”)

Need to design a short channel device to minimize 2D effects.

**Question**: How do we control 2D electrostatics in short channel MOSFETs?

**Answer**: Screen out the 2D fields.
Screening by free carriers

\[ \psi(r) = \frac{q}{4\pi \varepsilon_s r} e^{-r/L_D} \]

\[ L_D = \sqrt{\frac{\varepsilon_s k_B T}{q^2 n_0}} \]

Debye length

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Geometric screening length: bulk MOSFET
Geometric screening length: DG MOSFET

\[ T_{OX} = 1 \text{ nm} \]

Off-state: \( V_G = 0V, \ V_D = 1V, \ I_{off} = 0.1\mu A/\mu m \) (by H. Pal, Purdue, 2012)
Non-planar MOSFETs


Computing $\Lambda$

\[
\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon_s} = -\frac{qN_A(x,y)}{\varepsilon_s} 
\]

$\Lambda_{NW} < \Lambda_{DG\,SOI} < \Lambda_{SOI} < \Lambda_{BULK}$

$L_{\text{min}} \approx 3\Lambda$


2D electrostatics

\[ \frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{-qN_A(x,y)}{\varepsilon_S} \]

1) Effective doping

2) Barrier lowering

3) Geometric screening length

4) Capacitor model (lecture notes)
“Well-tempered MOSFET”

1) \( Q_n(0) \approx -C_{inv}(V_{GS} - V_T) \)

\[ V_T = V_{T0} - \delta V_{DS} \]
\( m = \text{constant} \)

2) region under strong control of gate \((m \sim 1)\)

3) Additional increases in \( V_{DS} \) beyond \( V_{DSAT} \) drop near the drain and have a small effect on \( I_{DS} \) (small DIBL)
“Well-tempered MOSFET”

$E_X$ vs. $x$ for $V_{GS} = 0.5V$

Example

$L = 105 \text{ nm}$

$L = 85 \text{ nm}$

(Courtesy, Shuji Ikeda, ATDF, Dec. 2007)

Increased DIBL and SS
2D MOS electrostatics degrade device performance (increases DIBL and SS).

The goal of MOSFET design is to make 1D electrostatics hold at the VS – with small DIBL and a SS parameter, $m$, which is nearly one.

The way to achieve this is to engineer the device such that the gate voltage controls the height of the source to channel energy barrier.

Next Lecture: Let’s re-visit the VS model.