Provide a numerical answer to the question below.

Traditionally, SiO$_2$ has been used as the gate dielectric for MOS transistors. As transistor dimensions scaled down to pack more transistors per chip, the thickness of the SiO$_2$ had to be reduced. It turns out that an SiO$_2$ thickness of 1 nm is too thin; it results in too much gate current. Answer the following question.

- **Compute the electron transmission of an SiO$_2$ layer that is 1 nm thick.**

  Use our expression for the transmission of a tunnel barrier,

  
  
  and assume that the barrier height is

  
  
  You may also assume that the effective mass is.