Homework 7: Gate Dielectric Breakdown: Statistics, Correlation, Projection

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In the class, we derived a set of formula for the statistics of soft and hard breakdown. In this HW, we will make sure that you can derive the relationships and understand their limitations.

Part I: Analytical Formula for Correlated Breakdown

1. Prove that the IDDQ of an IC with many soft breakdowns is given by \( L = (e^{\xi x} - 1)/\xi \). Show that the formula reduces to the appropriate limit when time-correlation is absent.

2. Show that the pair-cumulative probability distribution of two breakdown spots separated by a distance \( x \) (on a 1D line) is given by \( P_2[ x_l - x_j < x ] = x(2 - x)/L_c(2 - L_c) \), where \( L_c \) is distance the maximum distance of the second breakdown with respect to the first breakdown.

3. (Optional) Consider a gate dielectric shaped as a circle. Show that the CDF between the two breakdown spots located at \((x_1, y_1)\) and \((x_2, y_2)\) separated by a distance \( l \) is given by

\[
P(l) = 4l [ 1 - (1/2 + \pi/4)l + l^2/3 ]
\]

Part 2: A Comprehensive calculation of dielectric lifetime that weaves the pieces together

A. Determining mean-lifetime at operating conditions

In a particular TDDB experiment, 81 NMOSFETs (area=2.5 \( \mu \)m\(^2\), Channel length=0.25 \( \mu \)m, channel width=10 \( \mu \)m, \( T_{ox}=2.5 \) nm) are placed in three groups so that each group contains 27 transistors. The transistors are stressed at 3.75, 4, and 4.5 volts with mean failure times (of 27 transistors in each group) of 15980 sec, 1238 sec, and 1.2 sec, respectively. The Weibull slope of each group is determined by Maximum likelihood technique and is given by \( \beta = 1.8 \) with a variation of 0.2.
a) For these transistors, what is the mean time to failure at 1.5 volts? At 2.0 volts? For simplicity, use the simple scaling rule that $T_{BD}(V_1)/T_{BD}(V_2) = \exp[\gamma_V(V_1 - V_2)]$, where $\gamma_V$ is the voltage acceleration factor (Note: Be careful about units of $\gamma$: decades/volts, number/volt).

b) Assume that an IC made of this technology has individual transistor of size 0.25 $\mu$m x 1 $\mu$m. What is the mean lifetime of an IC with 100 million transistors?

c) If the IC must survive 10 years with 50% probability, what is the safe operating voltage?

d) If we can not let more than 1 in 10000 ICs returned due to TDDB failure, what is the safe operating voltage?

e) Instead of 100 million transistors, if the IC contains 10 million transistors, would the safe operating voltage be higher and lower? Why?

f) (optional) What are the uncertainty limits of safe operating voltage due to uncertainty in $\beta$.

B. Nonlinear voltage acceleration (Optional)

Anode hole injection theory predicts that the voltage acceleration factor $\gamma$ is not a constant, but increases with decreasing voltages.

a) Is the empirical value of $\gamma_V$ determined above consistent with values in Fig. 2?

b) Use piecewise approximation (e.g., 4-3.5 volts, 3.5-3 volts, < 3V) for $\gamma(V)$ recalculate the values of (a-e) in Section 1. How does the nonlinearity in voltage acceleration changes the safe operating conditions?

C. Scaling to thinner oxides

As a CTO of your company, you want to decide if it would be safe to adopt 90 nm technology with 1.5 nm gate oxides:

a) Determine $\beta$ from Fig. 3 for 1.5 nm oxides (This figure is the proof that Weibull slope scales linearly with oxide thickness).

b) Recalculate the mean-time to failures for the same 100 million transistors (size 0.13 $\mu$m x 1 $\mu$m). Recalculate the safe-operating voltage using both linear and nonlinear voltage acceleration models. Assume NMOS transistors dictate TDDB lifetime.

c) What would be the PMOS TDDB lifetime and safe operating voltages be under these conditions. Should $\beta$ for 1.5 nm oxide in PMOS be different from that of NMOS transistor? Why or why not? Which of the figure below should you use to calculate the voltage acceleration factors for PMOS?
D. Statistics of multiple Breakdown

a) If the 100-million transistor IC discussed above can survive three breakdown events as a whole (3 separate transistors having one breakdown each), what is the net increase in lifetime of the technology compared to those that can survive no more than one breakdown event? (Assume 100 ppm failure fraction, F).

b) If every transistor can survive two breakdown events, what is the increase in IC lifetime?

![Fig. 1](image1.png)

Fig. 1: For NMOS/PMOS TBD failure times, the rightmost curve is for 1.4 nm oxides, the middle curve for 2.0 nm oxides, and the rightmost curve is for 2.4 nm oxides. Gate oxide area is 2.5 $\mu$m$^2$.

![Fig. 2](image2.png)

![Fig. 3](image3.png)

Fig. 2: NMOS voltage acceleration factors. The numbers are compiled from data like those in Fig. 1.

Fig. 3: Weibull slopes for different oxide thicknesses. Each data point is related to a specific oxide thickness (see Fig. 1).
References:


