

*Spring 2019 Purdue University*

# **ECE 255: L12**

## **BJT Bias Circuits**

(Sedra and Smith, 7<sup>th</sup> Ed., Sec. 6.3)

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Lundstrom: 2019

# Announcements

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**Exam 1: Thursday, Feb. 7, 6:30 PM, LILY 1105.**

(Weeks -1- 4 topics, semiconductors, diodes, **BJTs**. i.e. HW1-HW4)

**Two practice exams are posted on BlackBoard**

**Graded HW can be picked up in EE 326B (Mary Ann Satterfield)**

**Professor Janes will conduct a help session for Exam 1 on Thursday, 2/7 at 1:30 PM in ME 1061.**

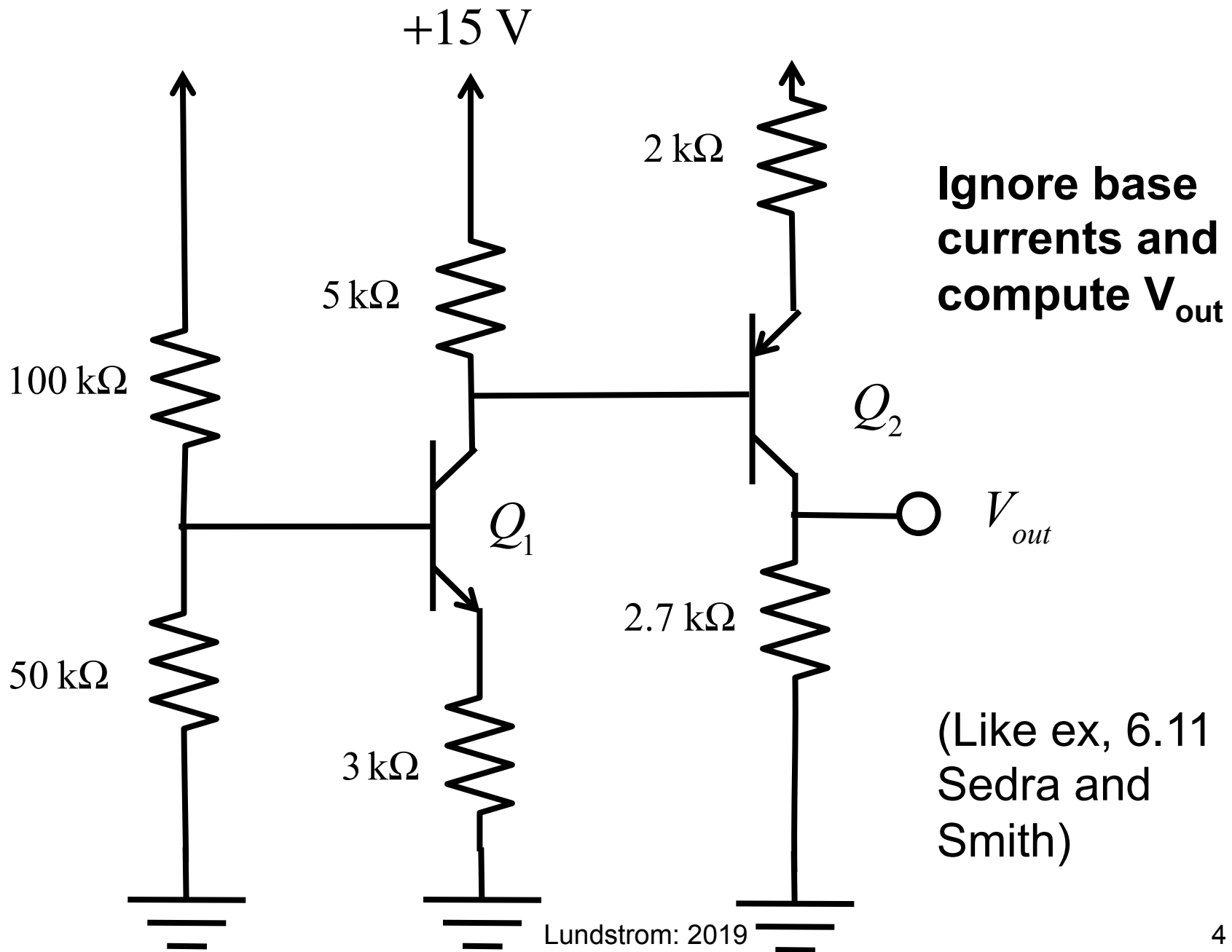
**Spice 1 project postponed until Monday, Feb. 11**

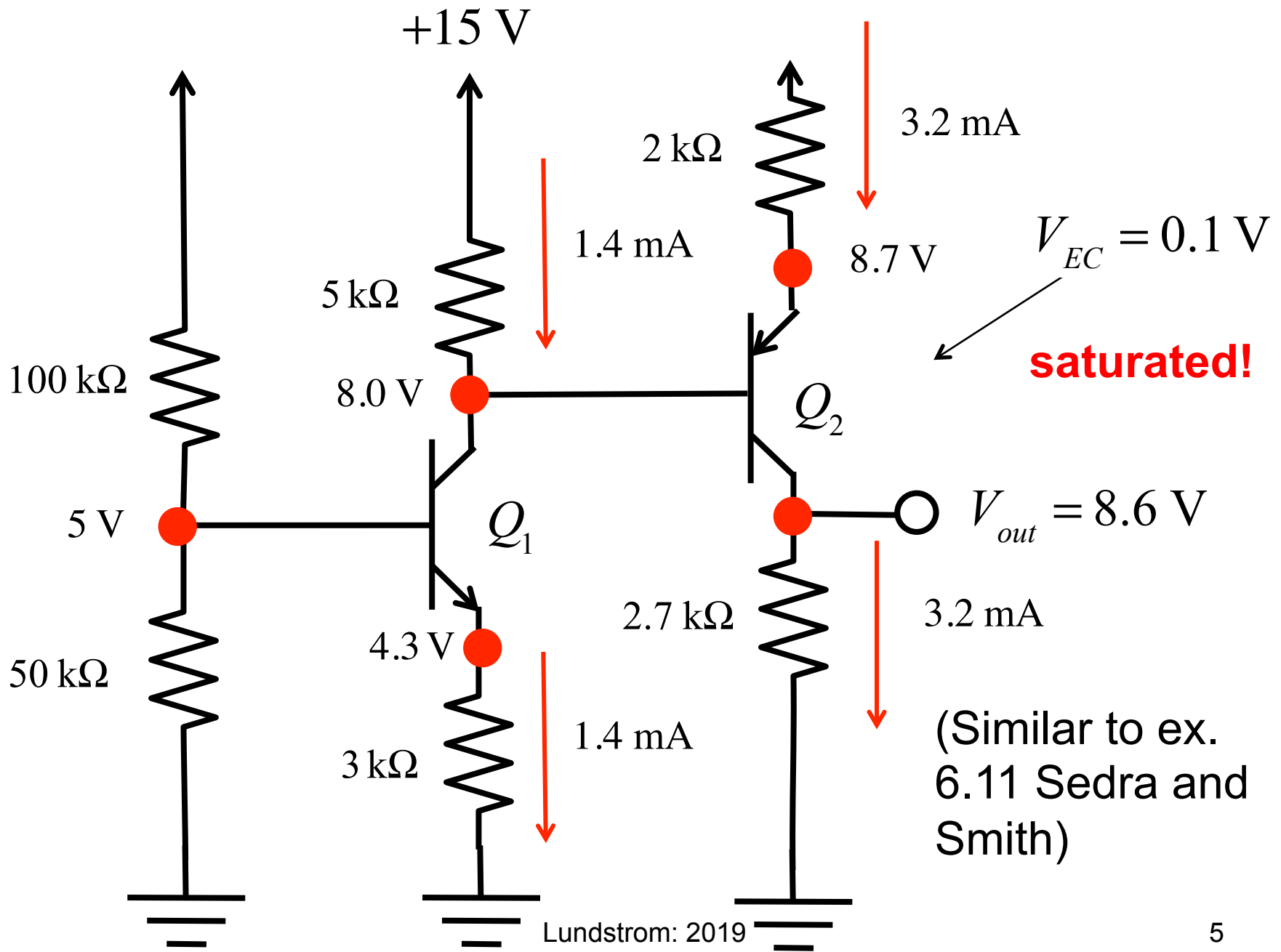
**There **will** be class on Friday, Feb. 8.**

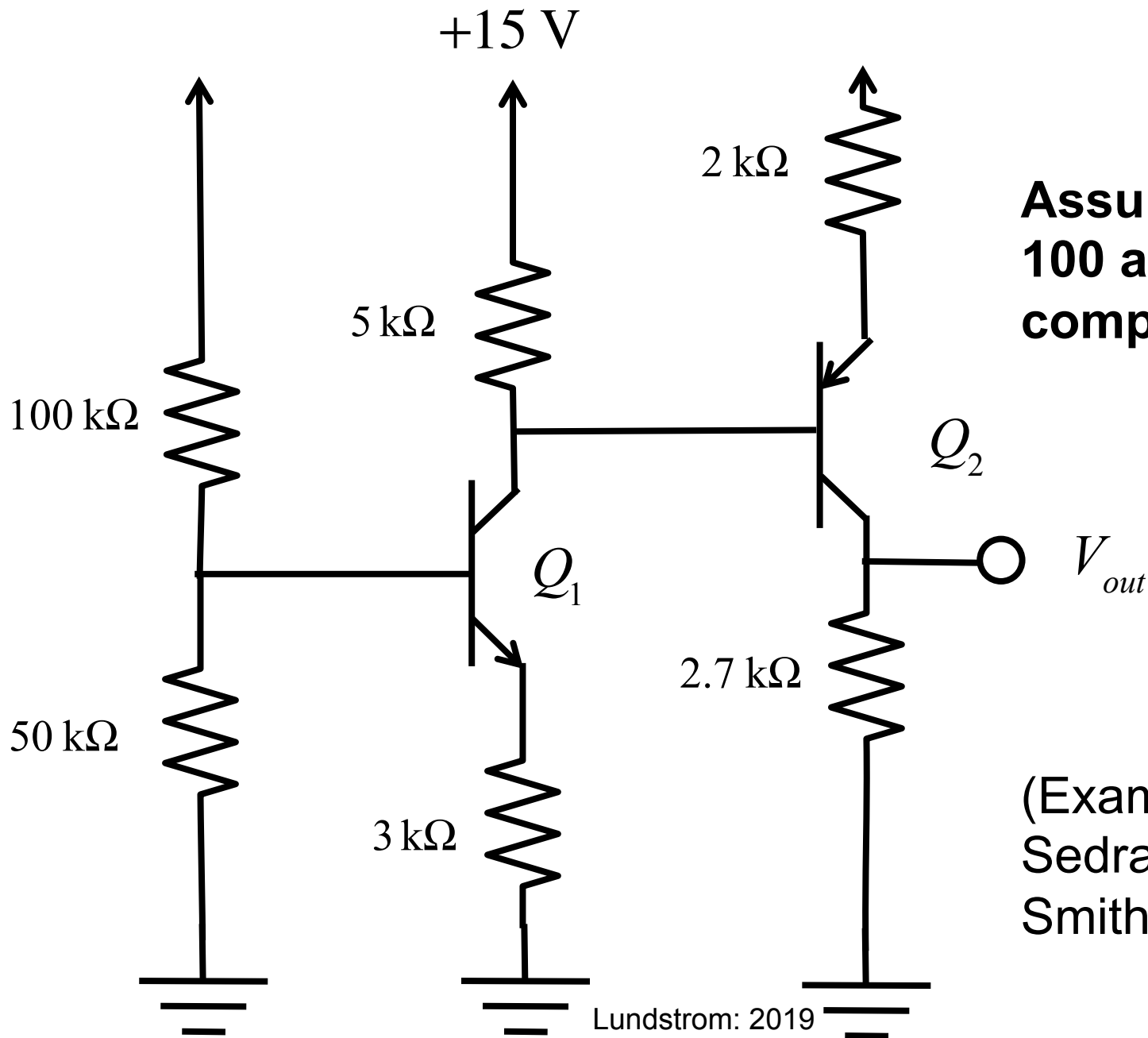
# DC bias circuits

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- 1) NPN and PNP circuits
- 2) Bias circuits (discrete)







**Assume beta = 100 and compute  $V_{out}$**

(Example 6.11 Sedra and Smith)

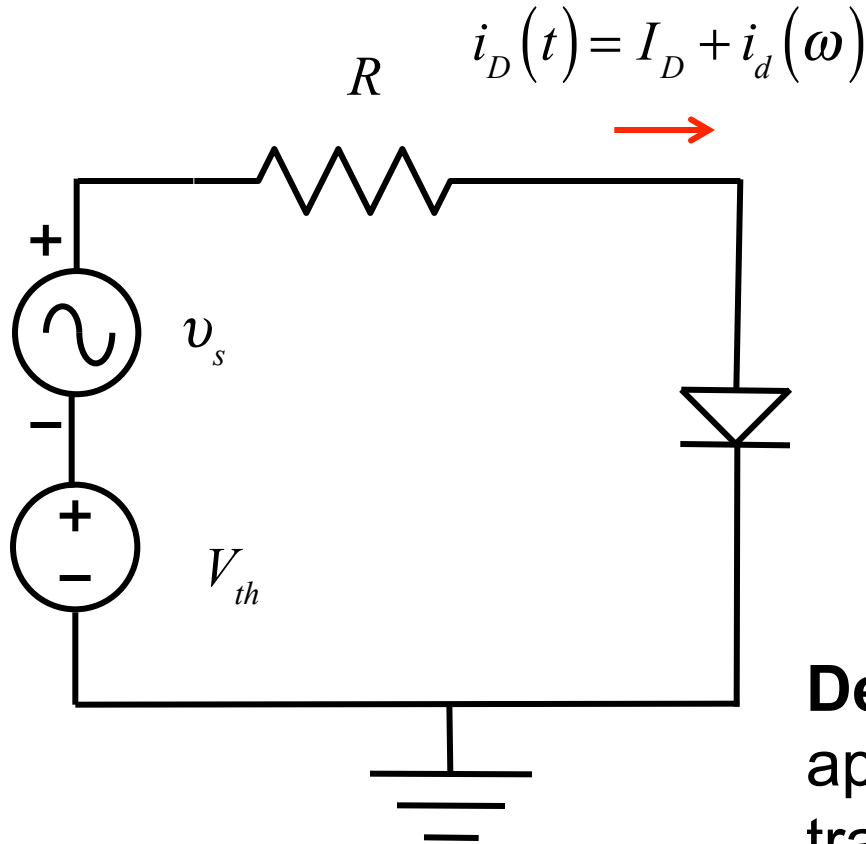
# BJT bias circuits

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- 1) NPN and PNP circuits
- 2) **Bias circuits (discrete)**

# Diode bias circuits

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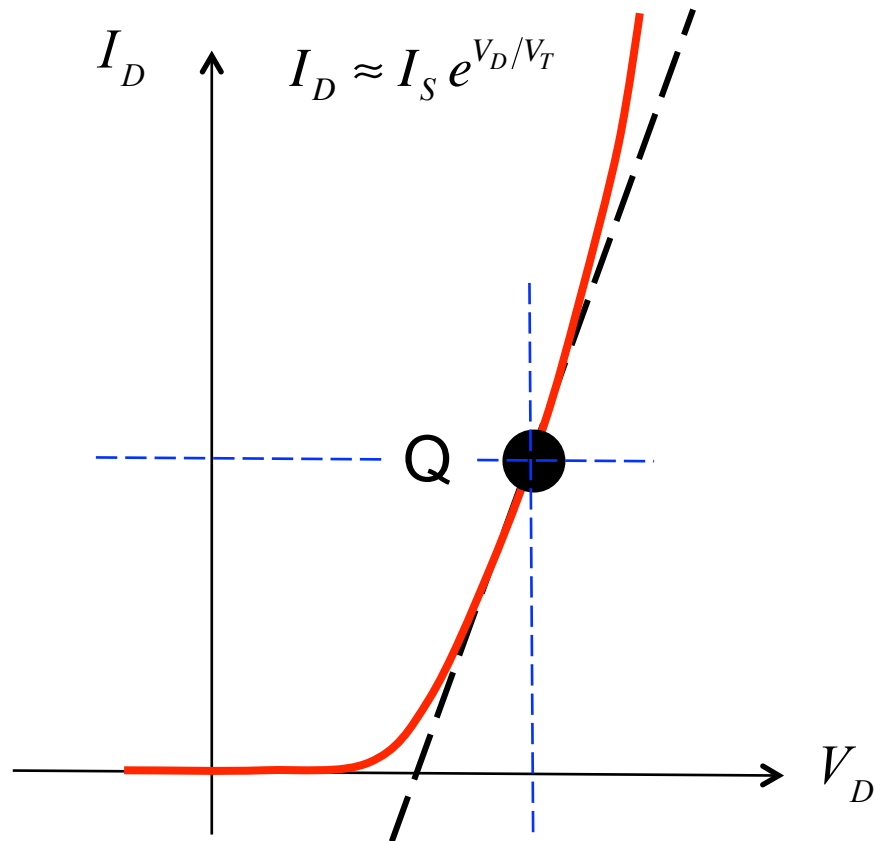
$$i_D(t) = I_D + i_d(\omega)$$

$$v_D(t) = V_D + v_s(\omega)$$

**Definition:** Bias: A voltage applied to a device (such as a transistor control electrode) to establish a reference level for operation.



# Diode bias circuits

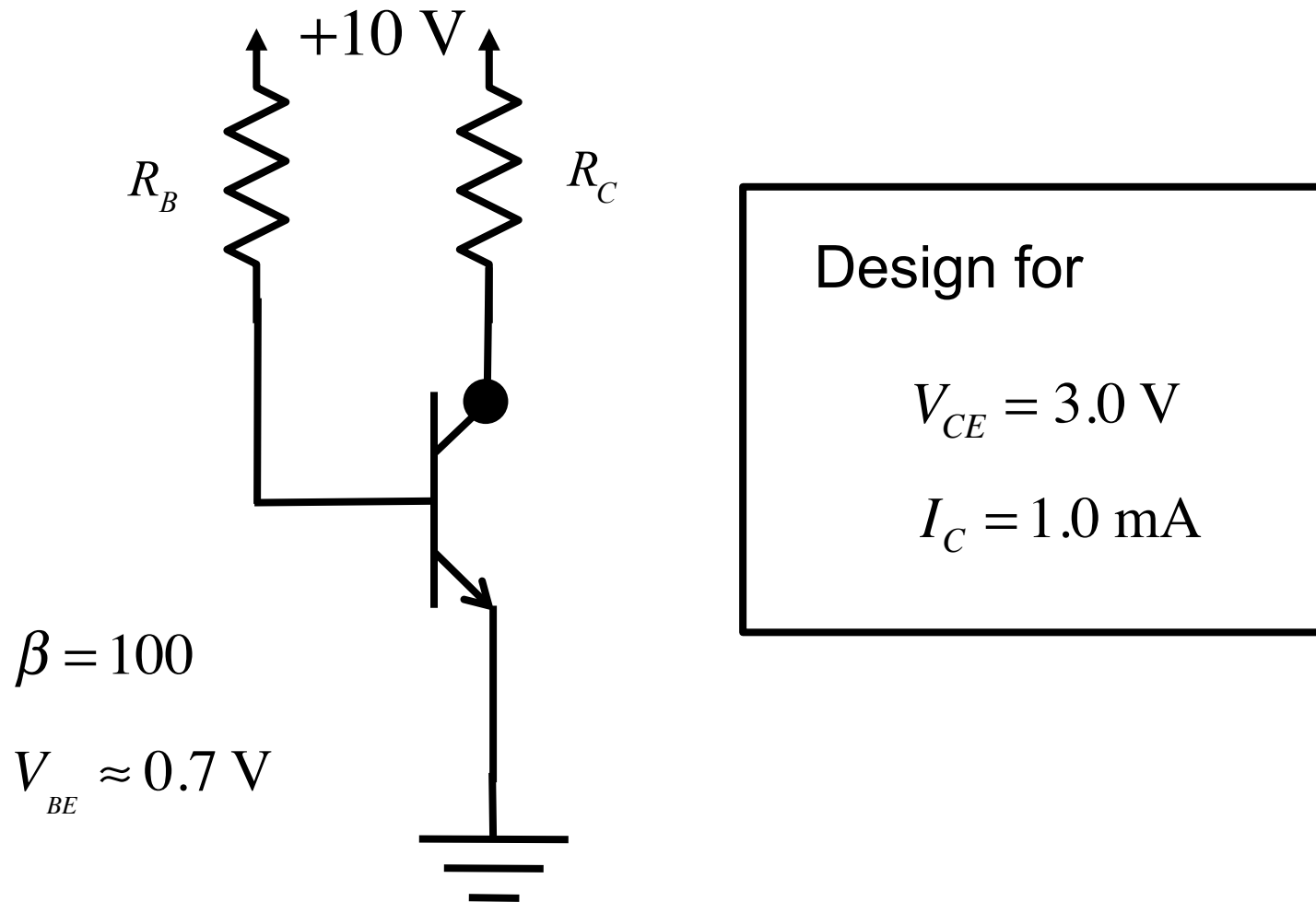


$$g_d = \left. \frac{dI_D}{dV_D} \right|_Q = \frac{1}{r_d}$$

$$r_d = \frac{V_T}{I_D} \Omega$$

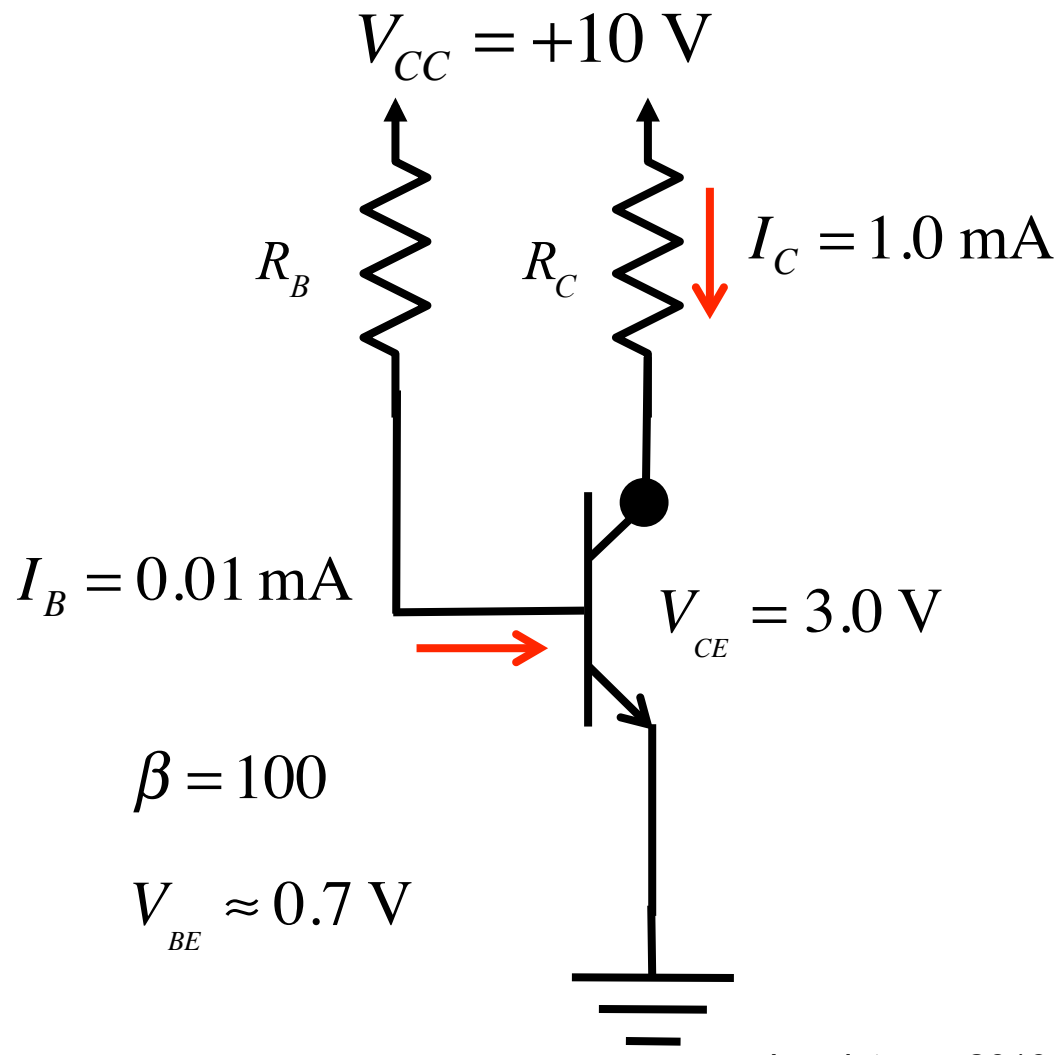
# Transistor bias circuit design

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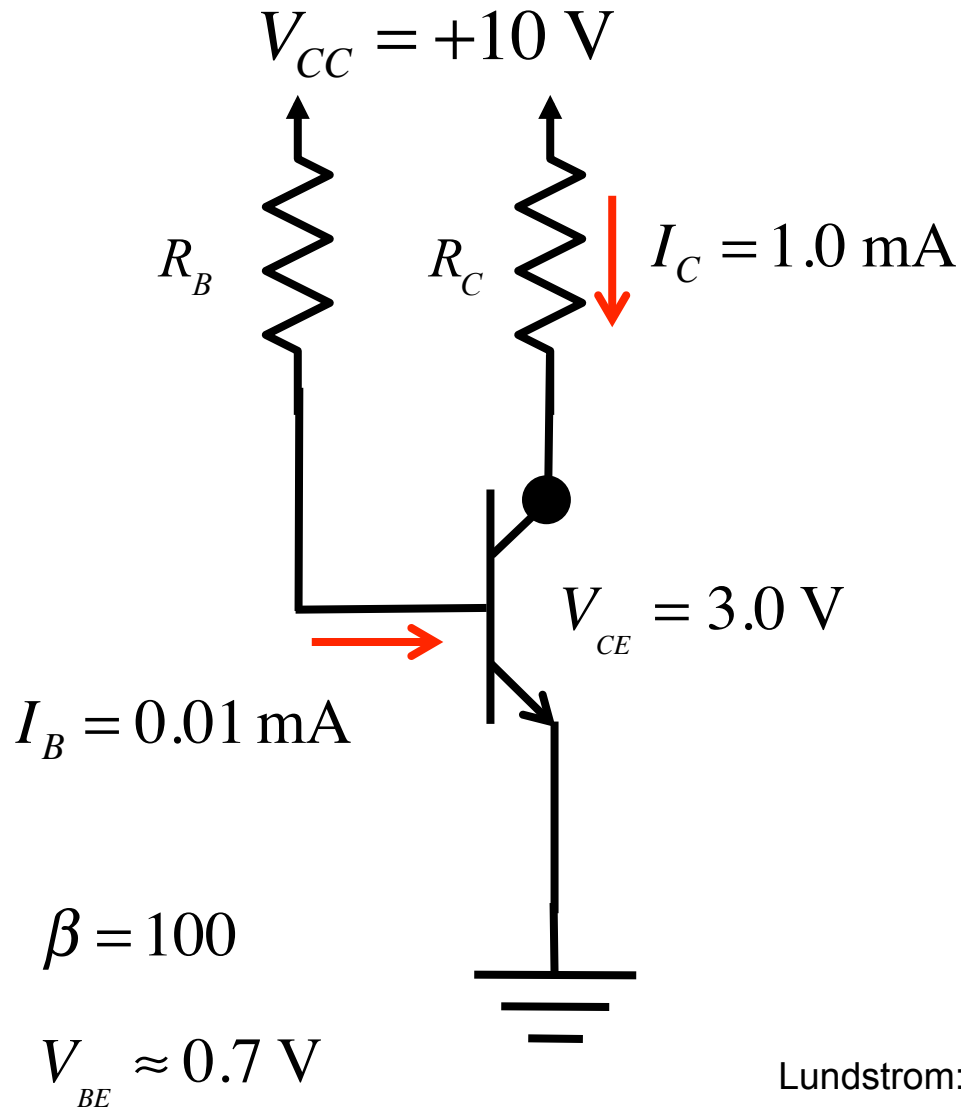


# Bias circuit design

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# Bias circuit design



$$I_C R_C = 7 \text{ V} \rightarrow R_C = 7 \text{ k}\Omega$$

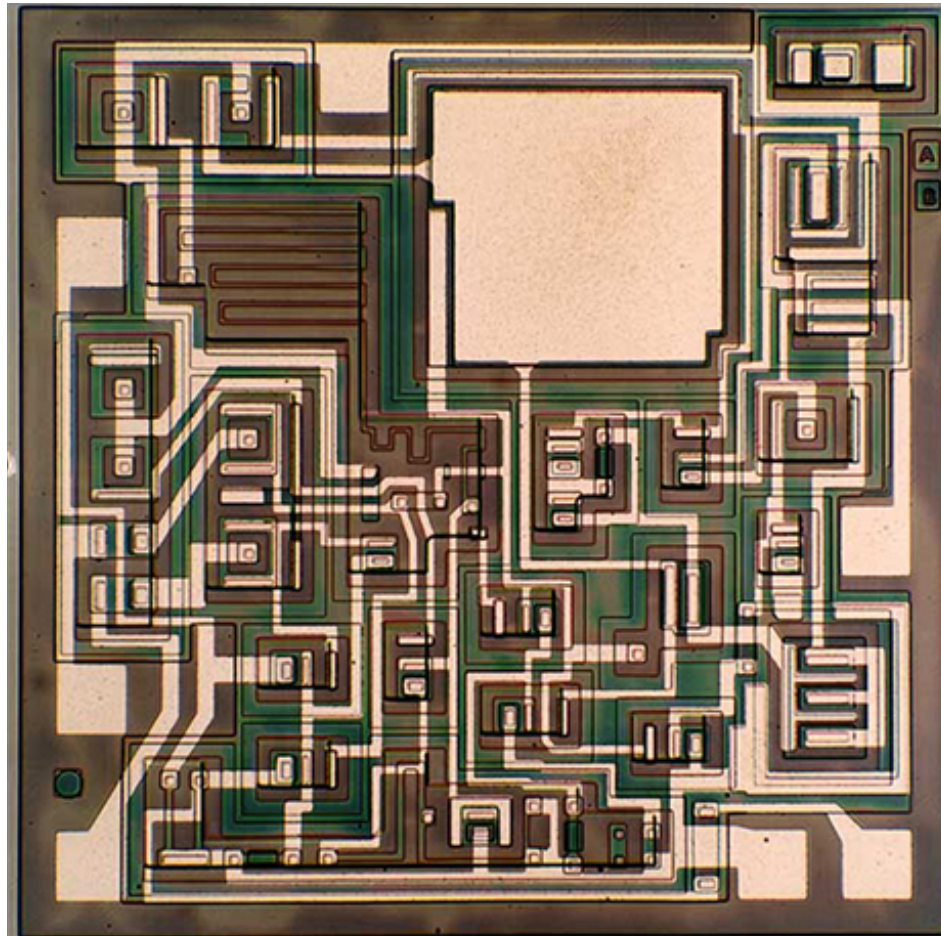
$$I_B = \frac{I_C}{\beta} = \frac{1 \text{ mA}}{100} = 0.01 \text{ mA}$$

$$I_B R_B = 9.3 \text{ V}$$

$$R_B = \frac{9.3 \text{ V}}{0.010 \text{ mA}} = 930 \text{ k}\Omega$$

# 741 Op amp

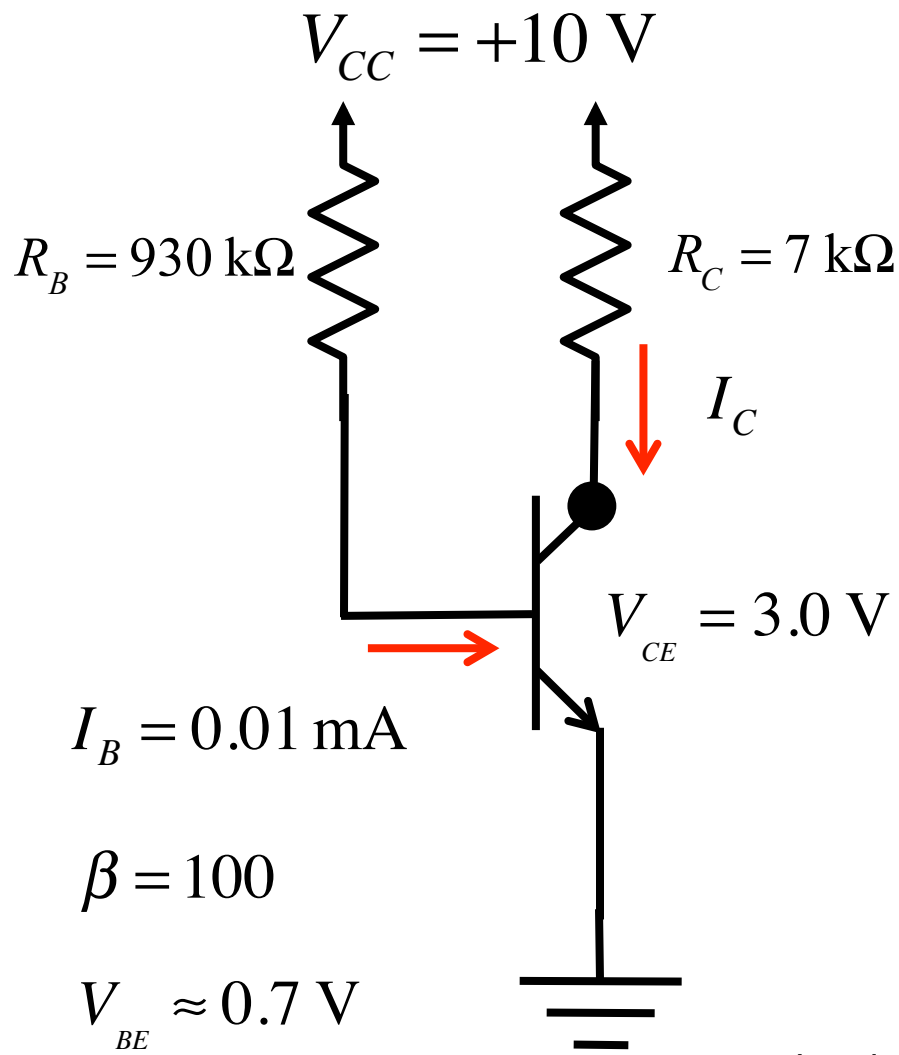
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David Fullagar

*IEEE Spectrum*, "Chip Hall of Fame: Fairchild Semiconductor  $\mu$ A741 Op-Amp," June 30, 2017

## Bad Bias circuit design



$$I_C = \beta I_B = \beta \left( \frac{V_{CC} - V_{BE}}{R_B} \right)$$

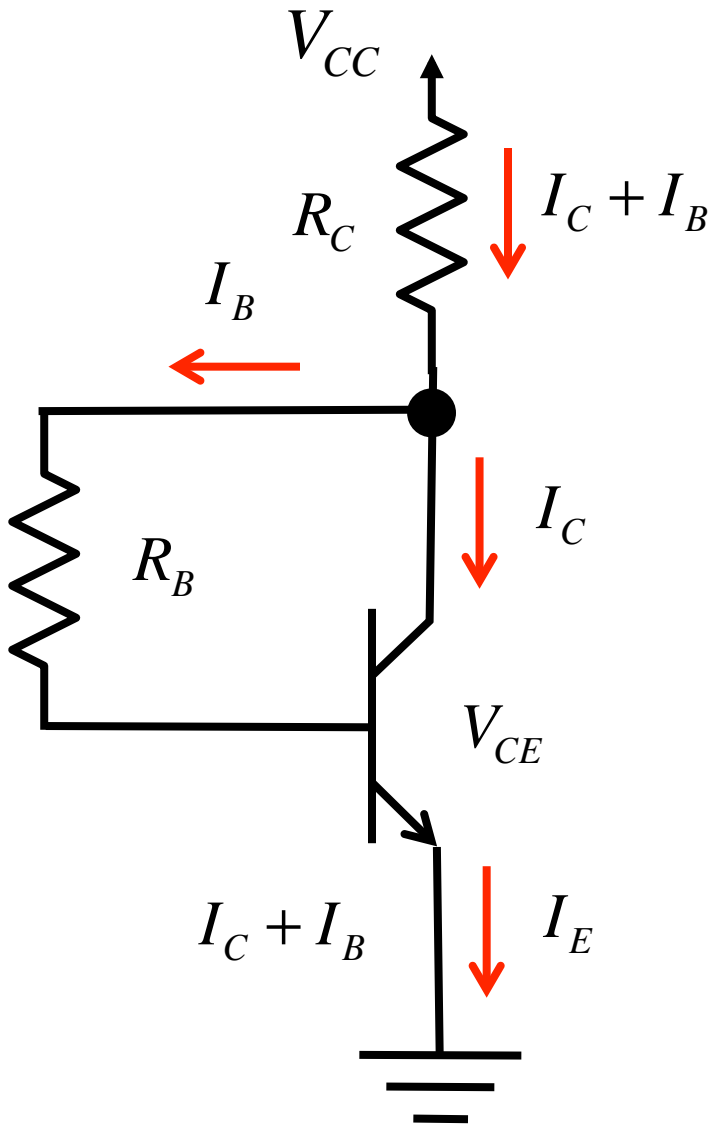
What if beta doubles?

$$I_C \rightarrow 2.0 \text{ mA}$$

$$V_C = 10 \text{ V} - I_C R_C = -4 \text{ V!}$$

**Saturation!**

## A better bias circuit



$$V_{CC} = R_C (I_C + I_C/\beta) I_C + R_B I_C/\beta + V_{BE}$$

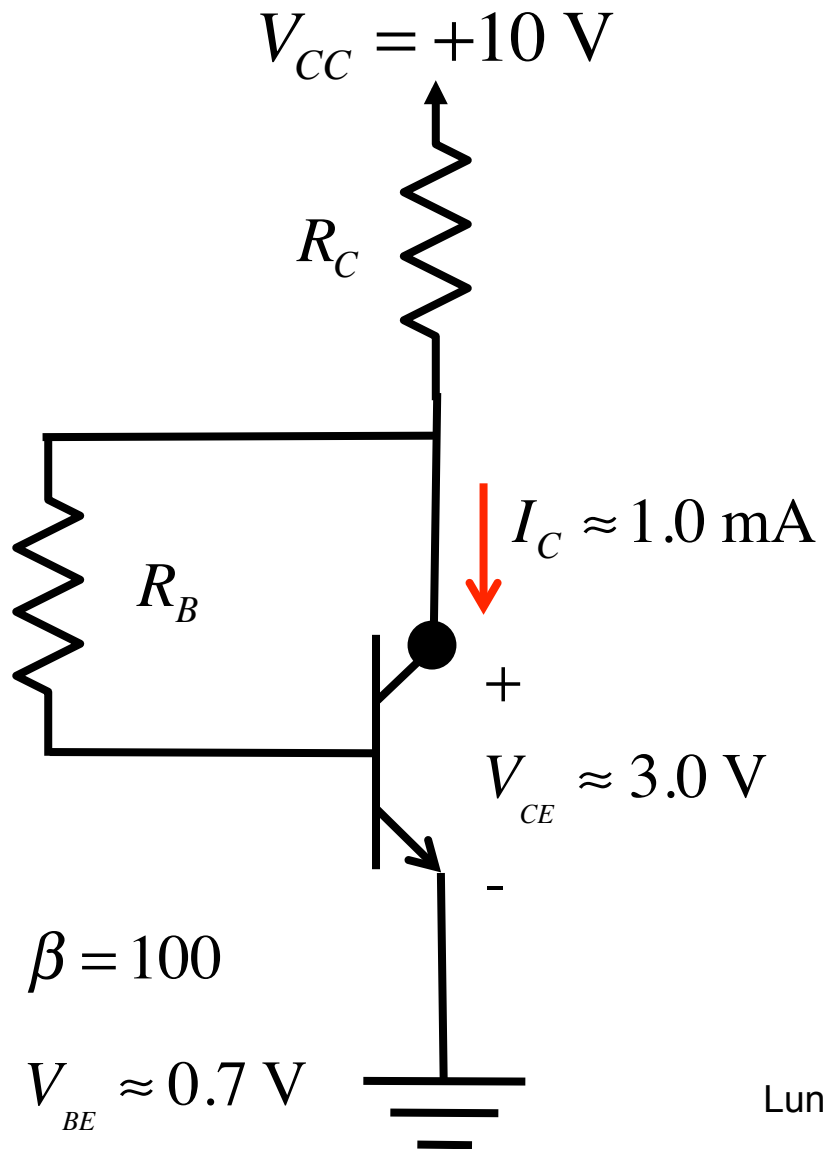
$$I_C = \frac{V_{CC} - V_{BE}}{R_C \left(1 + \frac{1}{\beta}\right) + R_B \frac{1}{\beta}}$$

$$\beta \rightarrow \infty$$

$$I_C \rightarrow \frac{V_{CC} - V_{BE}}{R_C}$$

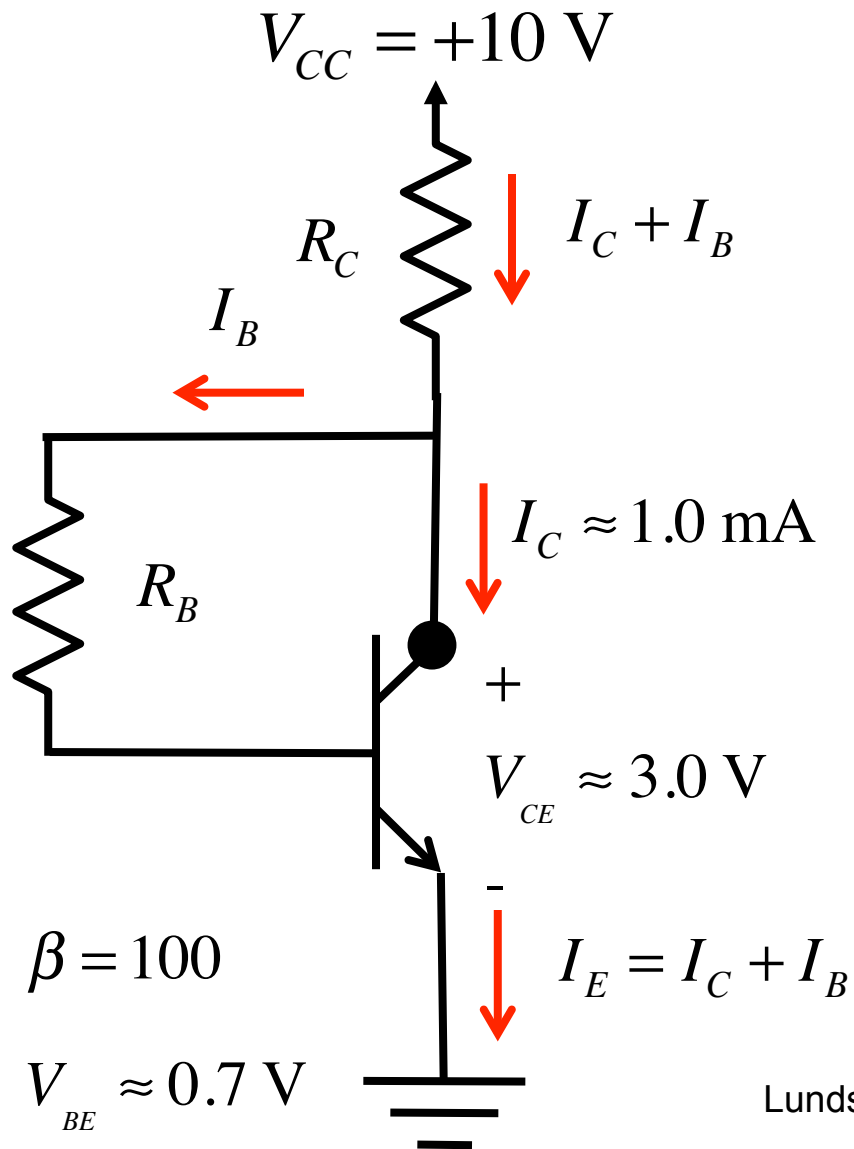
# Design

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## Design (Results)

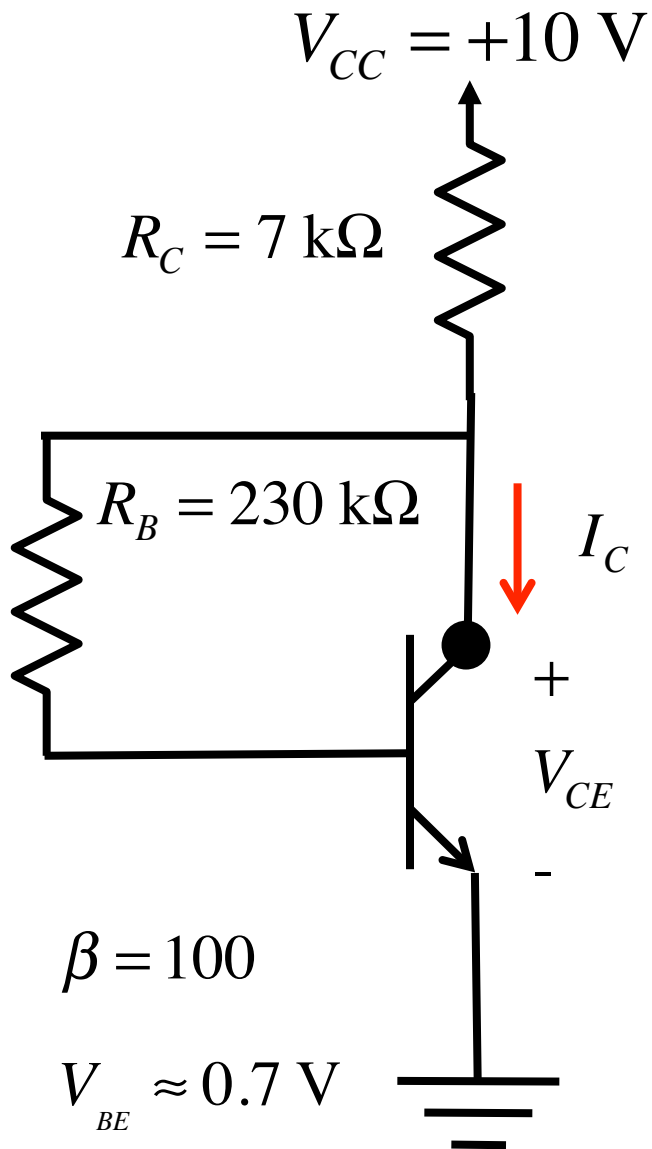


$$I_C R_C \approx 7 \text{ V} \quad R_C = 7 \text{ k}\Omega$$

$$I_B = 0.01 \text{ mA}$$

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{2.3}{0.01} = 230 \text{ k}\Omega$$

# Analysis



$$I_C = \frac{V_{CC} - V_{BE}}{R_C \left(1 + \frac{1}{\beta}\right) + R_B \frac{1}{\beta}}$$

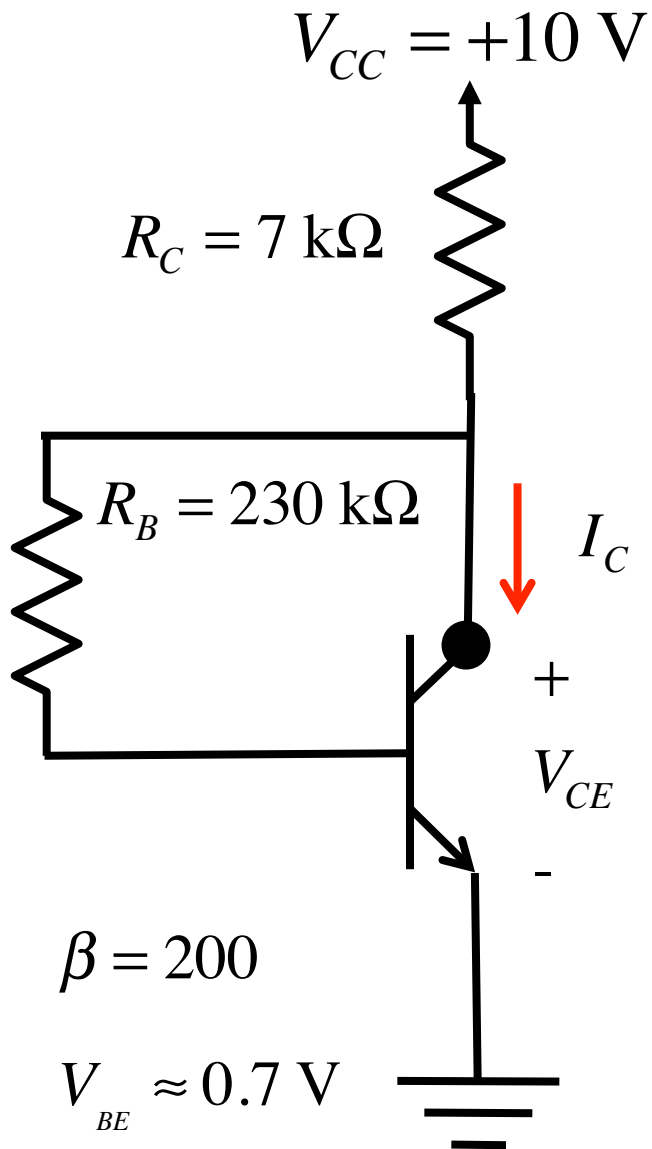
$$I_C = \frac{10 - 0.7}{7 \left(1 + \frac{1}{100}\right) + \frac{230}{100}}$$

$$I_C = 1.0 \text{ mA}$$

$$V_{CE} = V_{CC} - \left(\frac{\beta + 1}{\beta}\right) I_C R_C$$

$$V_{CE} = 2.9 \text{ V} \quad (\text{close})$$

## Analysis for beta = 200



$$I_C = \frac{V_{CC} - V_{BE}}{R_C \left(1 + \frac{1}{\beta}\right) + R_B \frac{1}{\beta}}$$

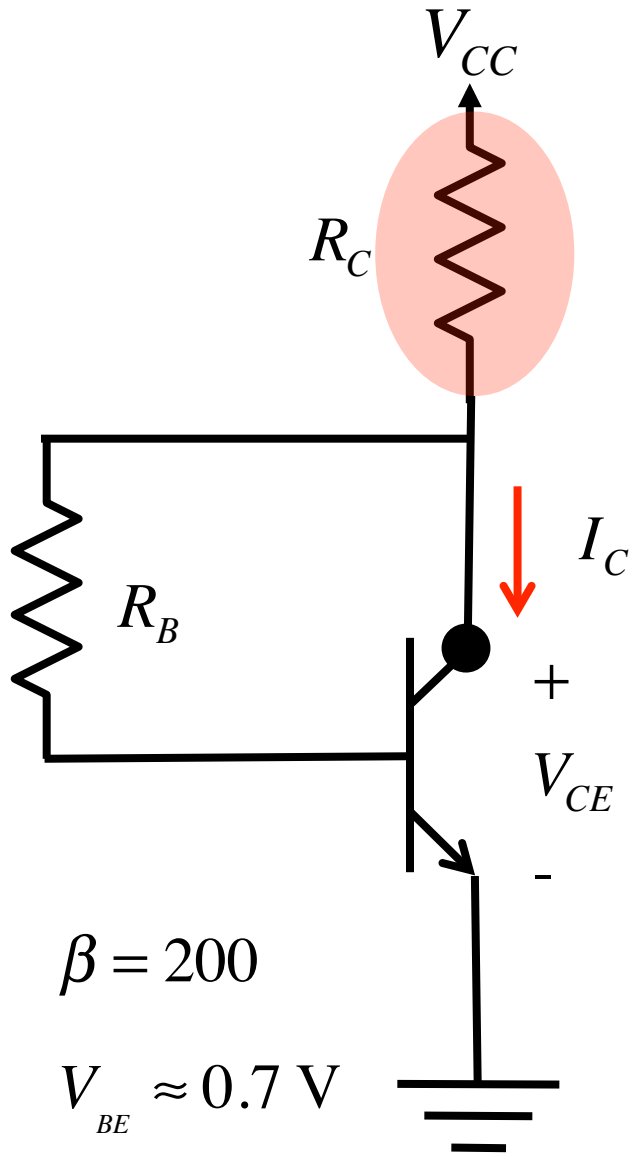
$$I_C = 1.1 \text{ mA}$$

$$(I_C = 1.0 \text{ mA})$$

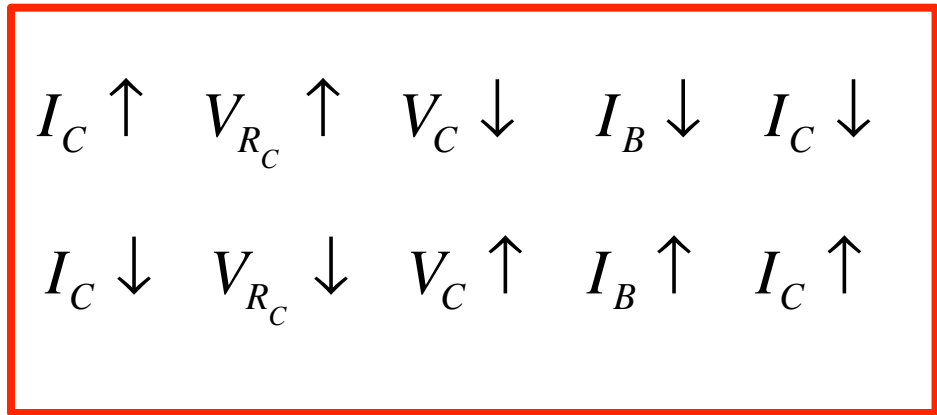
$$V_{CE} = 2.3 \text{ V}$$

$$(V_{CE} = 2.9 \text{ V})$$

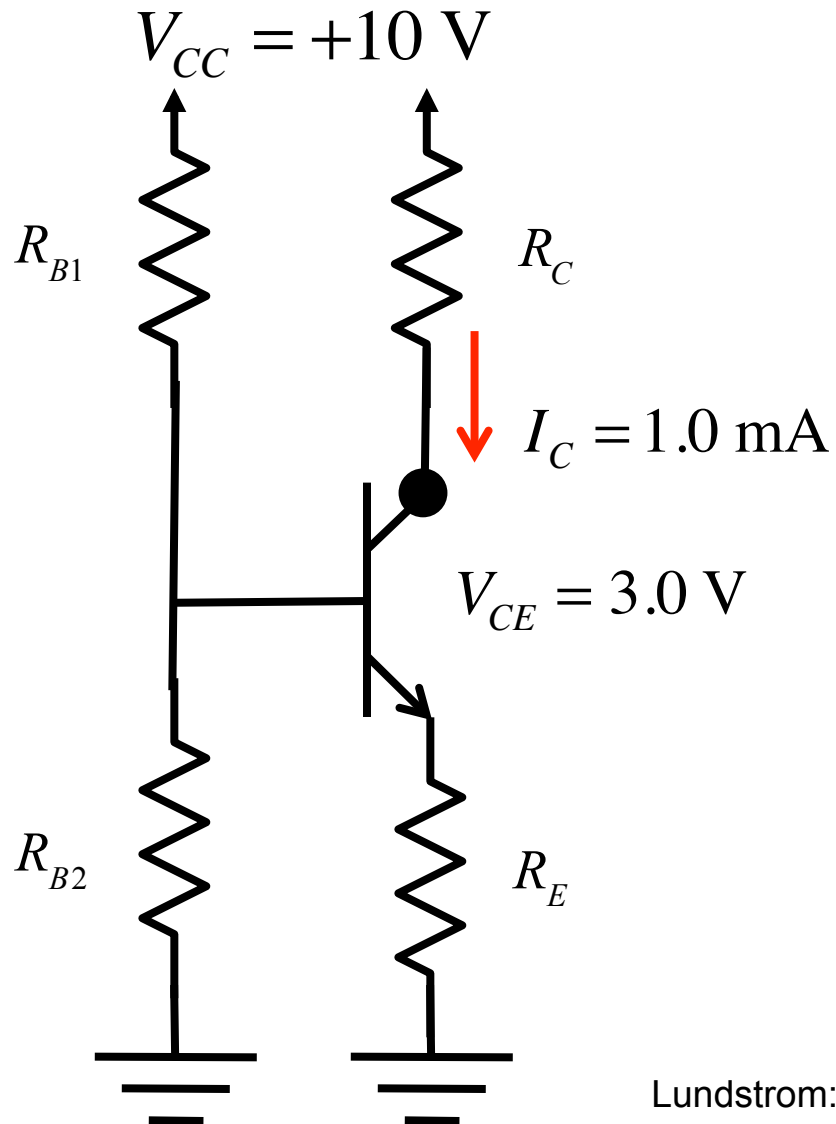
# Why does it work?



Negative feedback



# Classic 4-resistor Bias circuit design



Design for

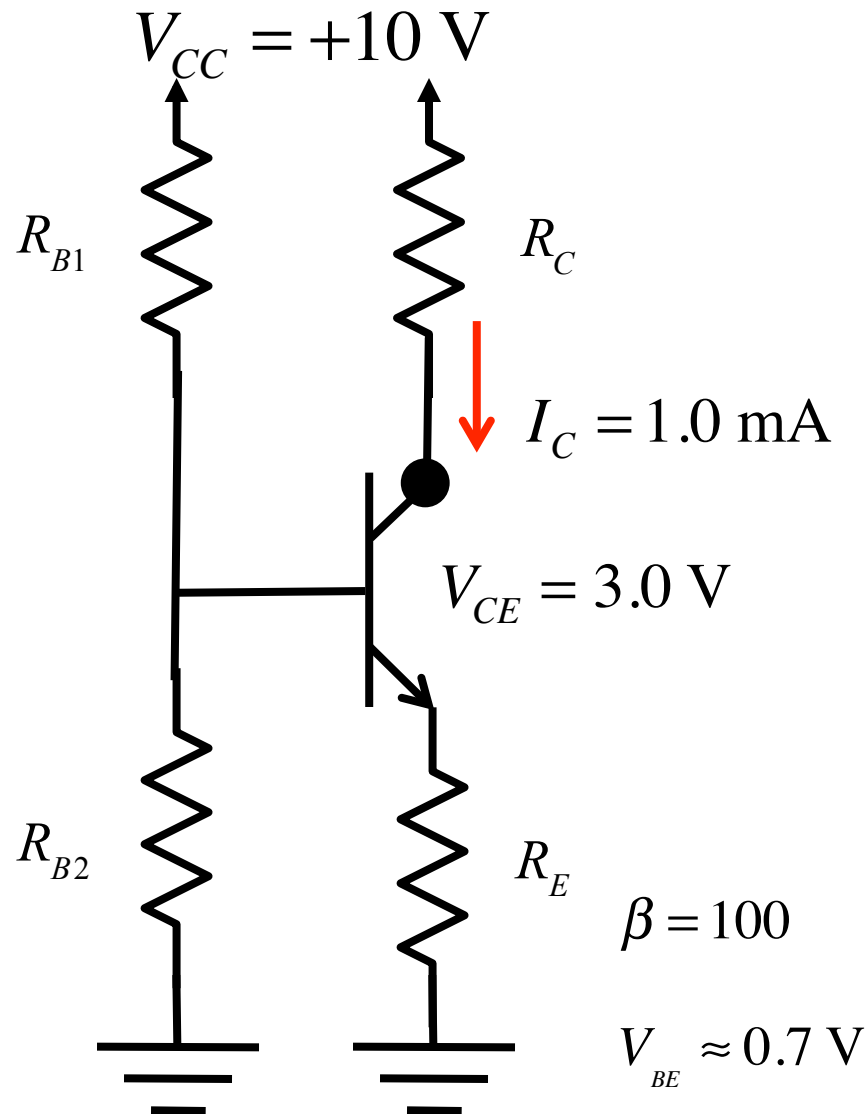
$$V_{CE} = 3.0\text{ V}$$

$$I_C = 1.0\text{ mA}$$

$$\beta = 100$$

$$V_{BE} \approx 0.7\text{ V}$$

# Classic Bias circuit design



**Start at the output:**

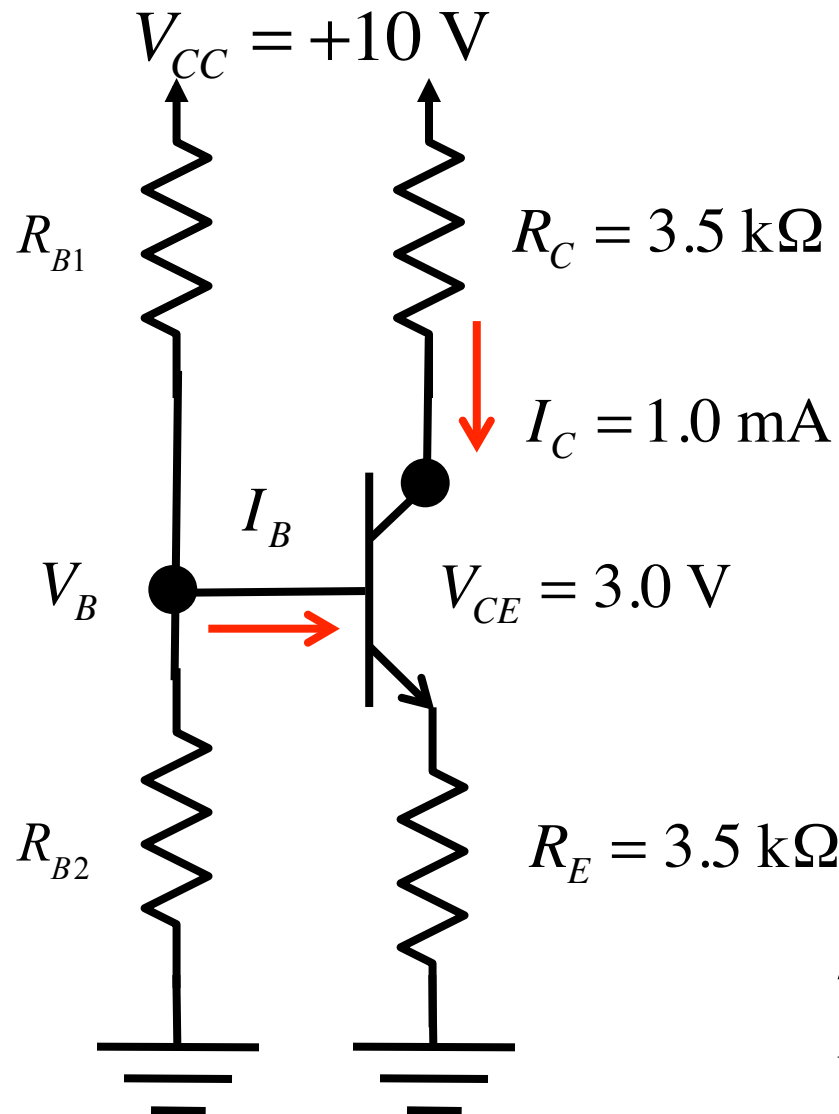
Have 7 V to split between 2 resistors.

Let:  $V_{R_C} = V_{R_E} = 3.5\text{ V}$

$$R_C = \frac{3.5\text{ V}}{1.0\text{ mA}} = 3.5\text{ k}\Omega$$

$$R_E = \frac{3.5\text{ V}}{1.01\text{ mA}} \approx 3.5\text{ k}\Omega$$

# Classic Bias circuit design



**Now move to the input:**

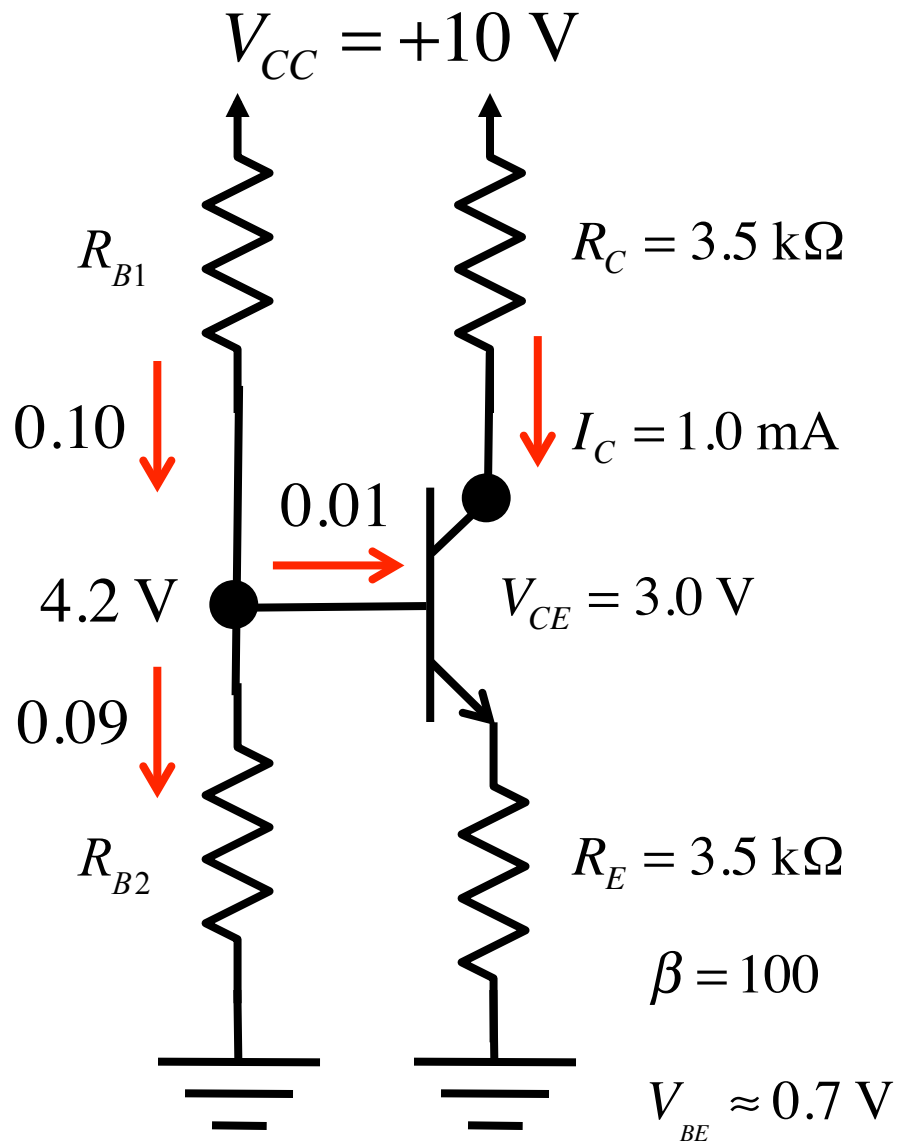
$$\begin{aligned} V_B &= V_{R_E} + 0.7 \\ &= 3.5 + 0.7 = 4.2\text{ V} \end{aligned}$$

$$I_B = \frac{I_C}{100} = 0.01\text{ mA}$$

$$\beta = 100$$

$$V_{BE} \approx 0.7\text{ V}$$

## Classic Bias circuit design



**Choose:**

$$I_{R_{B1}} = 10I_B = 0.1 \text{ mA}$$

$$I_{R_{B1}} = 0.1 \text{ mA} = \frac{(10 - 4.2) \text{ V}}{R_{B1}} \rightarrow 58 \text{ k}\Omega$$

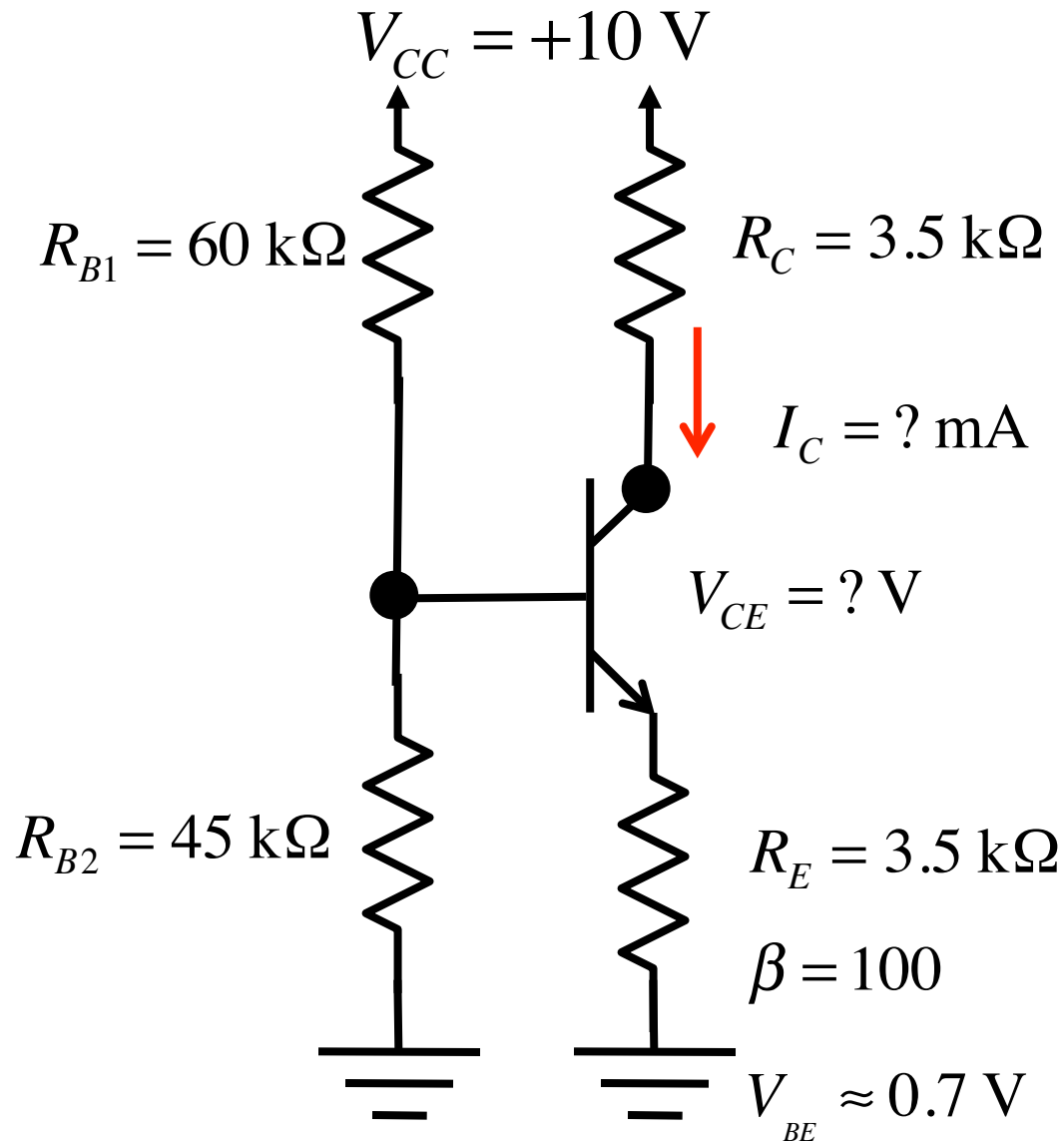
$$I_{R_{B2}} = I_{R_{B1}} - I_B$$

$$= 10I_B - I_B = 0.09 \text{ mA}$$

$$I_{R_{B2}} = 0.09 \text{ mA} = \frac{4.2 \text{ V}}{R_{B2}} \rightarrow 46.7 \text{ k}\Omega$$

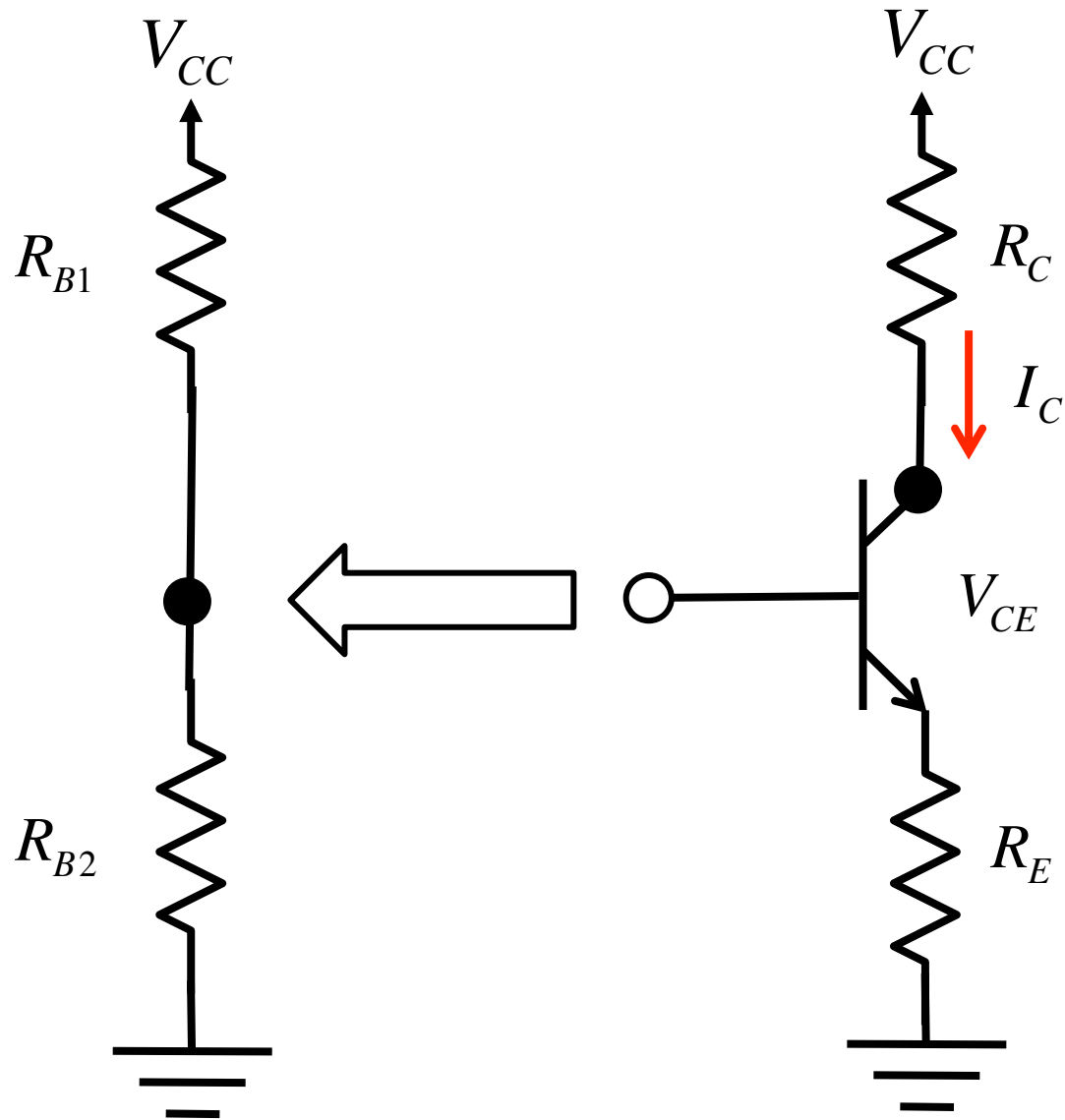


## Classic bias circuit analysis



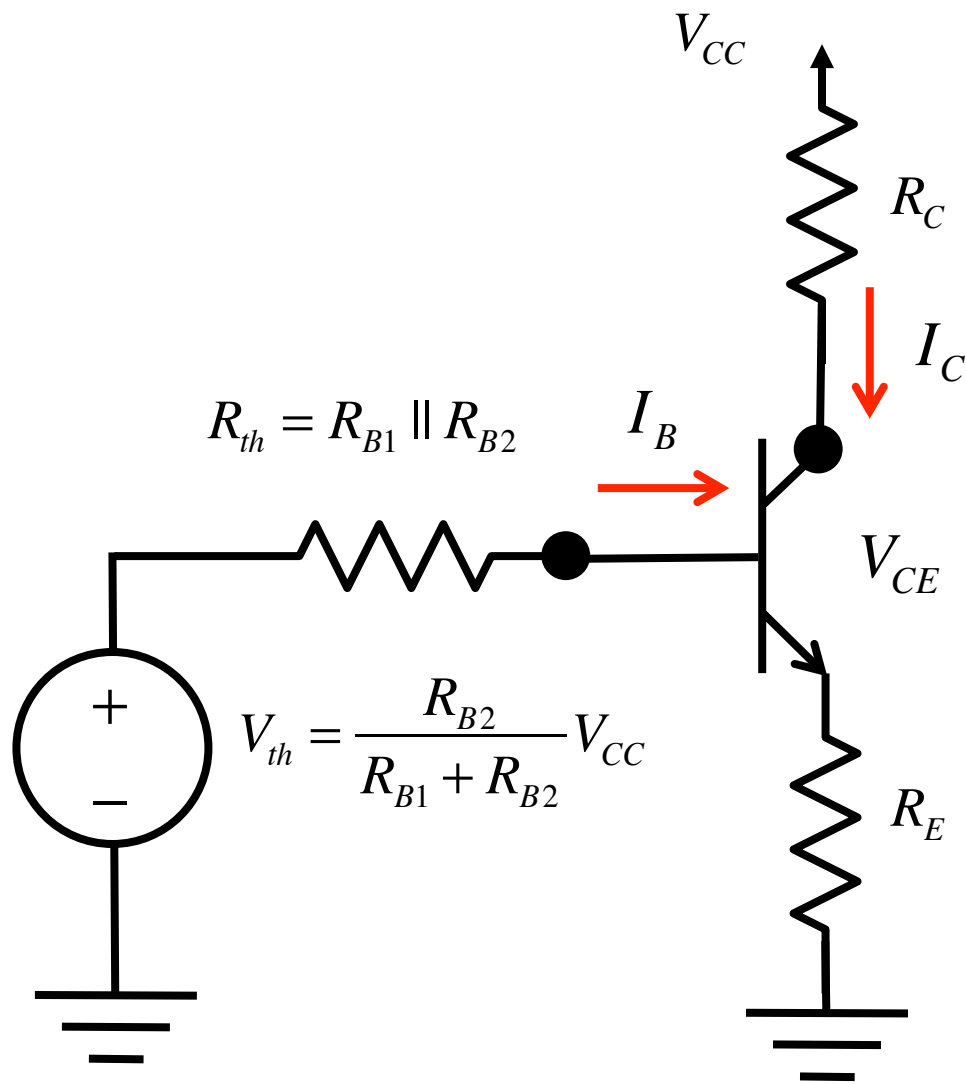
Now that everything is specified, we can **analyze** the circuit.

# Classic Bias circuit analysis

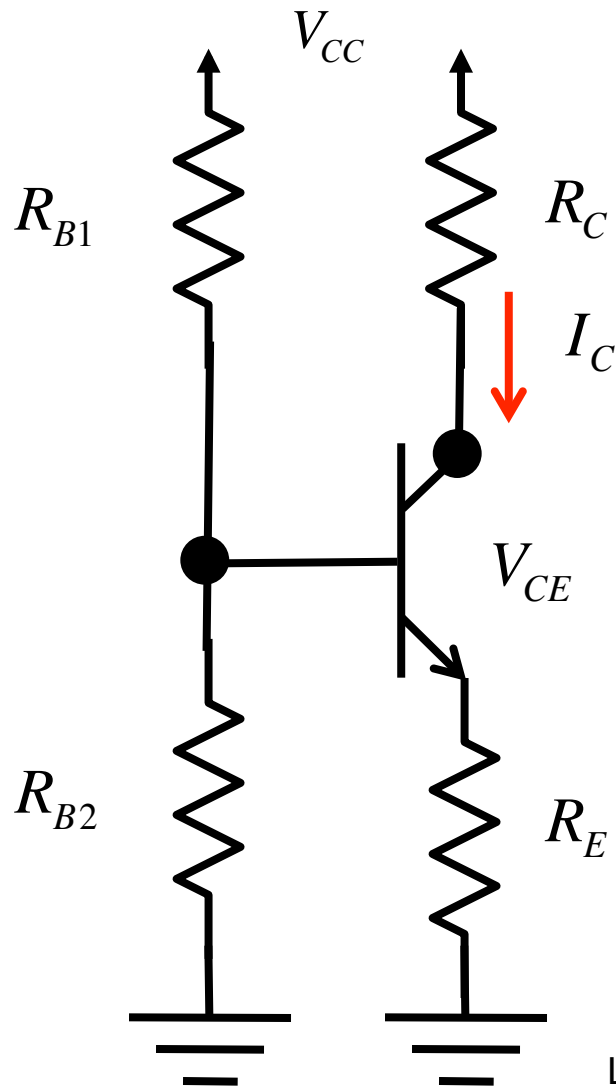


# Classic Bias circuit analysis

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# Classic bias circuit design

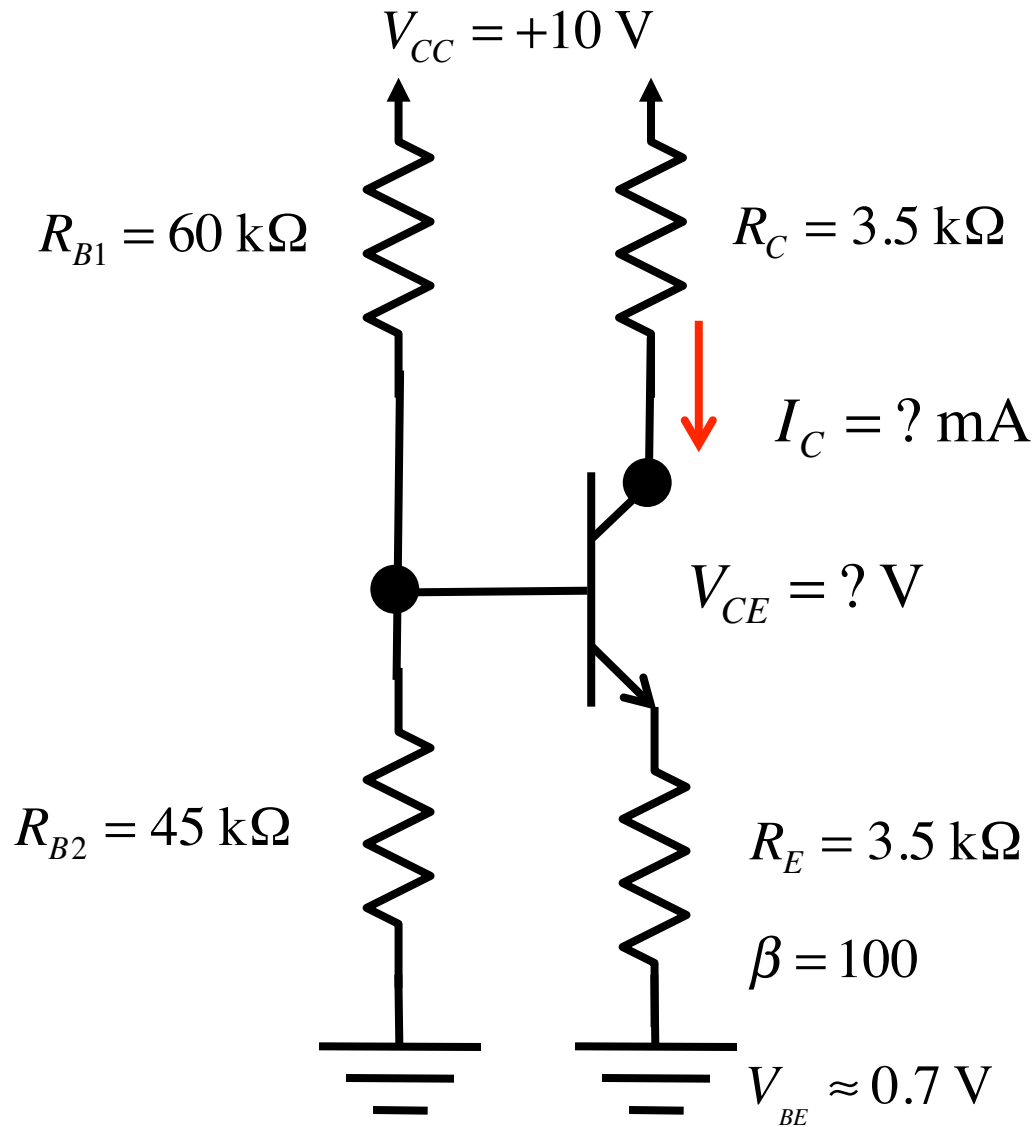


$$I_C = \beta \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1)R_E}$$

$$R_{th} = R_{B1} \parallel R_{B2}$$

$$V_{th} = V_{CC} \frac{R_{B2}}{R_{B1} + R_{B2}}$$

# Classic bias circuit analysis

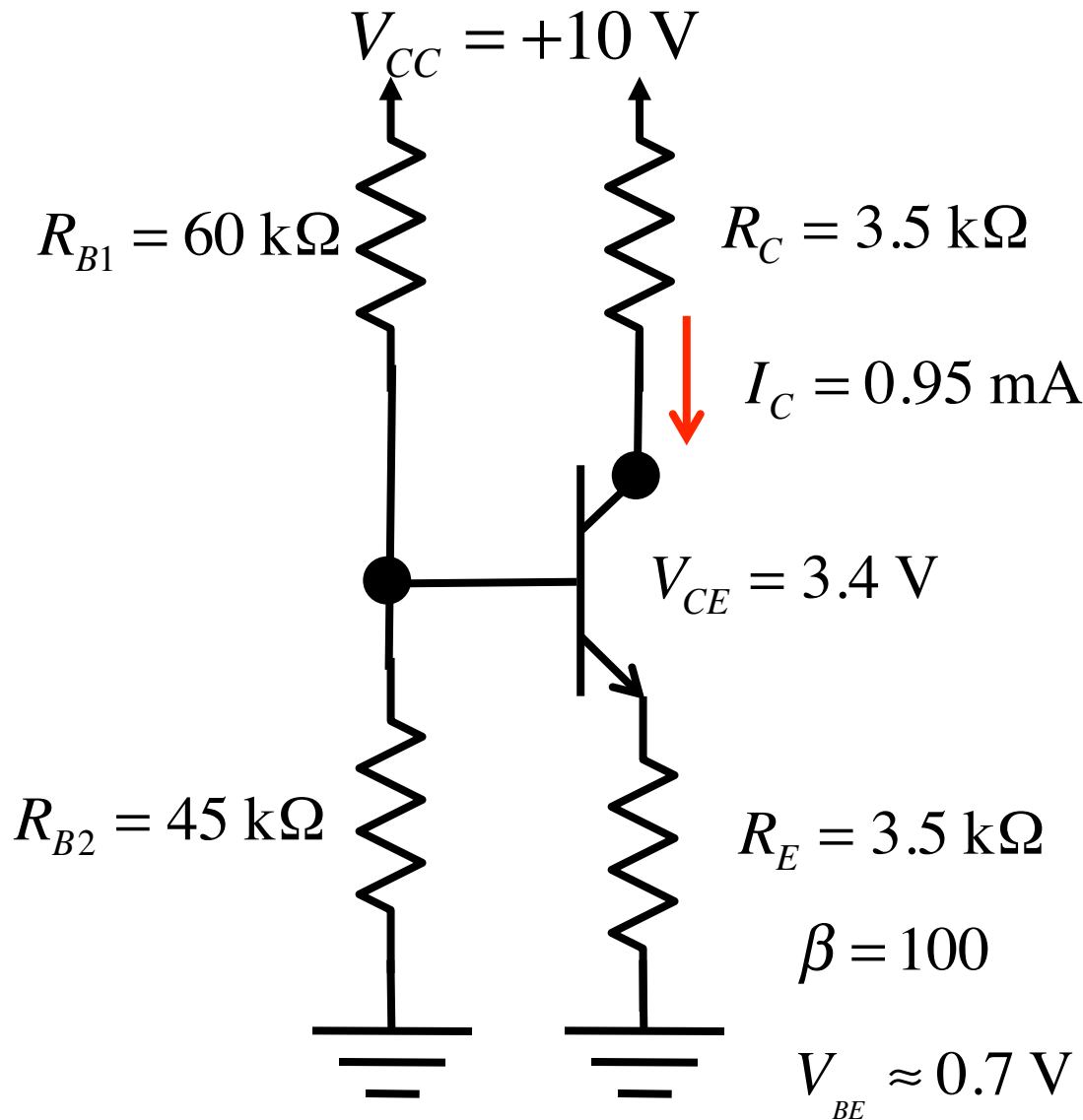


$$I_C = \beta \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1)R_E}$$

$$I_C = 0.95 \text{ mA}$$

$$V_{CE} = 3.4 \text{ V}$$

# Classic Bias circuit design

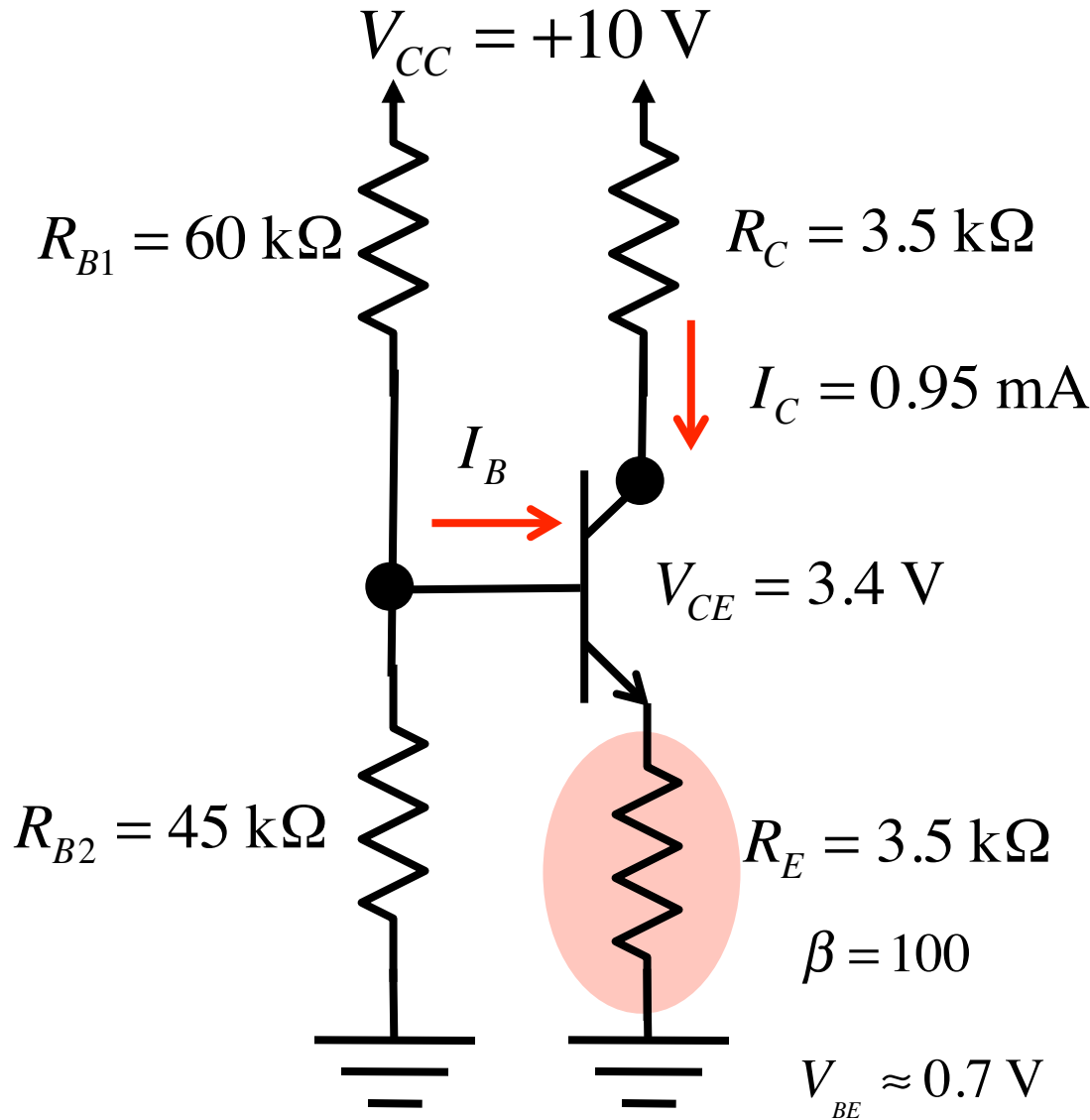


**What if beta doubles?**

$$I_C = 0.95 \text{ mA}$$
$$\rightarrow 1.02 \text{ mA}$$

**Why is the circuit so good?**

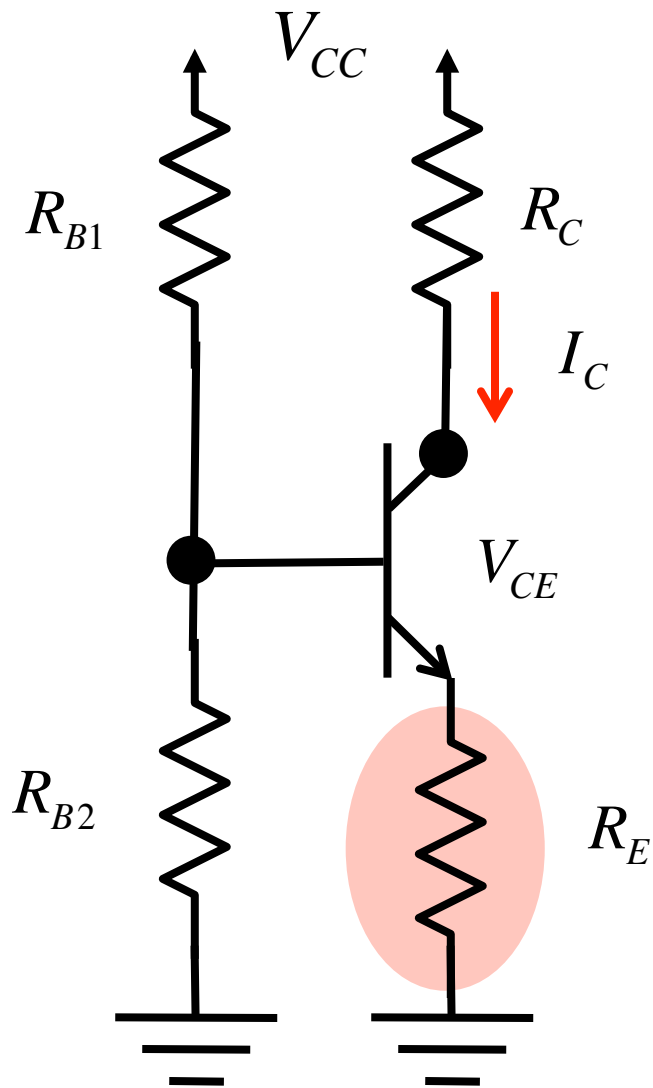
# Negative feedback



$I_C \uparrow$	$V_{R_E} \uparrow$	$I_B \downarrow$	$I_C \downarrow$
$I_C \downarrow$	$V_{R_E} \downarrow$	$I_B \uparrow$	$I_C \uparrow$

## From the equations

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$$I_C = \beta \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1)R_E}$$

$$(\beta + 1)R_E \gg R_{th}$$

$$I_C \approx \frac{\beta}{(\beta + 1)} \frac{V_{th} - V_{BE}}{R_E}$$

$$I_C \approx \frac{V_{th} - V_{BE}}{R_E}$$



# Summary

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Be comfortable analyzing NPN, PNP, and NPN-PNP DC circuits.

The classic 4-resistor bias circuit for discrete transistors makes use of negative feedback to deal with variations in beta.

For IC design, we don't use the 4-resistor bias circuit because high value resistors are "expensive". Instead, we make use of transistors, because they are cheap.

# BJT bias circuits

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- 1) NPN and PNP circuits
- 2) Bias circuits (discrete)

