Spring 2019 Purdue University

ECE 255: L16

Biasing MOSFETs and BJTs

(Sedra and Smith, 7th Ed., Sec. 7.4)

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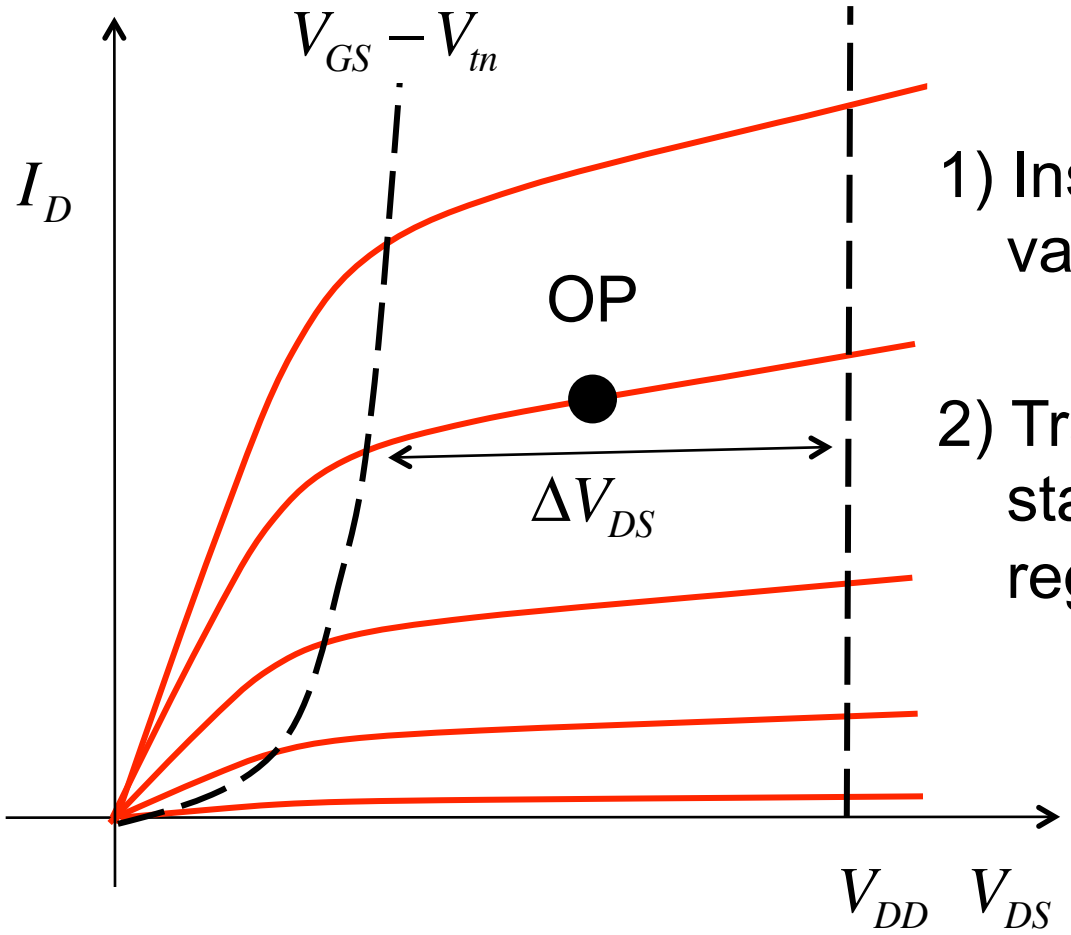
Outline

1) Bias circuit design
2) BJT bias circuits
3) Load line analysis
4) MOSFET bias circuits
5) Load line analysis

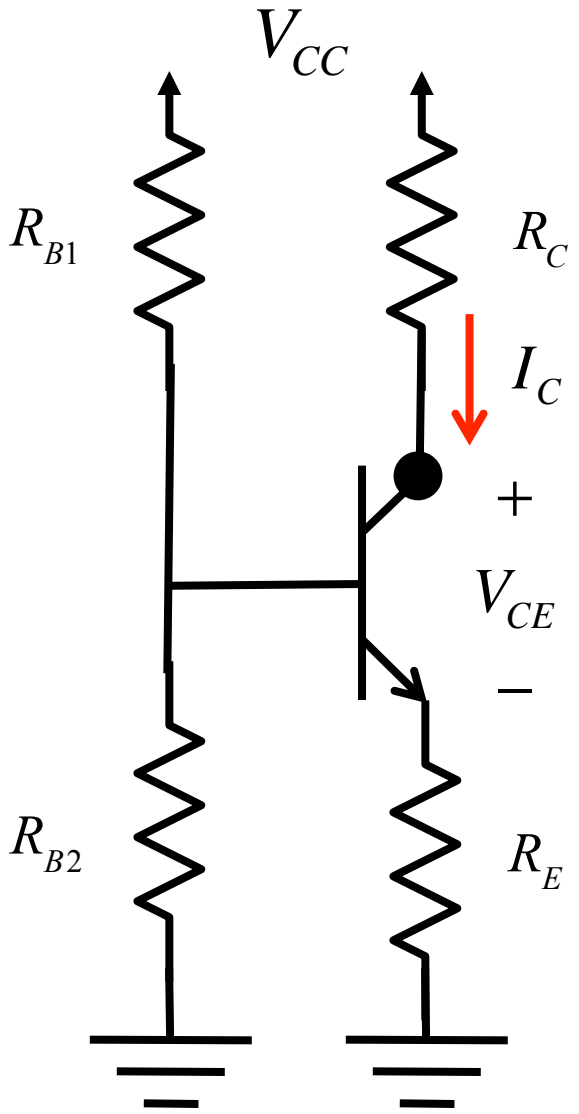
Operating point and bias circuit design



1) Insensitive to device variations (e.g. beta, V_t)

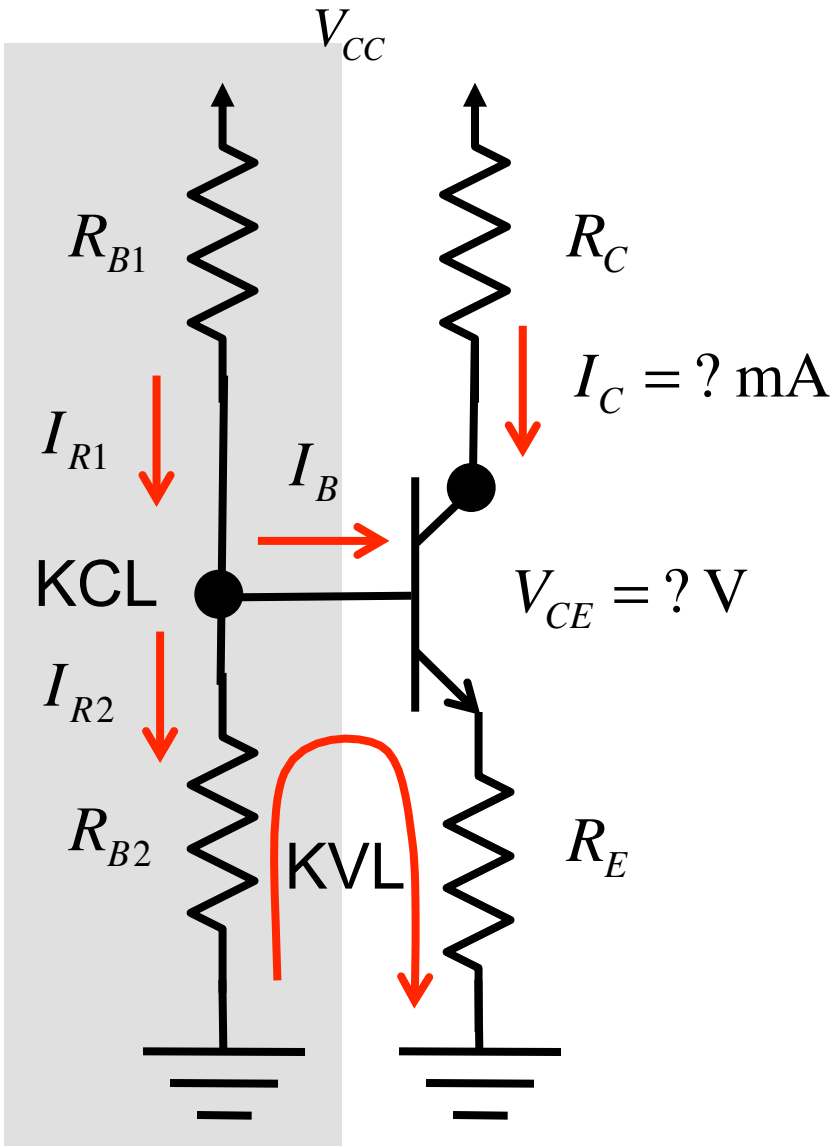
2) Transistor should stay in the active region.

Classic 4-resistor Bias circuit

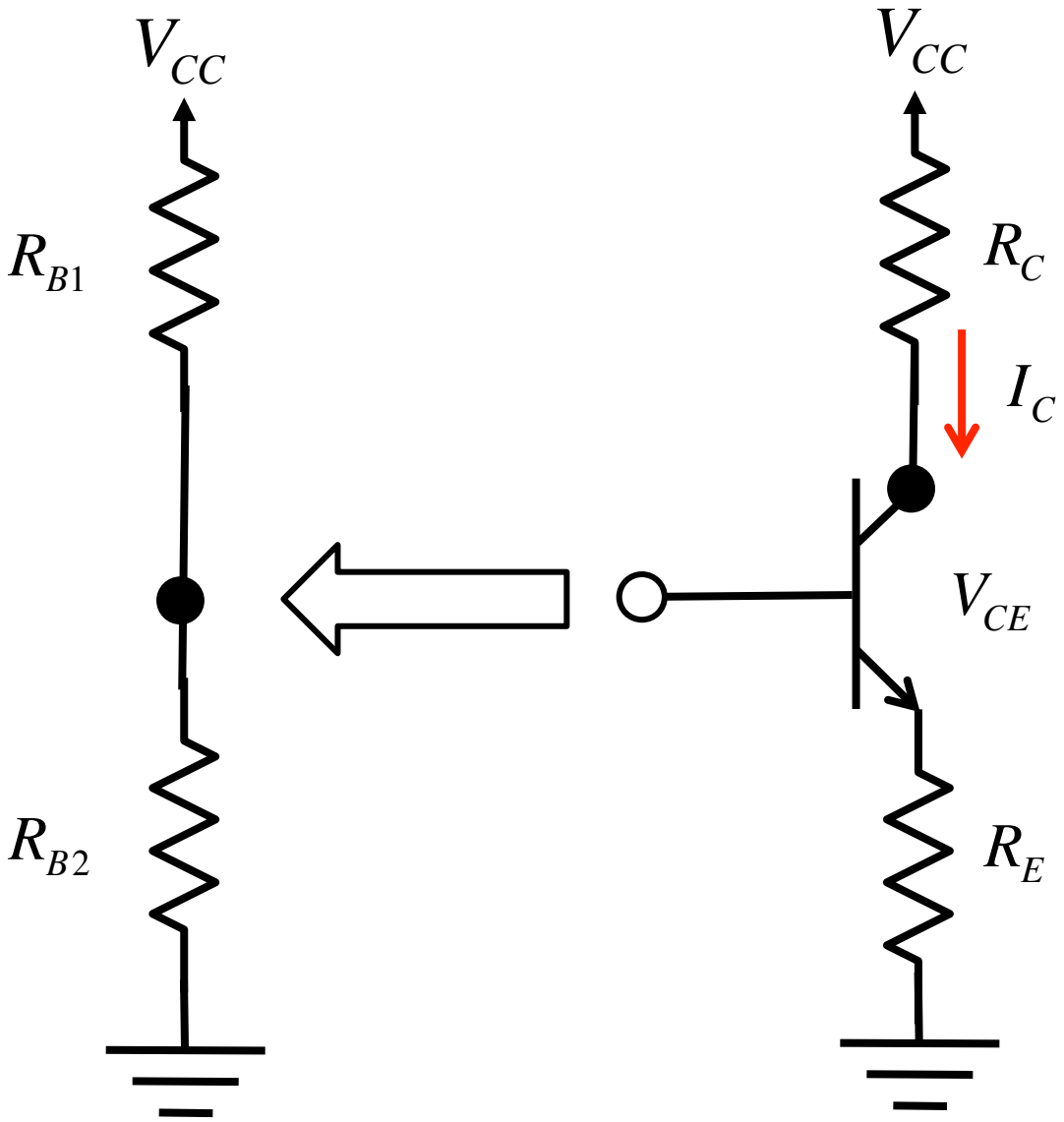


Suitable for
discrete transistors.

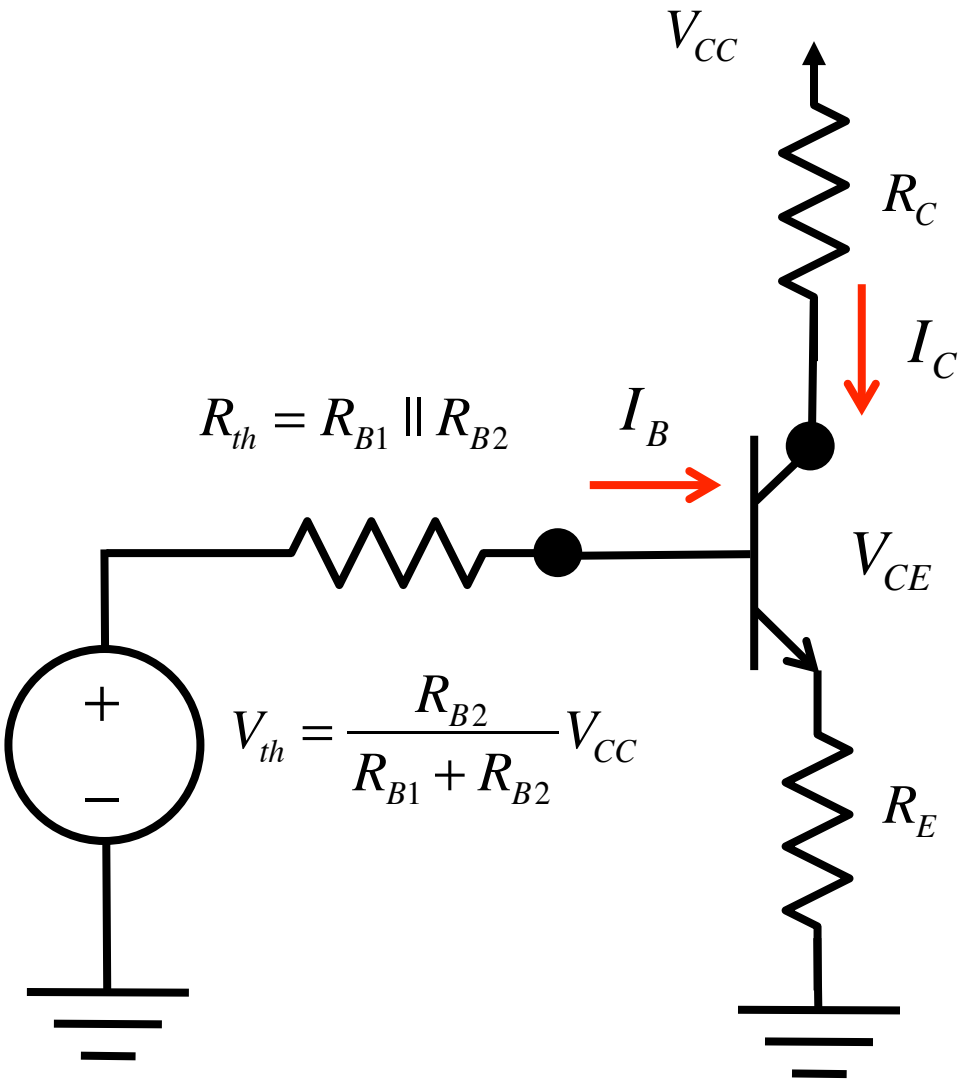
Classic bias circuit **analysis**



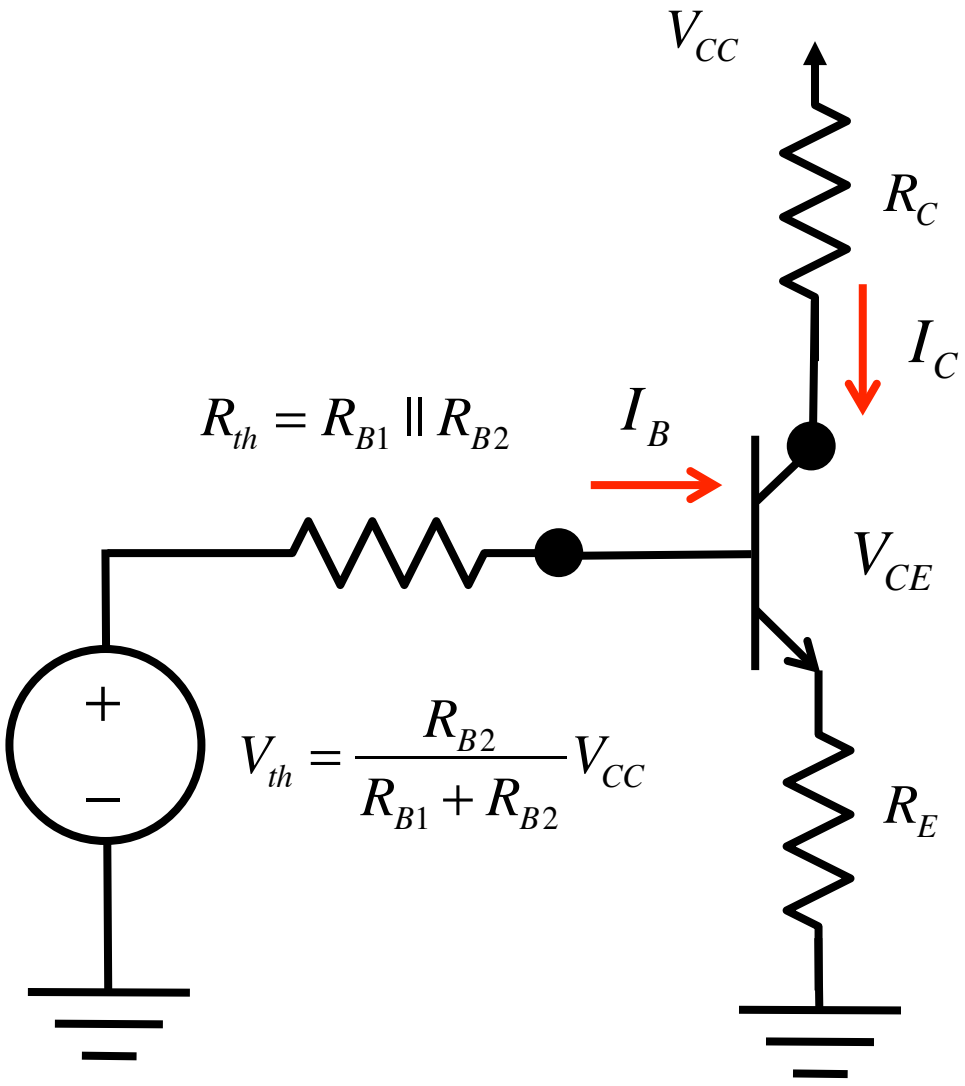
Classic Bias circuit analysis



Classic Bias circuit analysis



Classic Bias circuit analysis



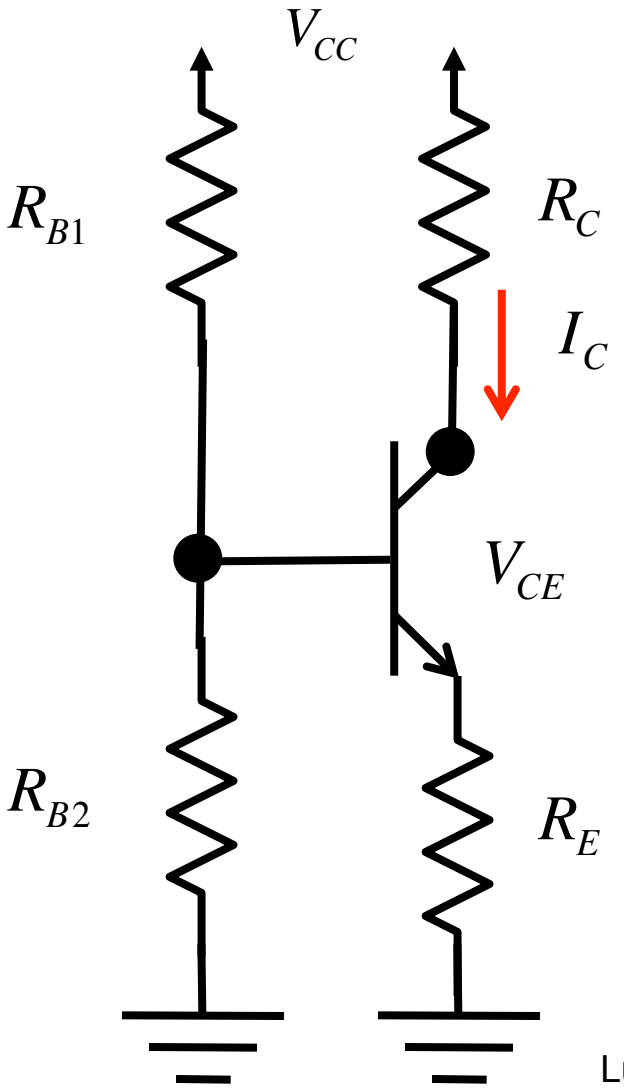
$$V_{th} = I_B R_{th} + V_{BE} + \left(I_B + I_C\right) R_E$$

$$V_{th} = I_B R_{th} + V_{BE} + \left(\beta + 1\right) I_B R_E$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + \left(\beta + 1\right) R_E}$$

$$I_C = \frac{\beta\left(V_{th} - V_{BE}\right)}{R_{th} + \left(\beta + 1\right) R_E}$$

Classic bias circuit analysis

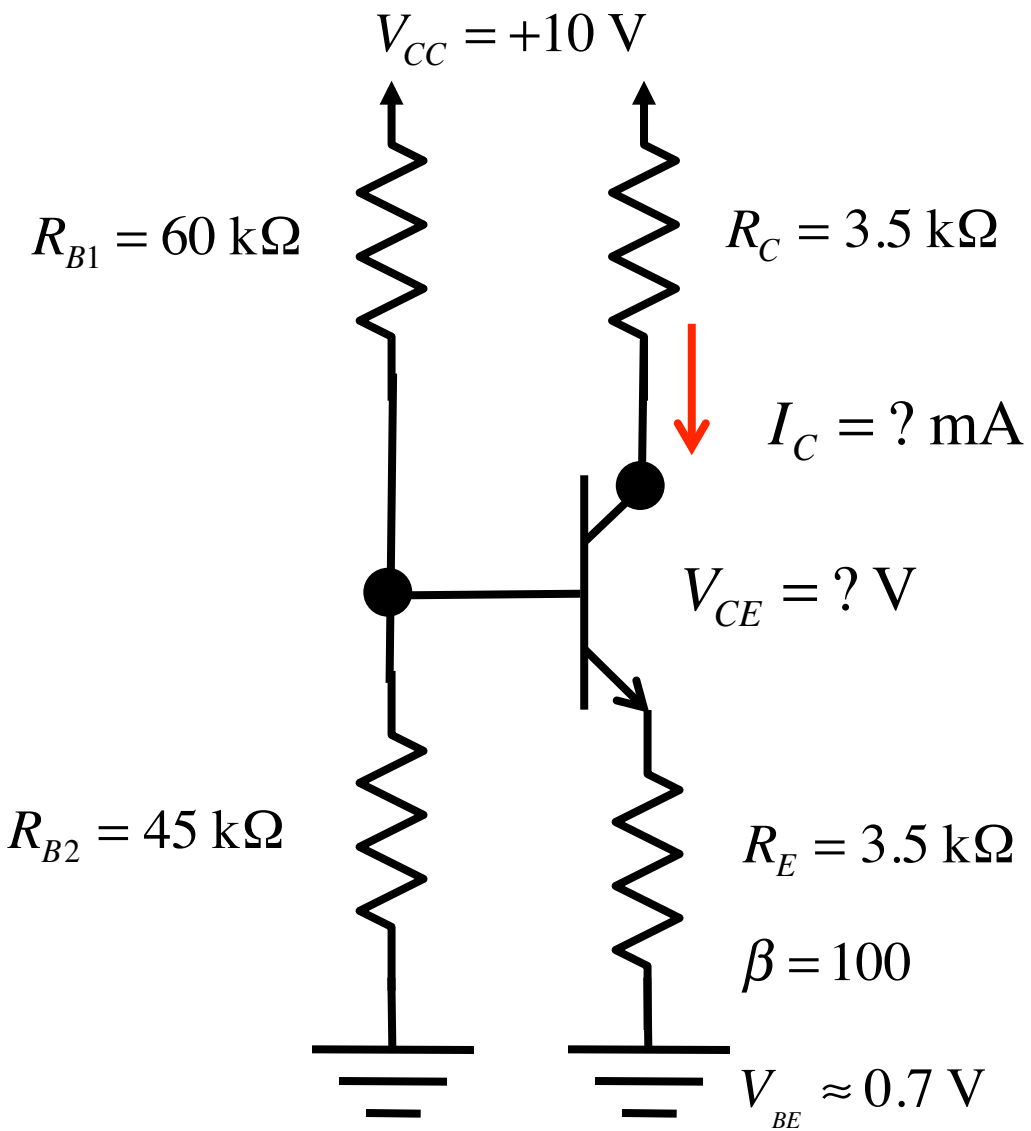


$$I_C = \beta \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$

$$R_{th} = R_{B1} \parallel R_{B2}$$

$$V_{th} = V_{CC} \frac{R_{B2}}{R_{B1} + R_{B2}}$$

Classic bias circuit **analysis**



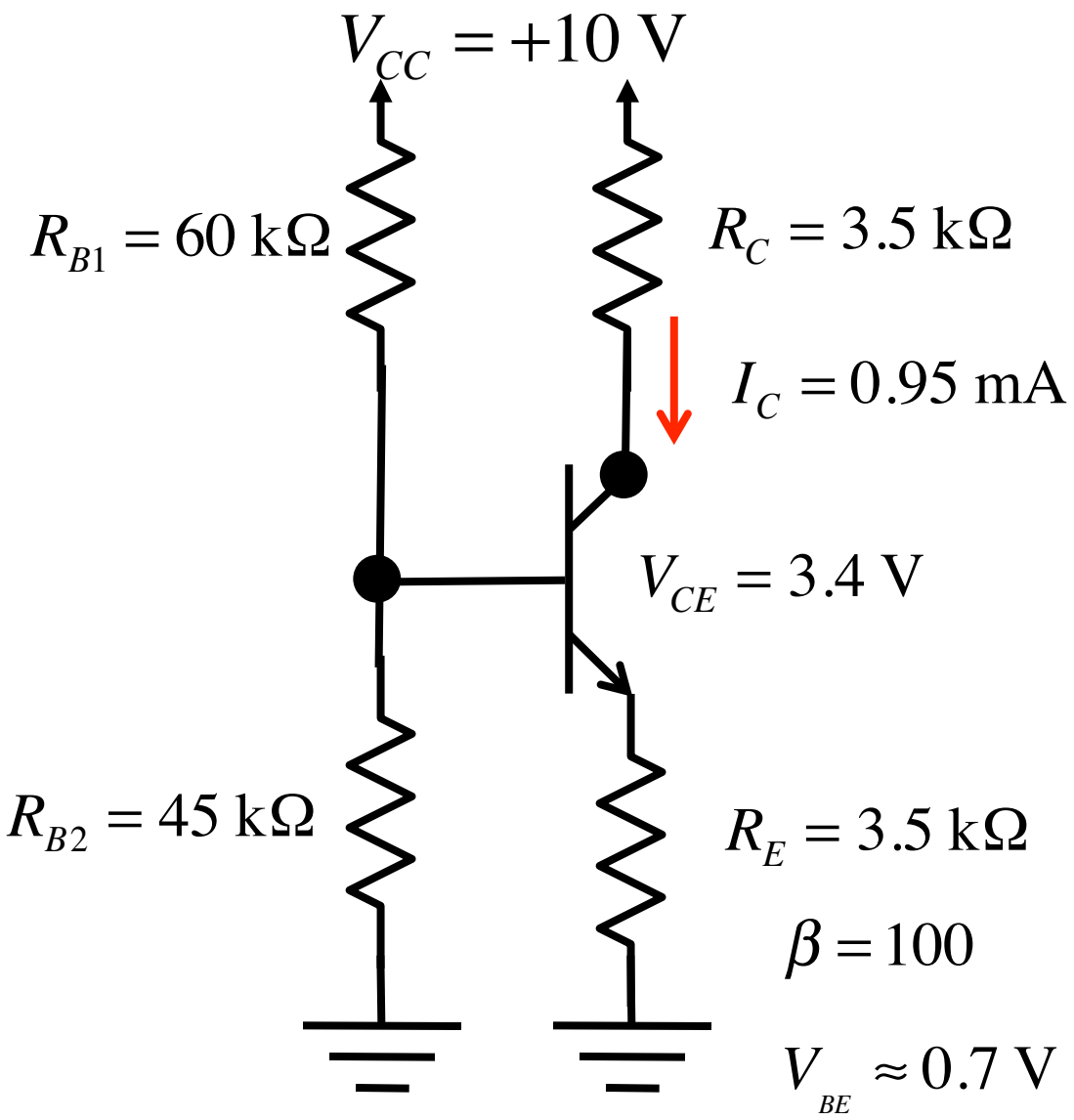
$$I_C = \beta \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$

$$V_{CE} = V_{CC} - I_C R_C - \frac{I_C}{\alpha} R_E$$

$$I_C = 0.95 \text{ mA}$$

$$V_{CE} = 3.4 \text{ V}$$

Sensitivity to beta



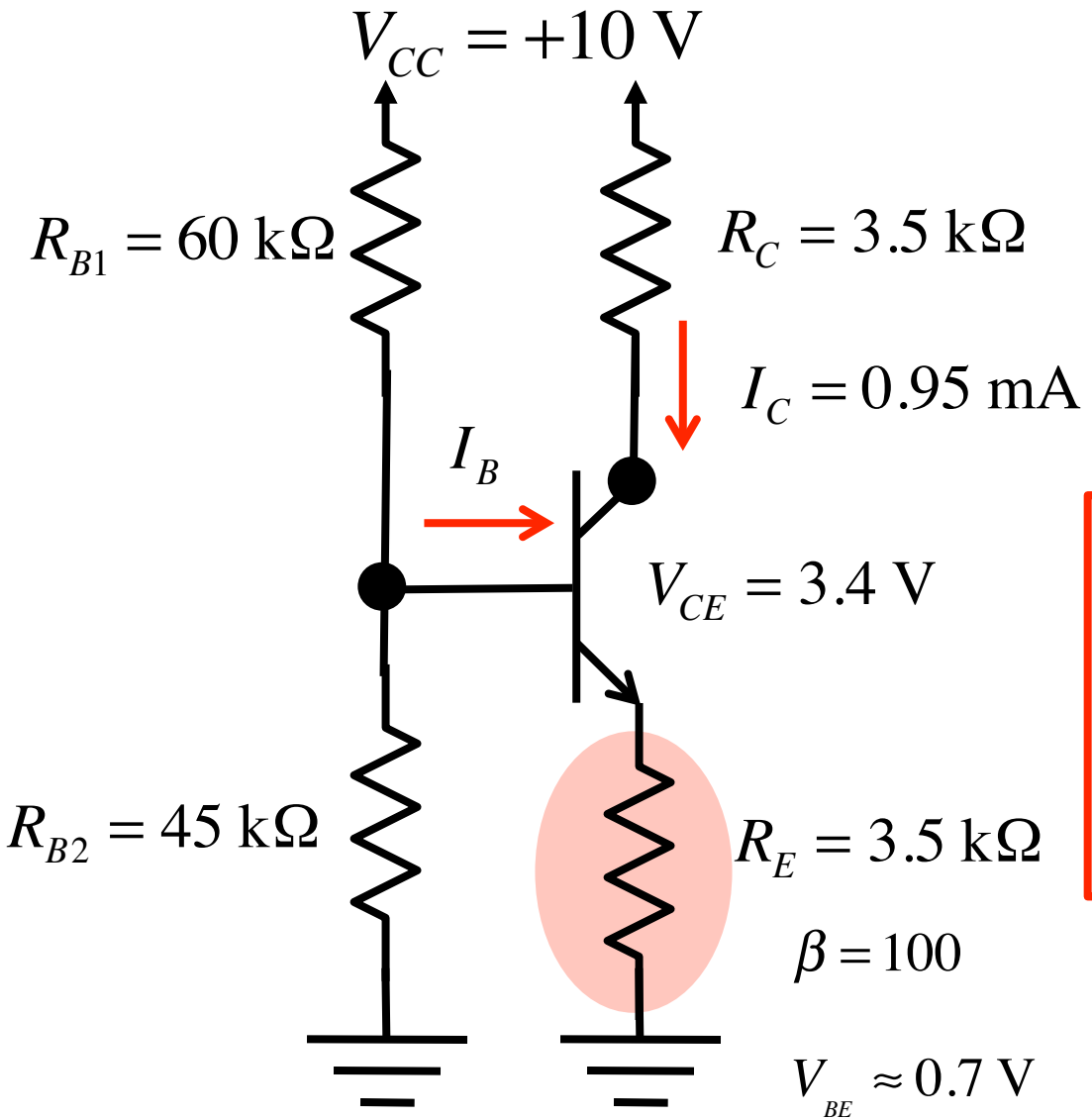
What if beta doubles?

$I_C = 0.95$ mA

$\rightarrow 1.02$ mA

Why is the circuit so good?

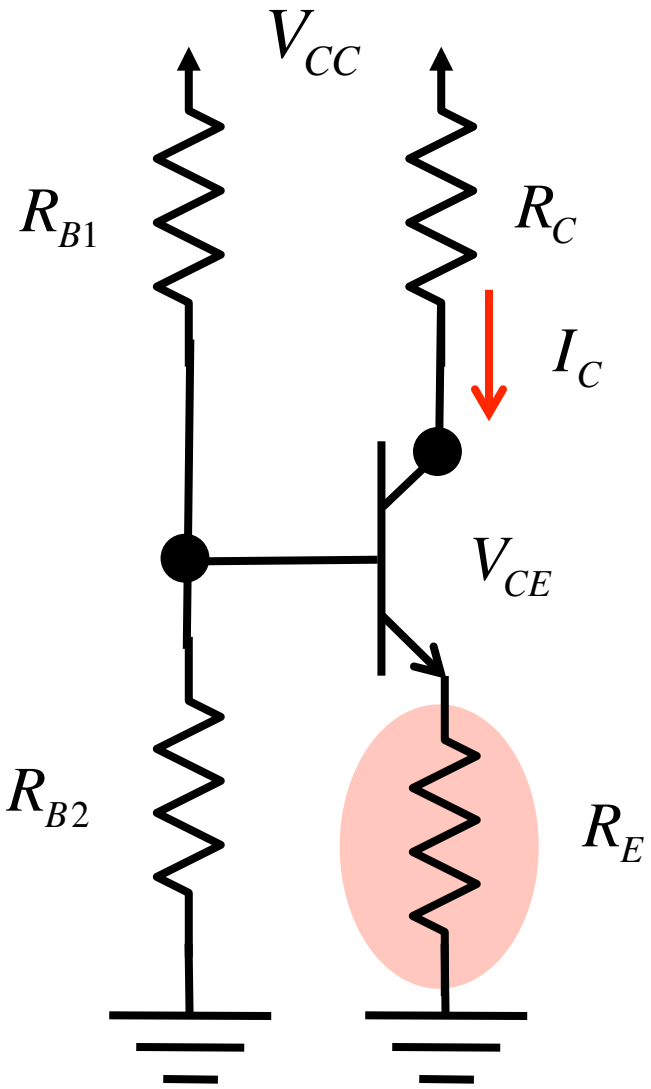
Negative feedback



$I_C \uparrow \quad V_{R_E} \uparrow \quad I_B \downarrow \quad I_C \downarrow$

$I_C \downarrow \quad V_{R_E} \downarrow \quad I_B \uparrow \quad I_C \uparrow$

From the equations



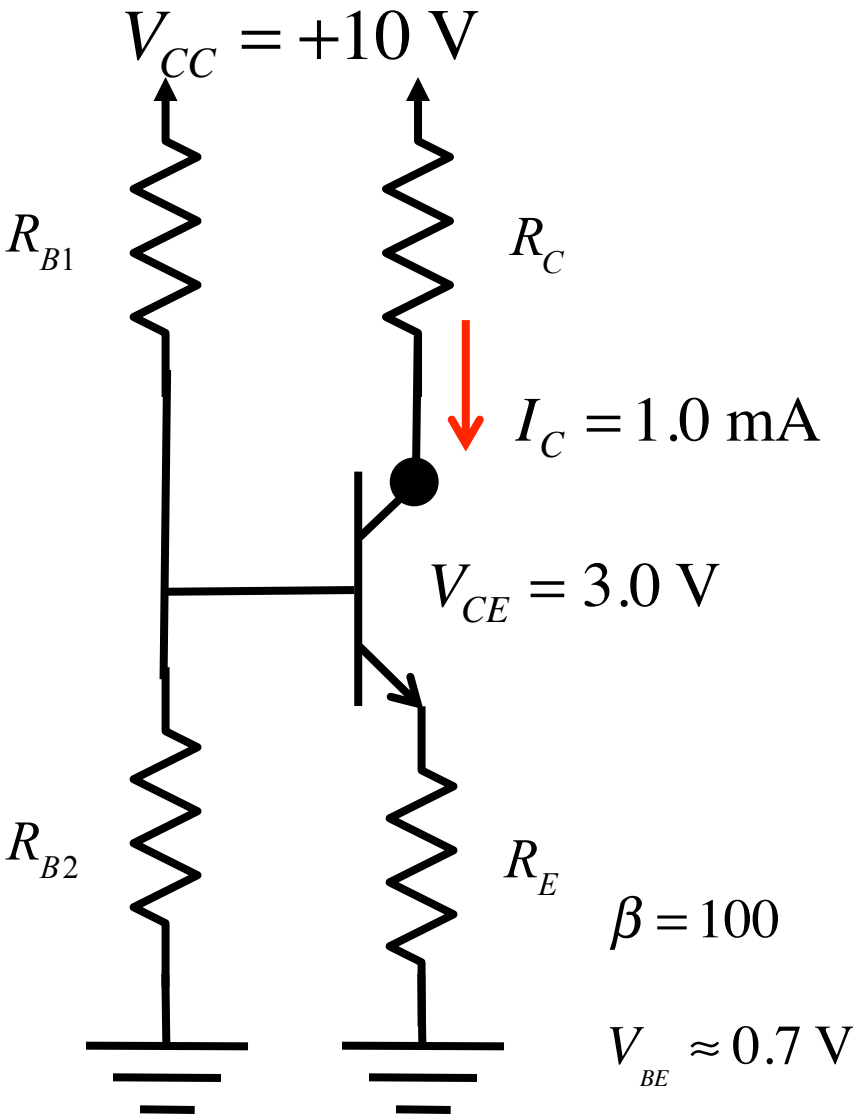
$$I_C = \beta \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$

$$(\beta + 1) R_E >> R_{th}$$

$$I_C \approx \frac{\beta}{(\beta + 1)} \frac{V_{th} - V_{BE}}{R_E}$$

$$I_C \approx \frac{V_{th} - V_{BE}}{R_E}$$

Classic Bias circuit **design**



Start at the output:

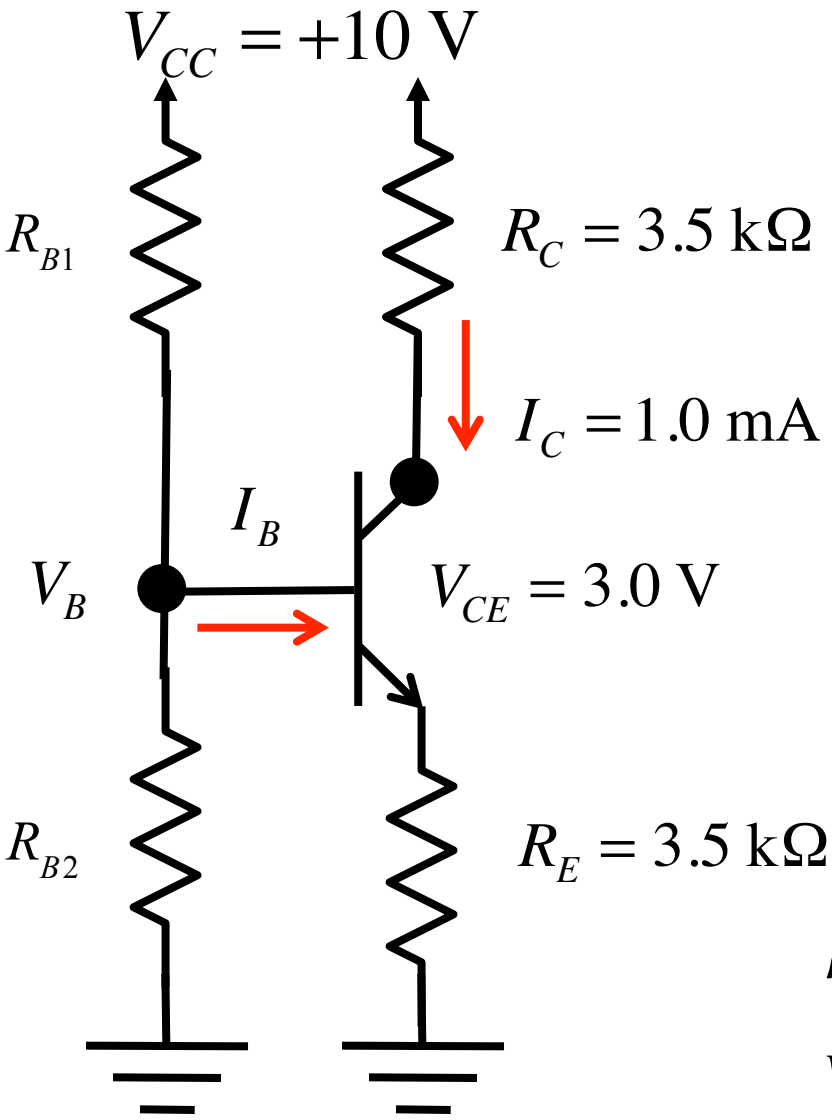
Have 7 V to split between 2 resistors.

Let: $V_{R_C} = V_{R_E} = 3.5$ V

$$R_C = \frac{3.5\text{ V}}{1.0\text{ mA}} = 3.5\text{ k}\Omega$$

$$R_E = \frac{3.5\text{ V}}{1.01\text{ mA}} \approx 3.5\text{ k}\Omega$$

Classic Bias circuit design



Now move to the input:

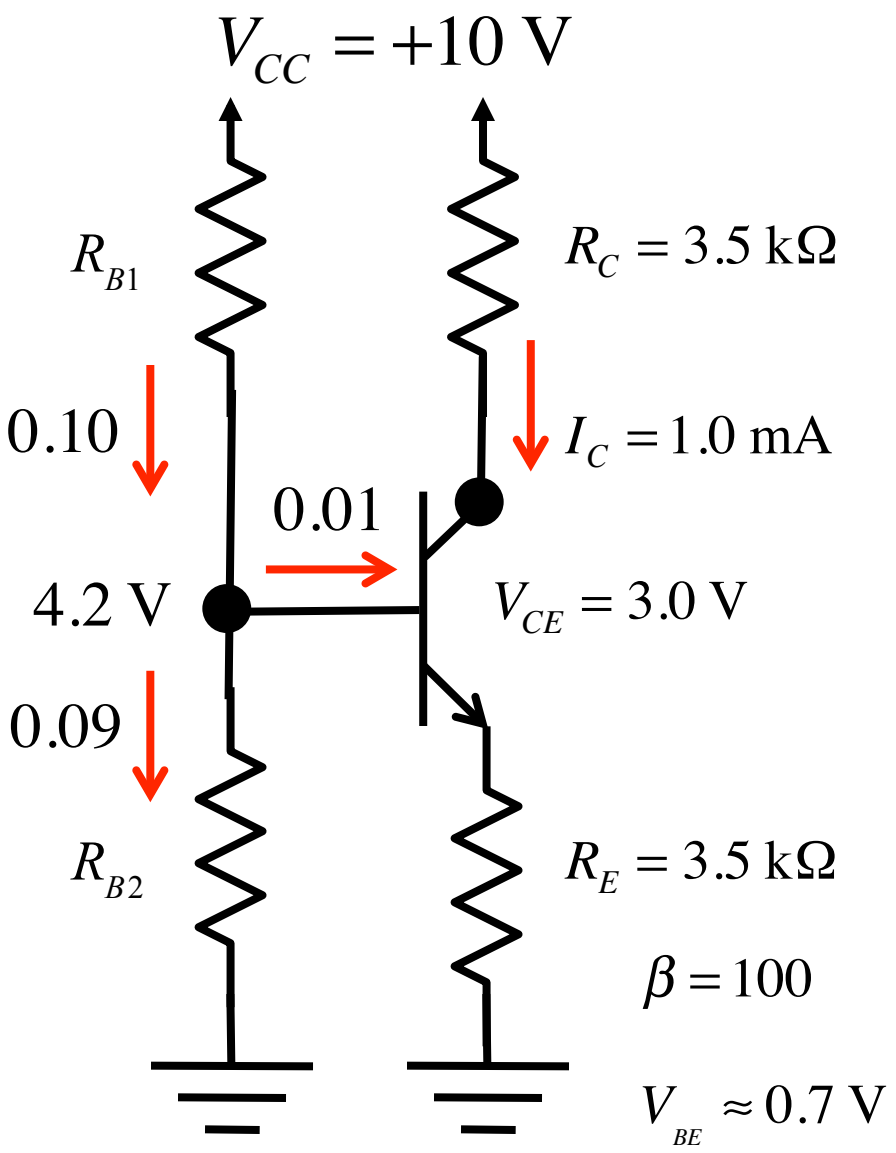
$$V_B = V_{R_E} + 0.7$$
$$= 3.5 + 0.7 = 4.2 \text{ V}$$

$$I_B = \frac{I_C}{100} = 0.01 \text{ mA}$$

$$\beta = 100$$

$$V_{BE} \approx 0.7 \text{ V}$$

Classic Bias circuit design



Choose:

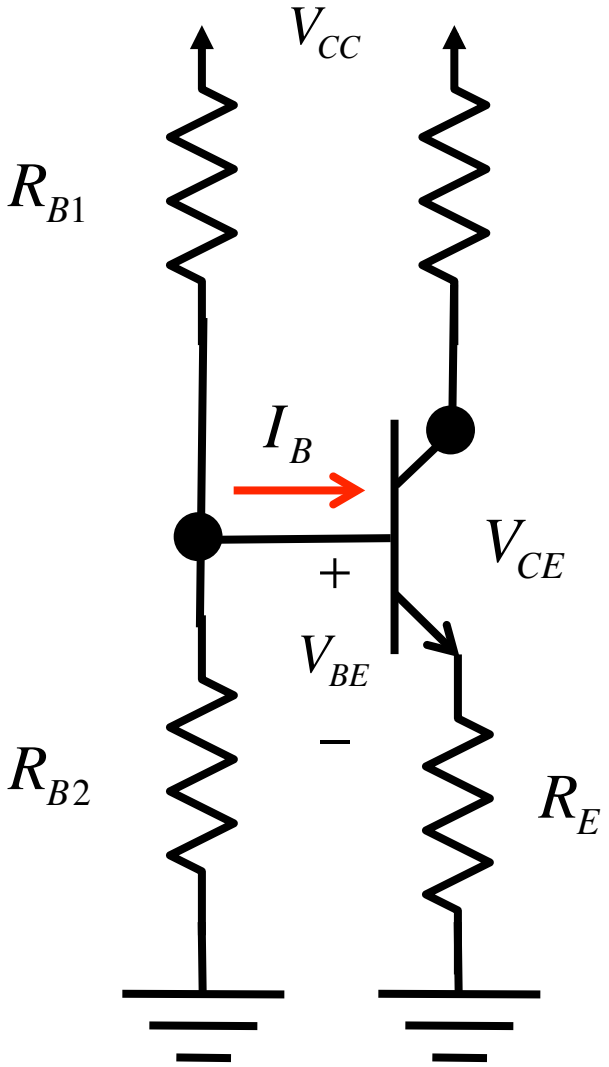
$$I_{R_{B1}} = 10 I_B = 0.1 \text{ mA}$$

$$I_{R_{B1}} = 0.1 \text{ mA} = \frac{(10 - 4.2)\text{V}}{R_{B1}} \rightarrow 58 \text{ k}\Omega$$

$$I_{R_{B2}} = I_{R_{B1}} - I_B$$
$$= 10 I_B - I_B = 0.09 \text{ mA}$$

$$I_{R_{B2}} = 0.09 \text{ mA} = \frac{4.2\text{V}}{R_{B2}} \rightarrow 46.7 \text{ k}\Omega$$

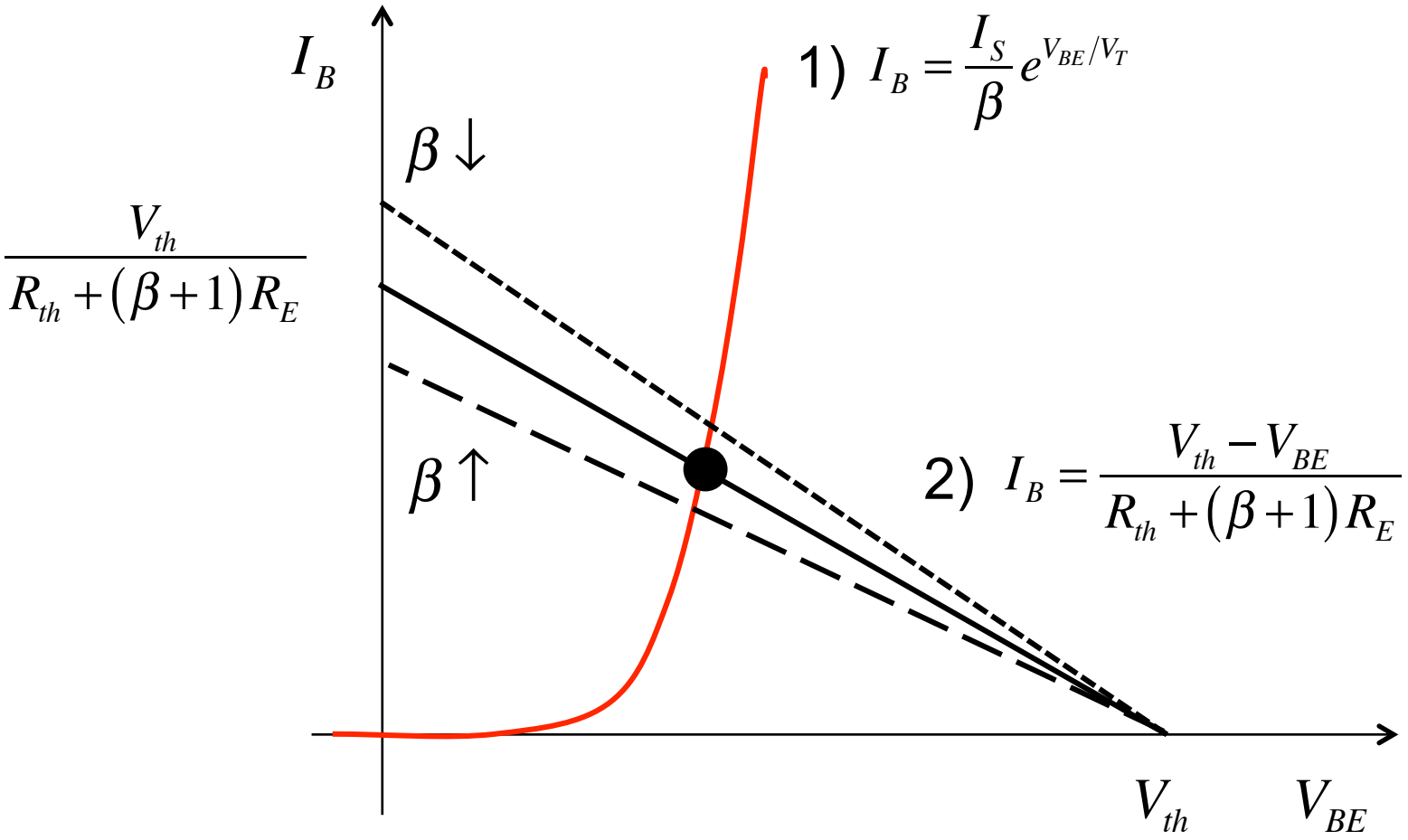
Load line analysis (input)



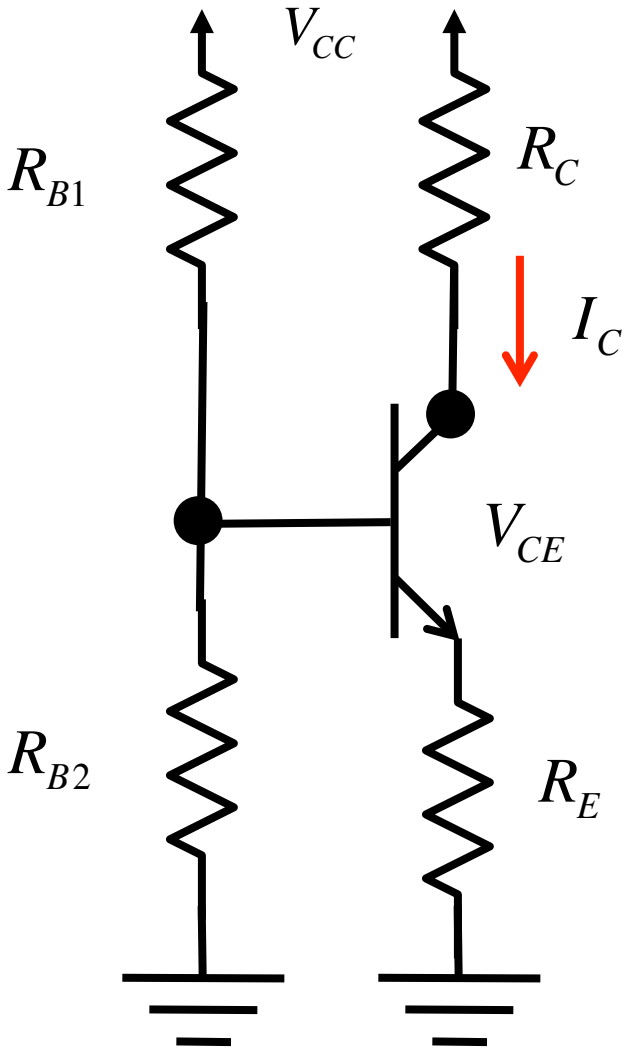
1) Device: $$I_B = \frac{I_S}{\beta} e^{V_{BE}/V_T}$$

2) Circuit: $$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E}$$

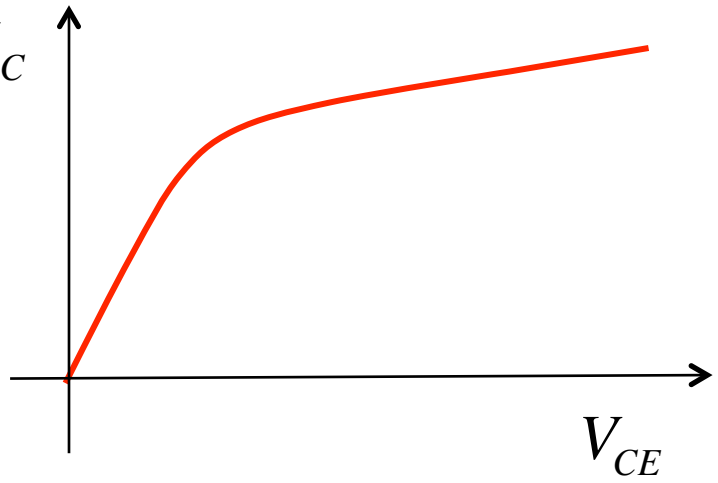
Load line analysis (input)



Load line analysis (output)



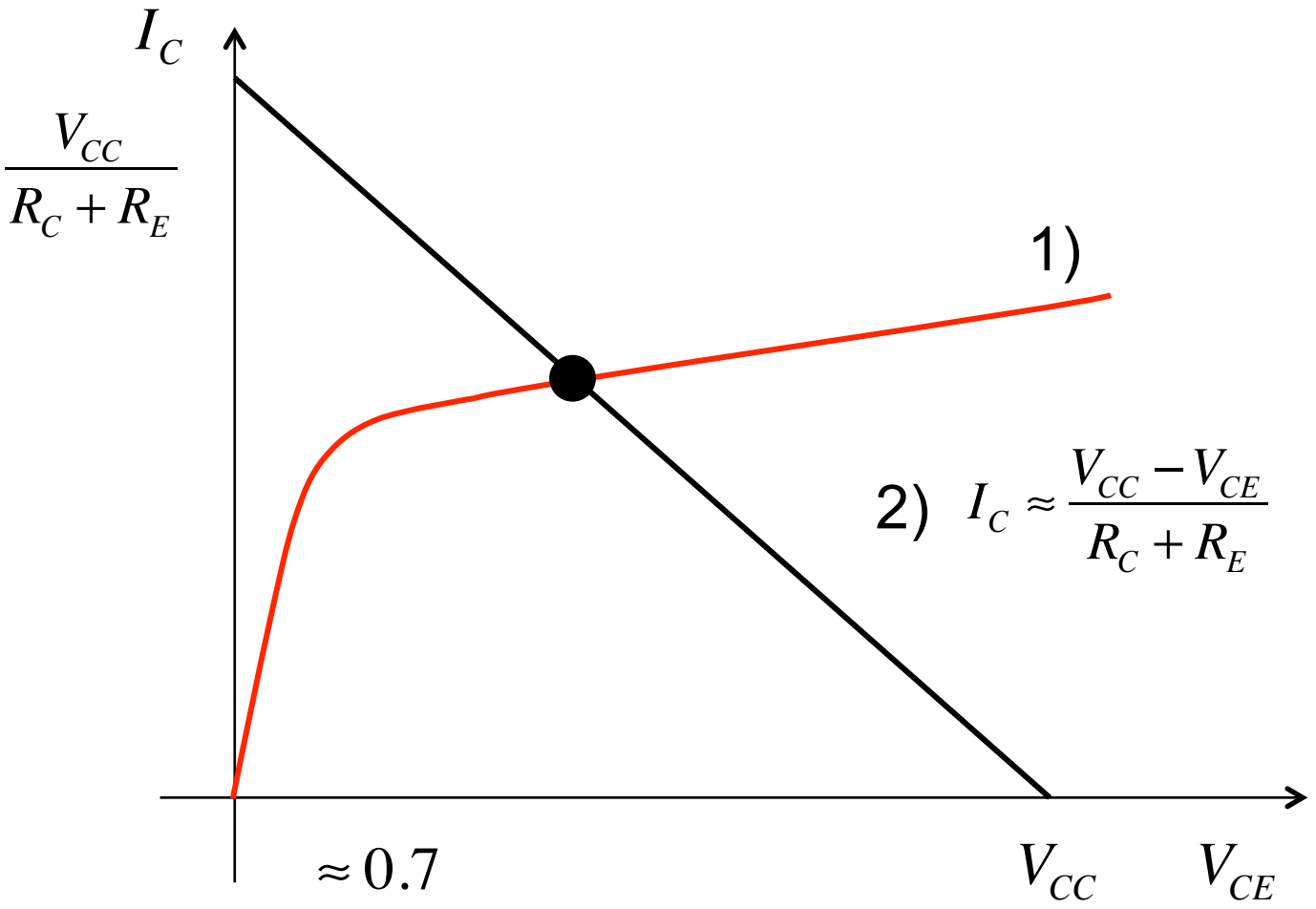
1) Device:



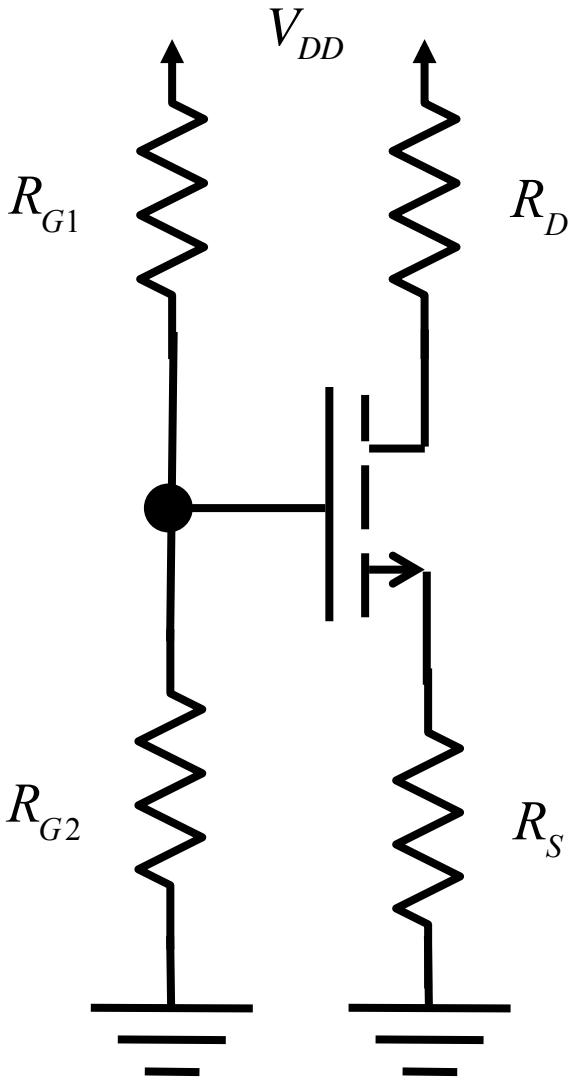
2) Circuit: $V_{CC} = I_C R_C + V_{CE} + \frac{I_C}{\alpha} R_E$

$$I_C \approx \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

Load line analysis (output)



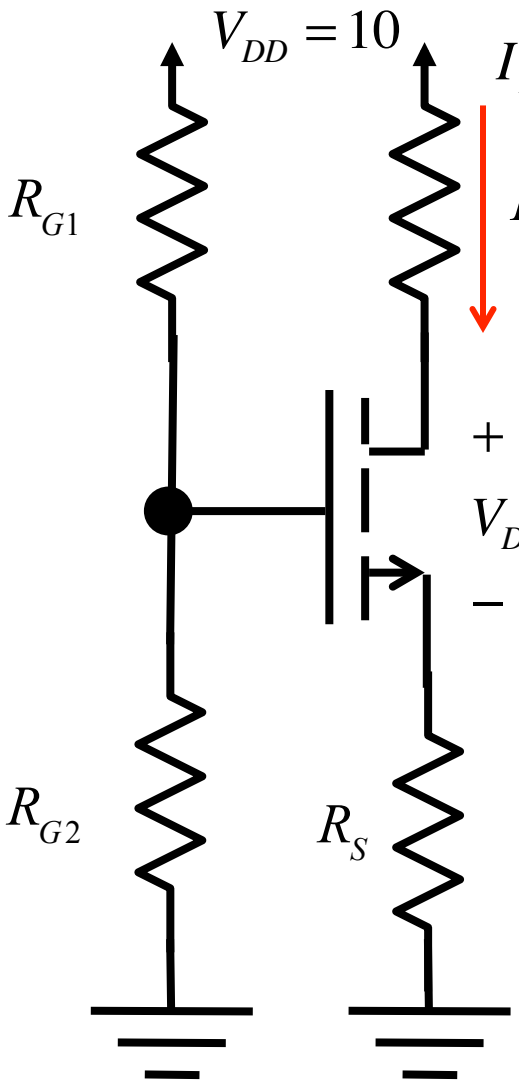
MOSFET 4-resistor bias circuit



Analysis: Given the resistors, power supply voltage, transistor parameters, find the currents and voltages.

Design: given the transistor parameters, power supply, and desired currents and voltages, find the resistor values.

MOSFET 4-resistor bias circuit **design**



Transistor model:

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

$$\frac{k_n'}{2}\frac{W}{L} = 0.1\,\text{mA/V}^2 \qquad V_{tn} = 1.0\ \text{V}$$

$$I_D = 0.1\left(V_{GS} - 1\right)^2$$

$$1 = 0.1\left(V_{GS} - 1\right)^2$$

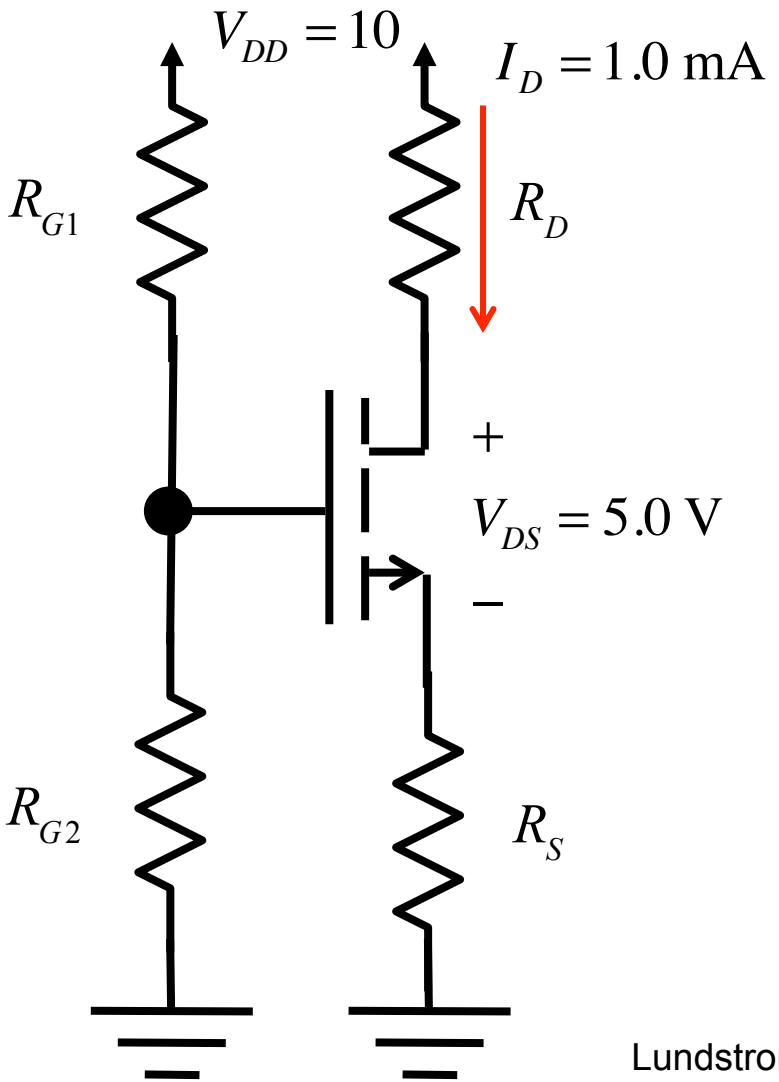
1) device

2) given current

3) Solve for V_{GS}

4) Select resistors to produce V_{GS} and V_{DS}

MOSFET 4-resistor bias circuit **design**



Transistor model:

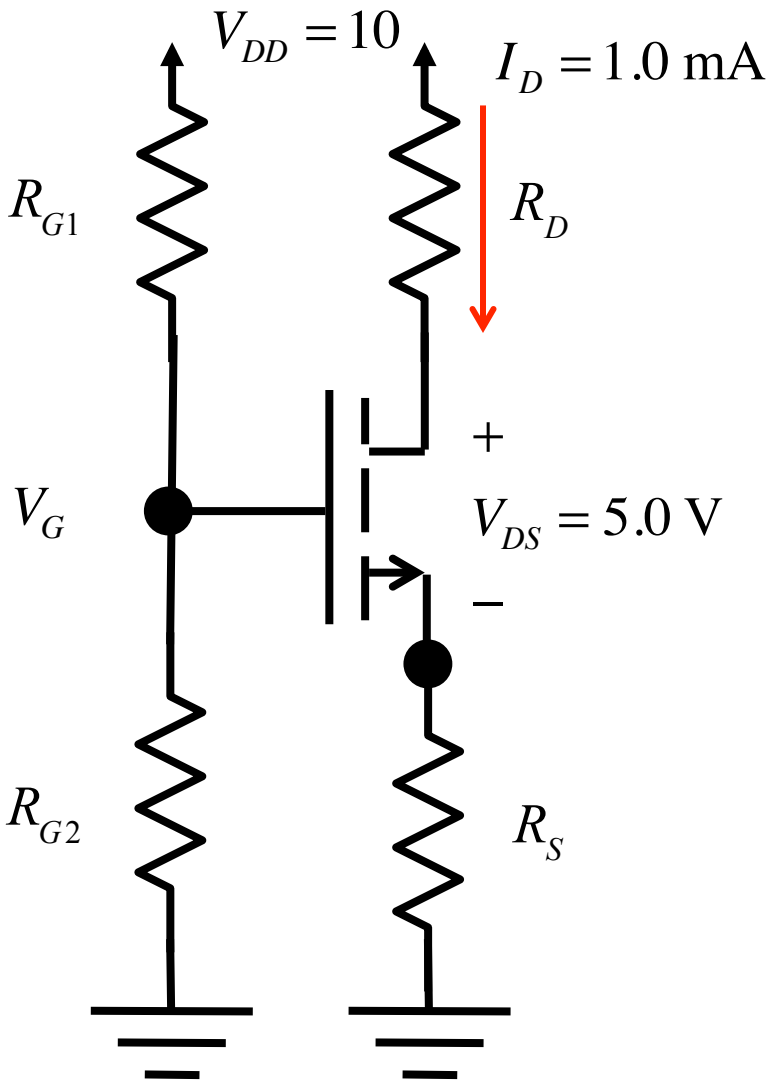
$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

$$\frac{k_n'}{2}\frac{W}{L} = 0.1\,\text{mA/V}^2 \quad V_{tn} = 1.0\text{ V}$$

$$1 = 0.1\left(V_{GS} - 1\right)^2$$

$$V_{GS} = 4.16$$

MOSFET 4-resistor bias circuit **design**



$$1 = 0.1\left(V_{GS} - 1\right)^2$$

$$V_{GS} = 4.16$$

(some arbitrary choices)

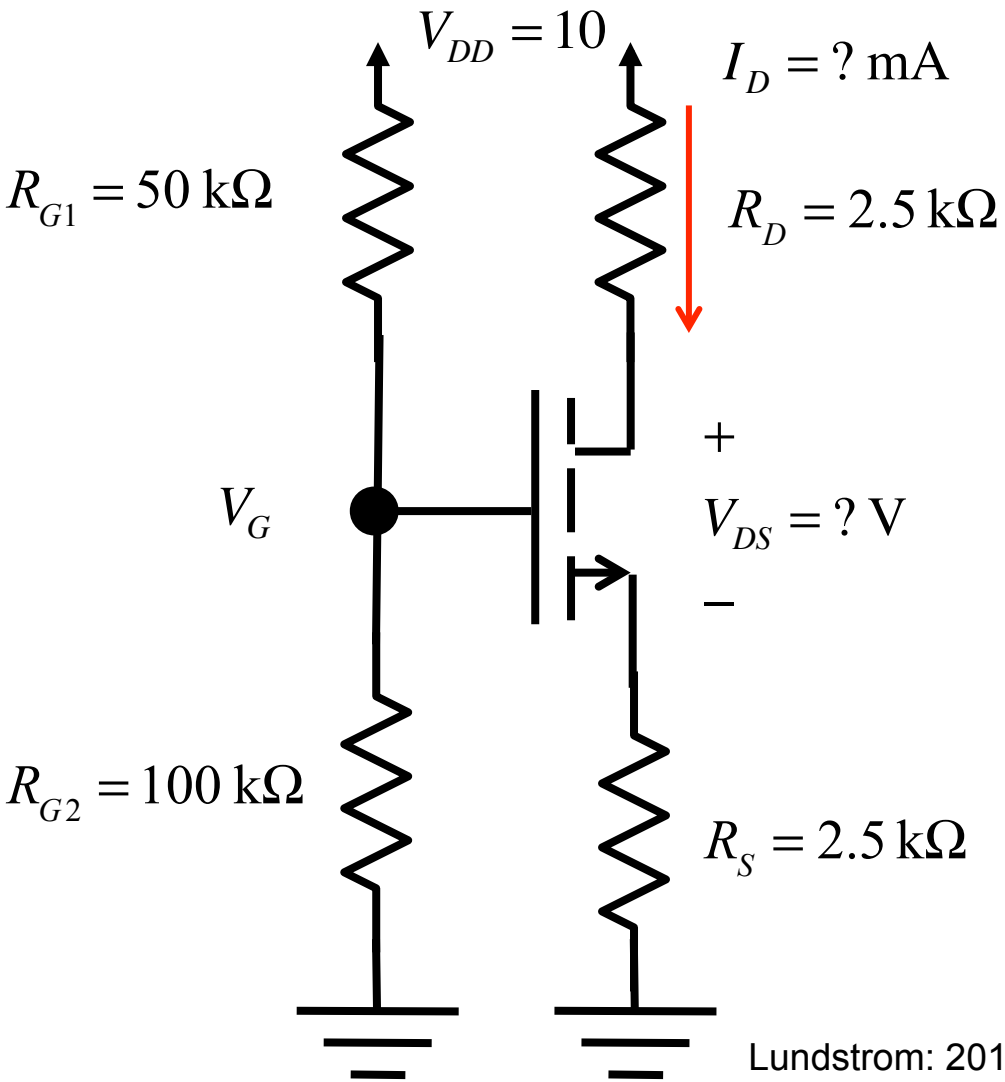
$V_S = 2.5$ $\qquad$ $R_S = R_D = 2.5$ k

$V_G = 2.5 + 4.16 = 6.66$

$R_S = 2.5\,\text{k}\Omega$ $\qquad$ $R_{G1} = 50\,\text{k}\Omega$

$R_D = 2.5\,\text{k}\Omega$ $\qquad$ $R_{G2} = 100\,\text{k}\Omega$

MOSFET 4-resistor bias circuit **analysis**



Transistor model:

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

$$\frac{k_n'}{2}\frac{W}{L} = 0.1\ \text{mA/V}^2 \quad V_{tn} = 1.0\ \text{V}$$

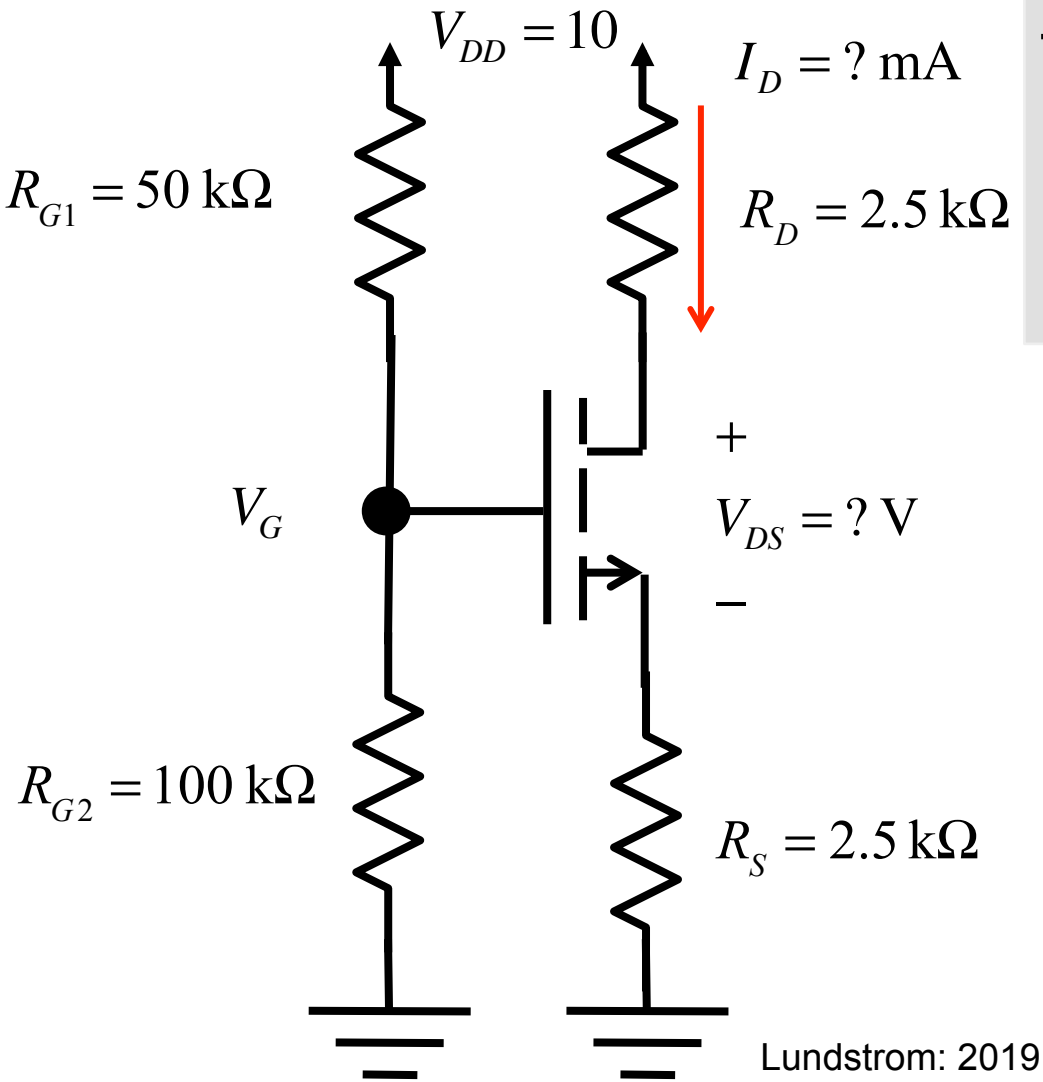
$$I_D = 0.1\left(V_{GS} - 1\right)^2\ \text{mA} \qquad (1)$$

(device)

$$V_{GS} = V_G - V_S = V_G - I_D R_S \qquad (2)$$

(circuit)

MOSFET 4-resistor bias circuit **analysis**



Transistor model:

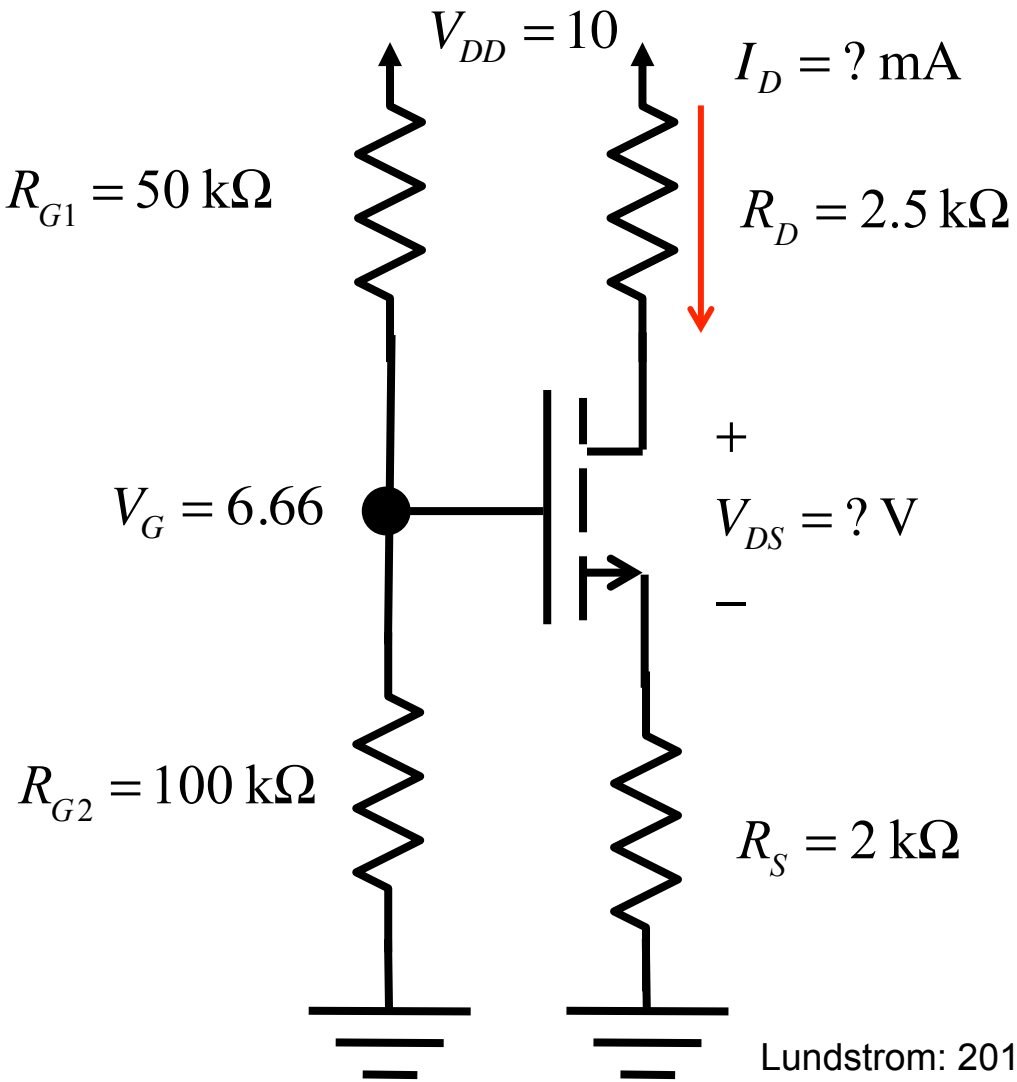
$$I_D = 0.1\left(V_{GS} - 1\right)^2$$

$$V_G = \frac{100}{50+100}10 = 6.66$$

$$V_{GS} = V_G - I_D R_S$$

$$I_D = 0.1\left(V_G - I_D R_S - 1\right)^2$$

MOSFET 4-resistor bias circuit **analysis**



$$I_D = 0.1\left(V_G - I_D R_S - 1\right)^2$$

$$10 I_D = \left(6.66 - 2.5 I_D - 1\right)^2$$

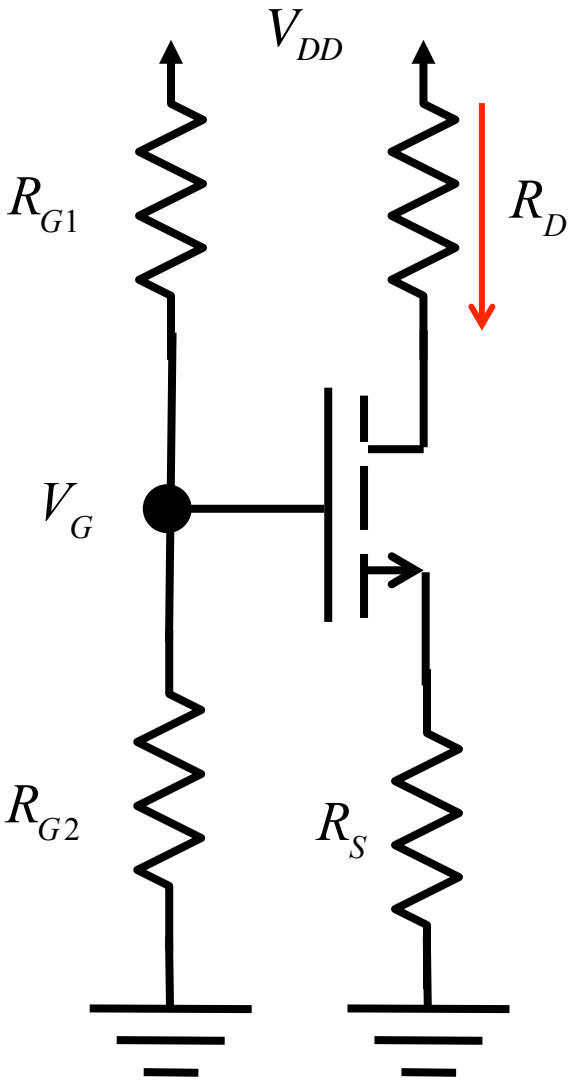
$$I_D^2 - 6.13 I_D + 5.12 = 0$$

$$I_D = 5.14\ \text{mA or } 1.0\ \text{mA}$$

$$I_D = 1.0\ \text{mA}$$

$$V_{DS} = 5.0\ \text{V}$$

Load line analysis



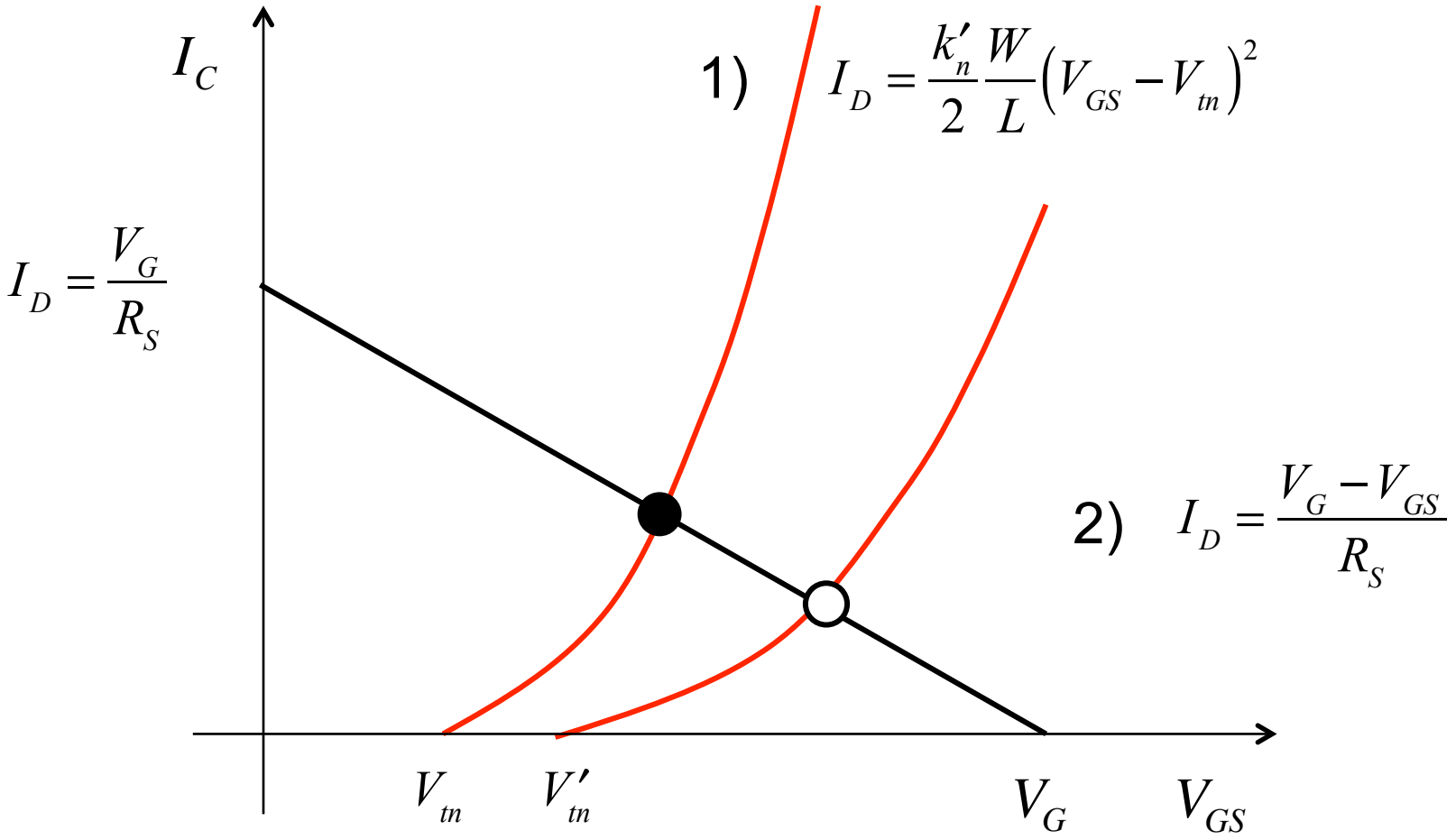
1) Device:

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

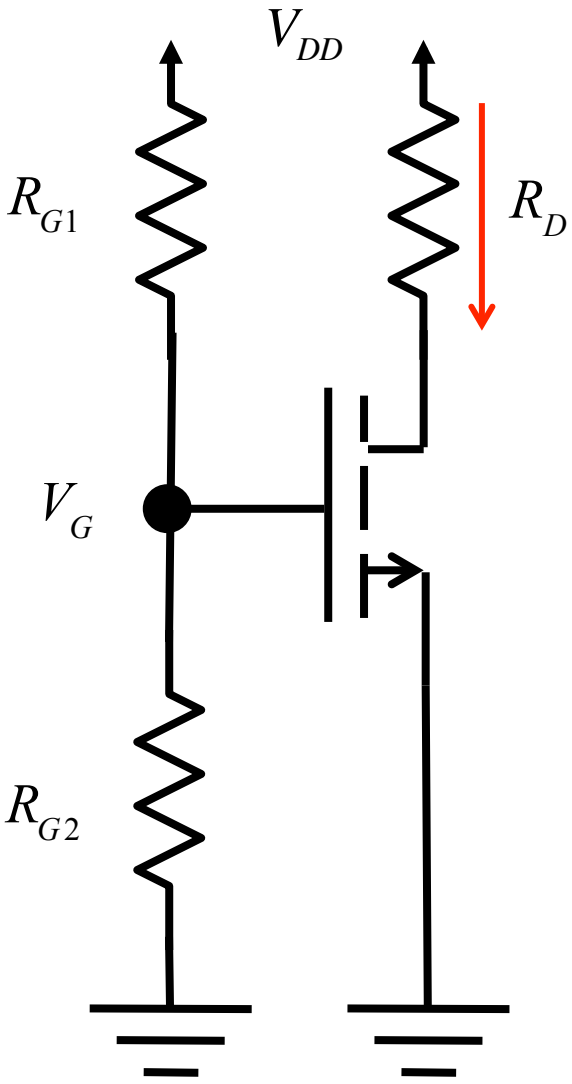
2) Circuit:

$$V_{GS} = V_G - I_D R_S$$

Load line analysis



Load line analysis (without Rs)



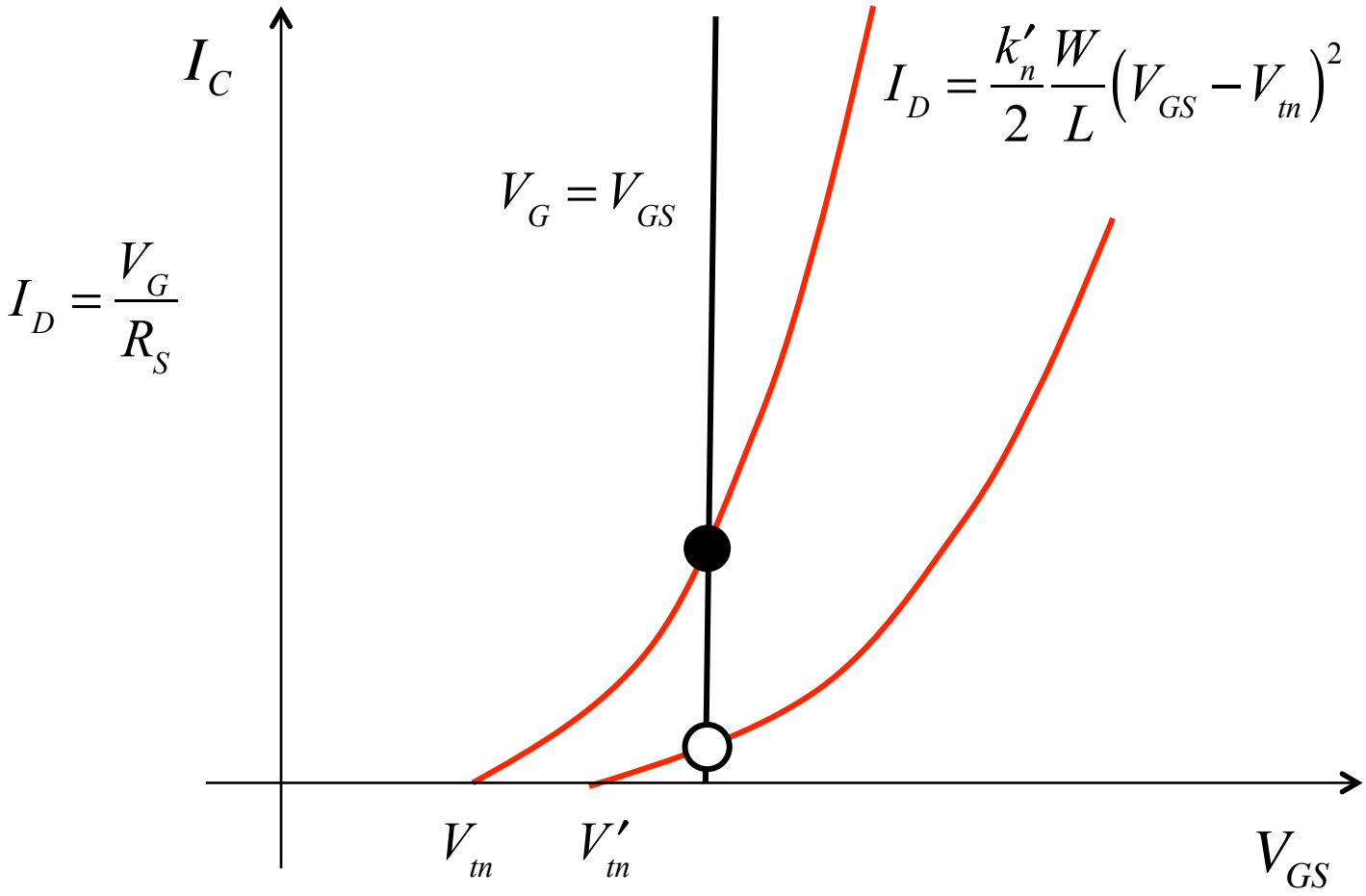
Device:

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

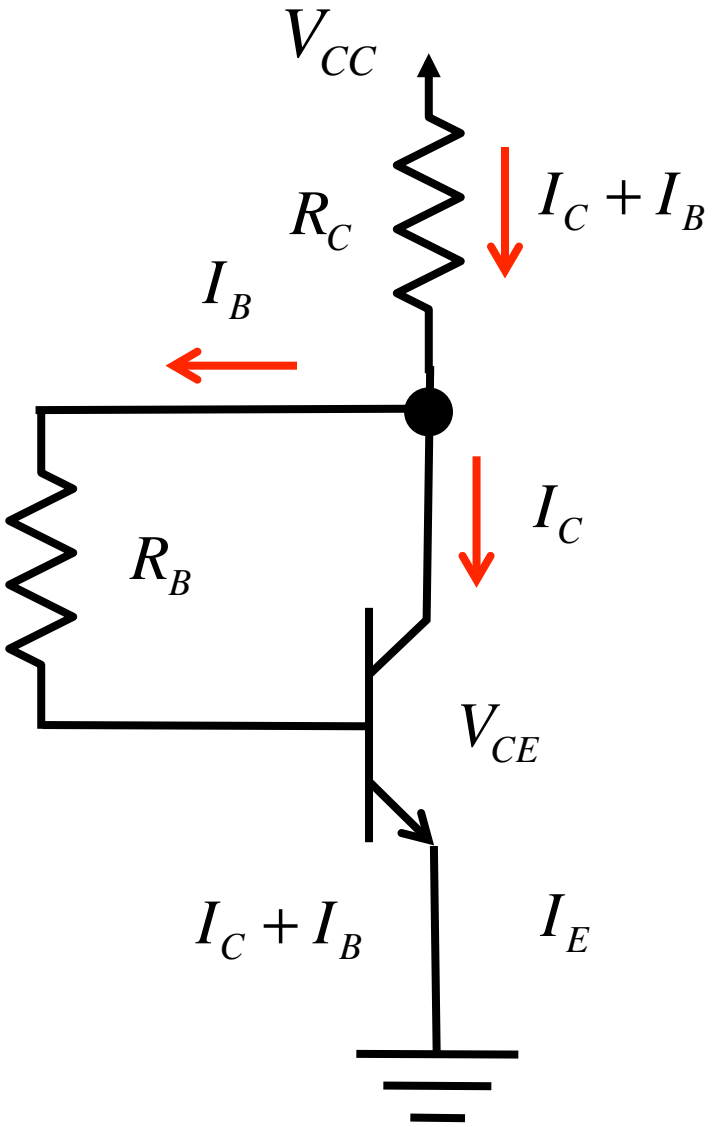
Circuit:

$$V_{GS} = V_G$$

Load line analysis



Also a good bias circuit



See Lecture 12

$$I_C = \frac{V_{CC} - V_{BE}}{R_C\left(1 + \frac{1}{\beta}\right) + R_B\frac{1}{\beta}}$$

$$\beta \to \infty$$

$$I_C \to \frac{V_{CC} - V_{BE}}{R_C}$$

Summary

The classic 4-resistor bias circuit for discrete transistors makes use of negative feedback to deal with variations in beta or threshold voltage.

Other bias circuits can also make use of negative feedback to stabilize the operating point against transistor variations.

Bias circuits should also be designed to that the transistor stays in the active (BJT) or saturation (MOSFET) region.

DC MOSFET Circuits

1) Bias circuit design
2) BJT bias circuits
3) Load line analysis
4) MOSFET bias circuits
5) Load line analysis