

*Spring 2019 Purdue University*

# **ECE 255: L21**

## **Discrete Amplifiers**

(Sedra and Smith, 7<sup>th</sup> Ed., Sec. 7.5)

Mark Lundstrom  
School of ECE  
Purdue University  
West Lafayette, IN USA

Lundstrom: 2019

# Announcements

---

- 1) There is no HW due Monday, but HW7 (Practice Problems for Exam 2) will be discussed in class on Monday.
- 2) Exam 2 is Tuesday, March 5, 6:30-7:30 PM PHYS 112
- 3) Professor Janes will hold a help session on Tuesday in ME 1061 at 1:30 PM.
- 4) No class on Friday, March 8

# Announcements

---

For Exam 2, you should be prepared on: (HW5- HW7)

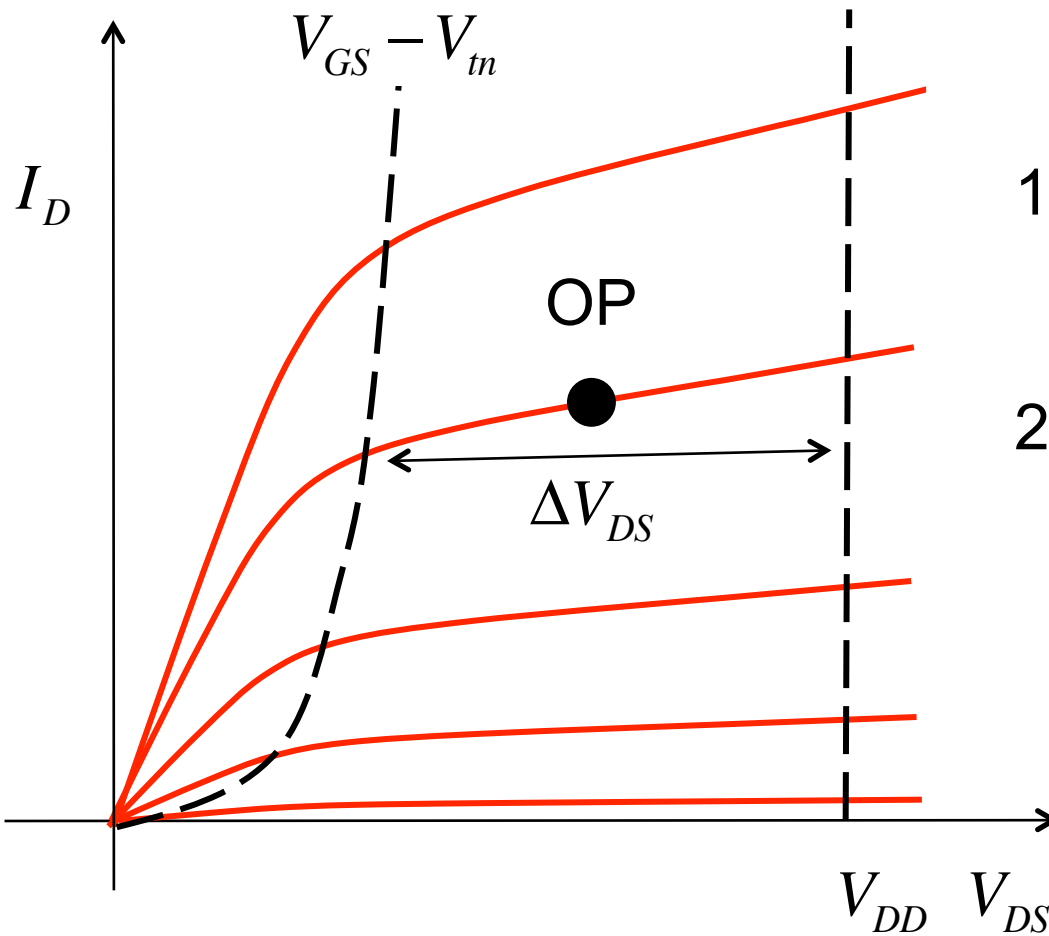
- 1) DC analysis / design of 4-resistor bias circuit
- 2) Small signal models
- 3) Reducing a circuit diagram to a s.s. equiv. circuit
- 3) Amplifier configurations
- 4) CE and CS in detail

# Outline

---

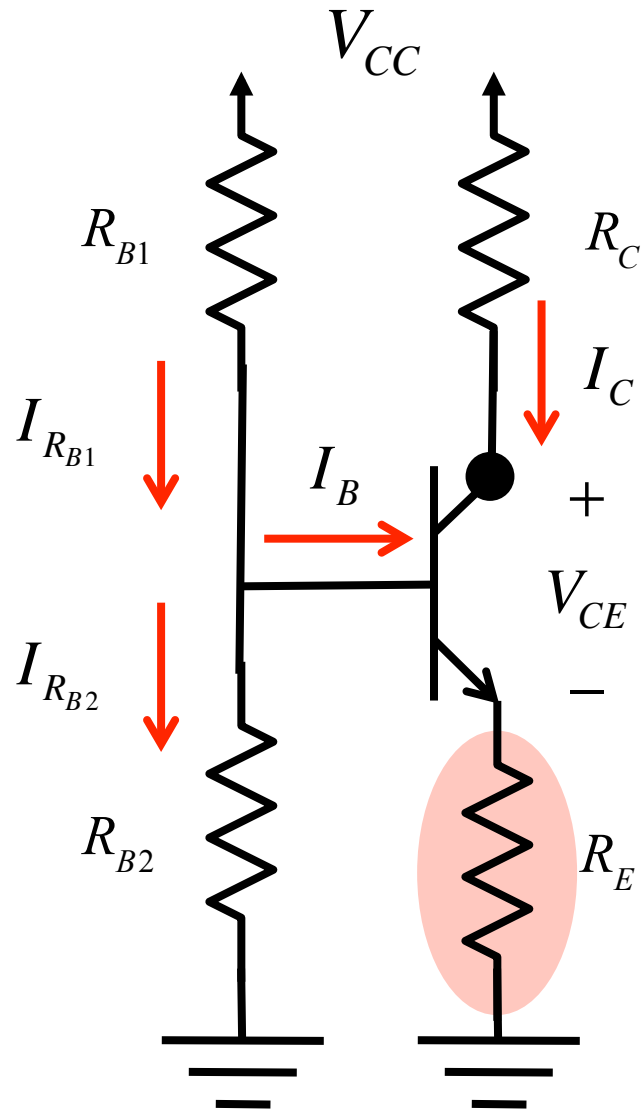
- 1) 4-resistor bias circuits
- 2) Common Source
- 3) Common Gate
- 4) Common Drain
- 5) Amplifier analysis examples

# Operating point and bias circuit design



- 1) Insensitive to device variations (e.g. beta,  $V_t$ )
- 2) Transistor should stay in the active region.

# Classic 4-resistor bias circuit



“Rule of thumb”

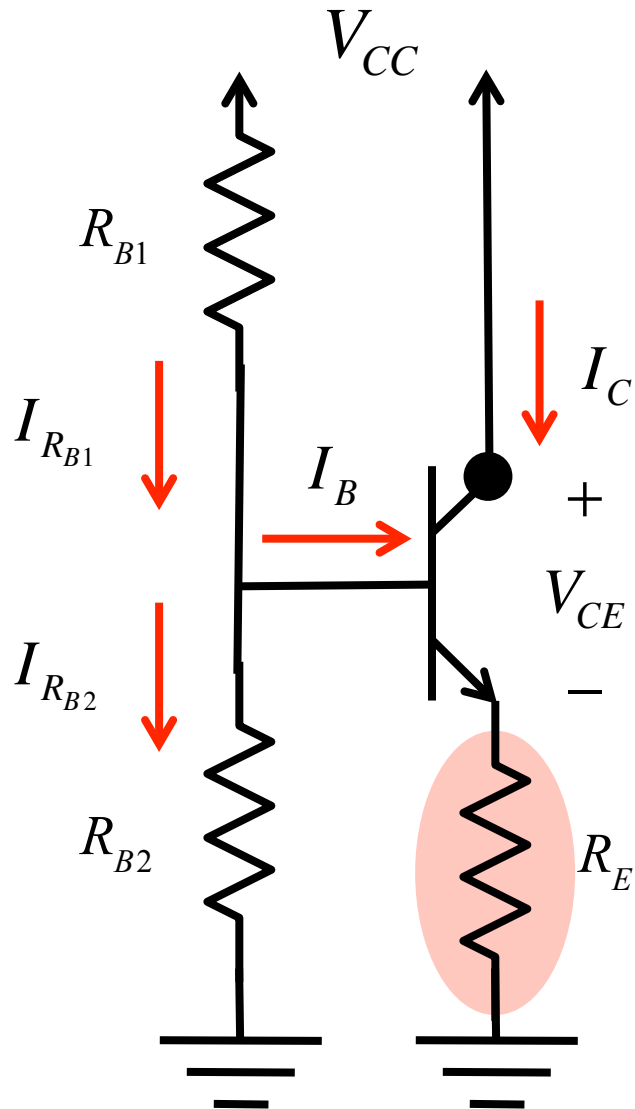
$$I_{R_{B1}} = 10I_B$$

$$I_C = \frac{\beta(V_{th} - V_{BE})}{R_{th} + (\beta + 1)R_E}$$

$$V_{th} = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC}$$

$$R_{th} = R_{B1} \parallel R_{B2}$$

# Classic 4-resistor bias circuit works with $R_C = 0$



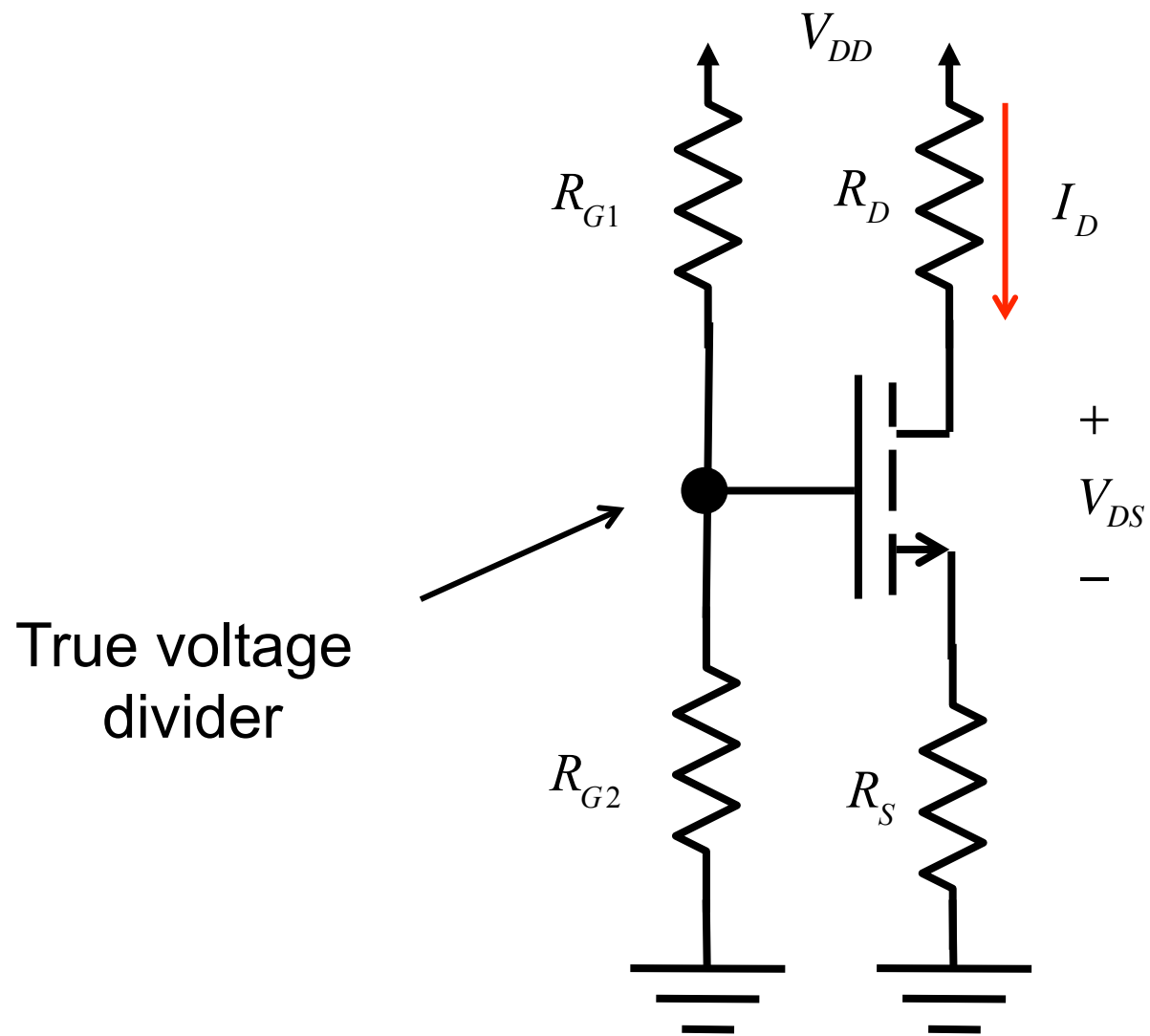
$$I_C = \frac{\beta(V_{th} - V_{BE})}{R_{th} + (\beta + 1)R_E}$$

$$V_{th} = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC}$$

$$R_{th} = R_{B1} \parallel R_{B2}$$

# Classic 4-resistor bias circuit (MOS)

---





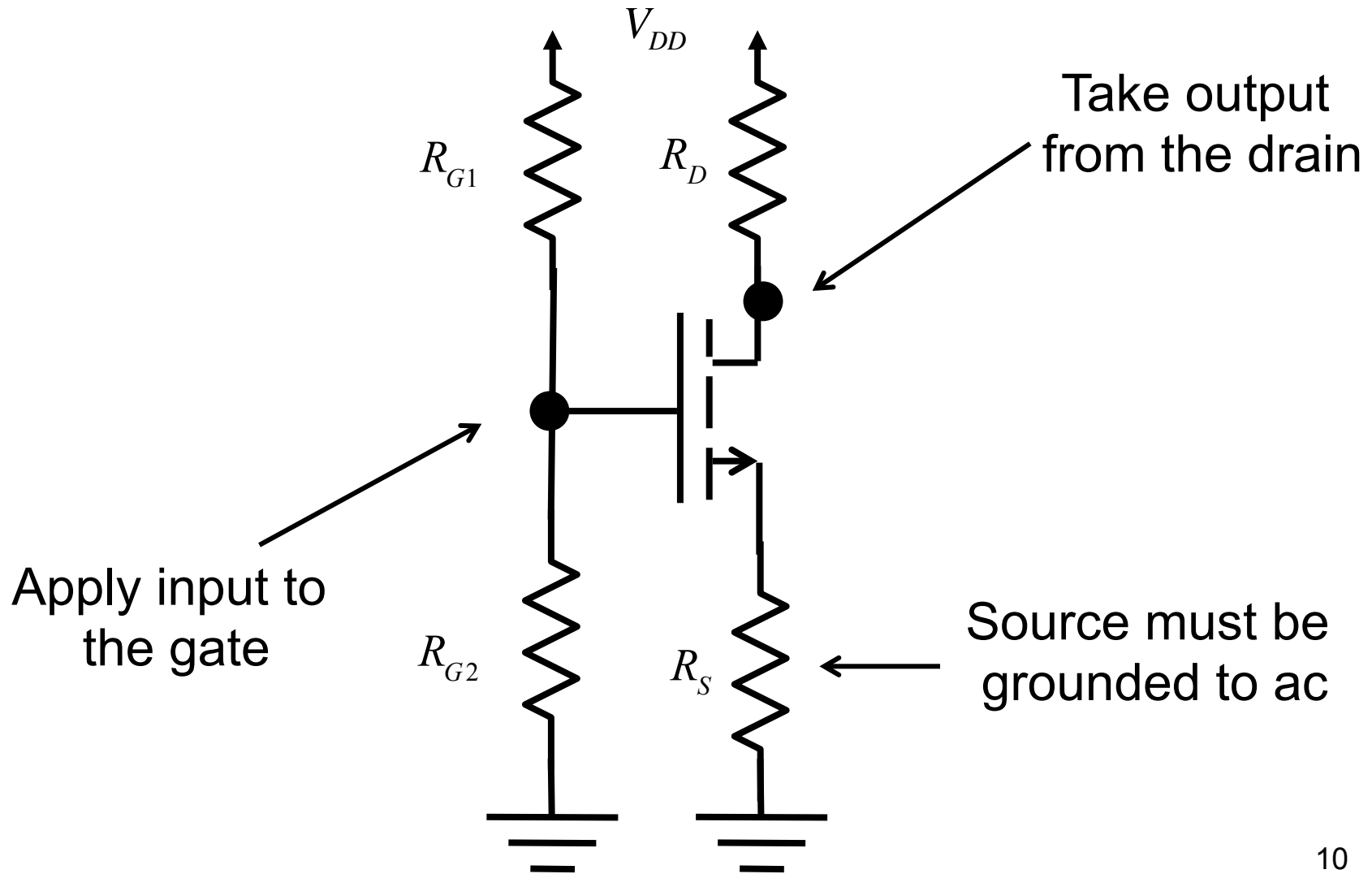
# Outline

---

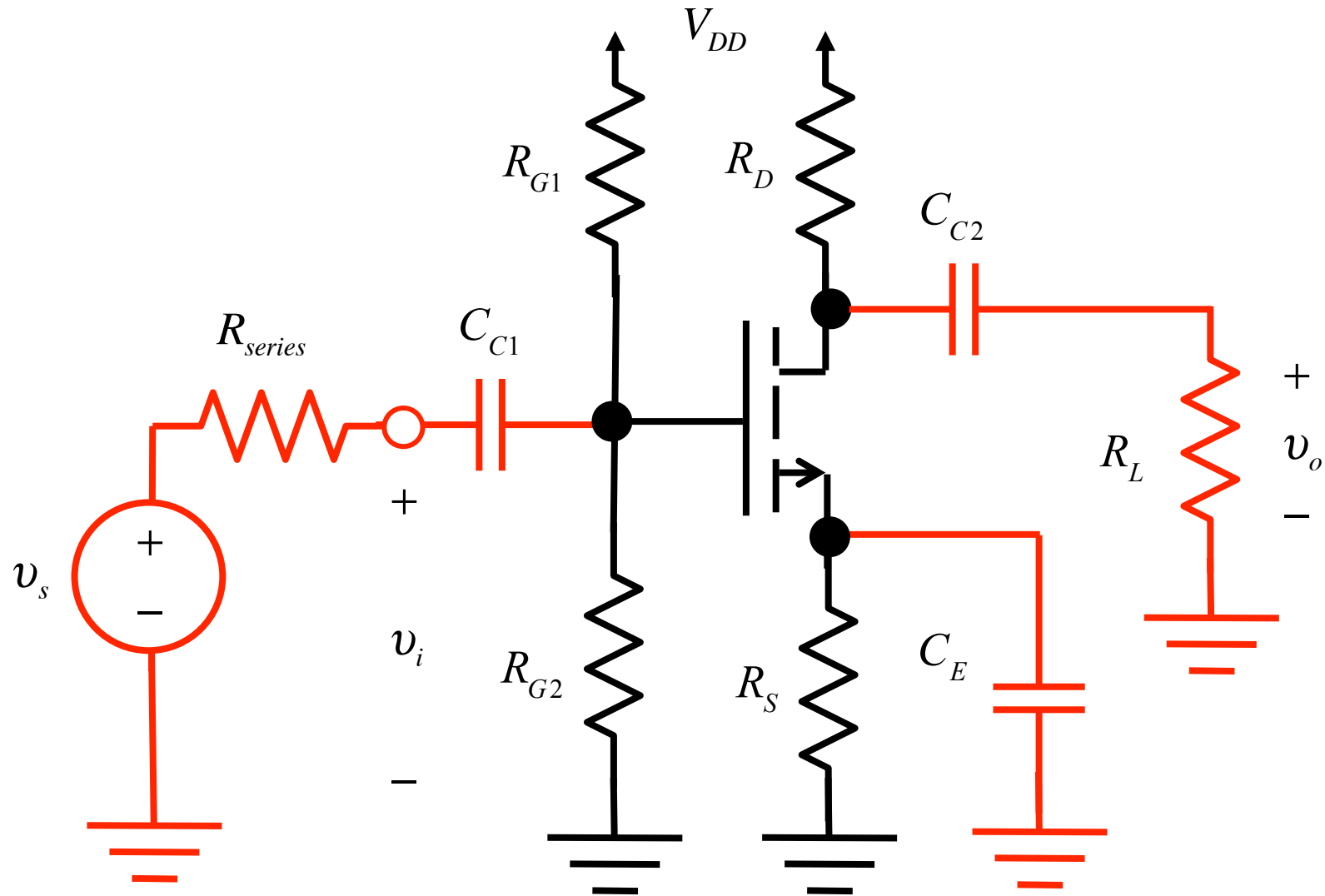
- 1) 4-resistor bias circuits
- 2) Common Source**
- 3) Common Gate
- 4) Common Drain
- 5) Amplifier analysis example

# Common Source

---

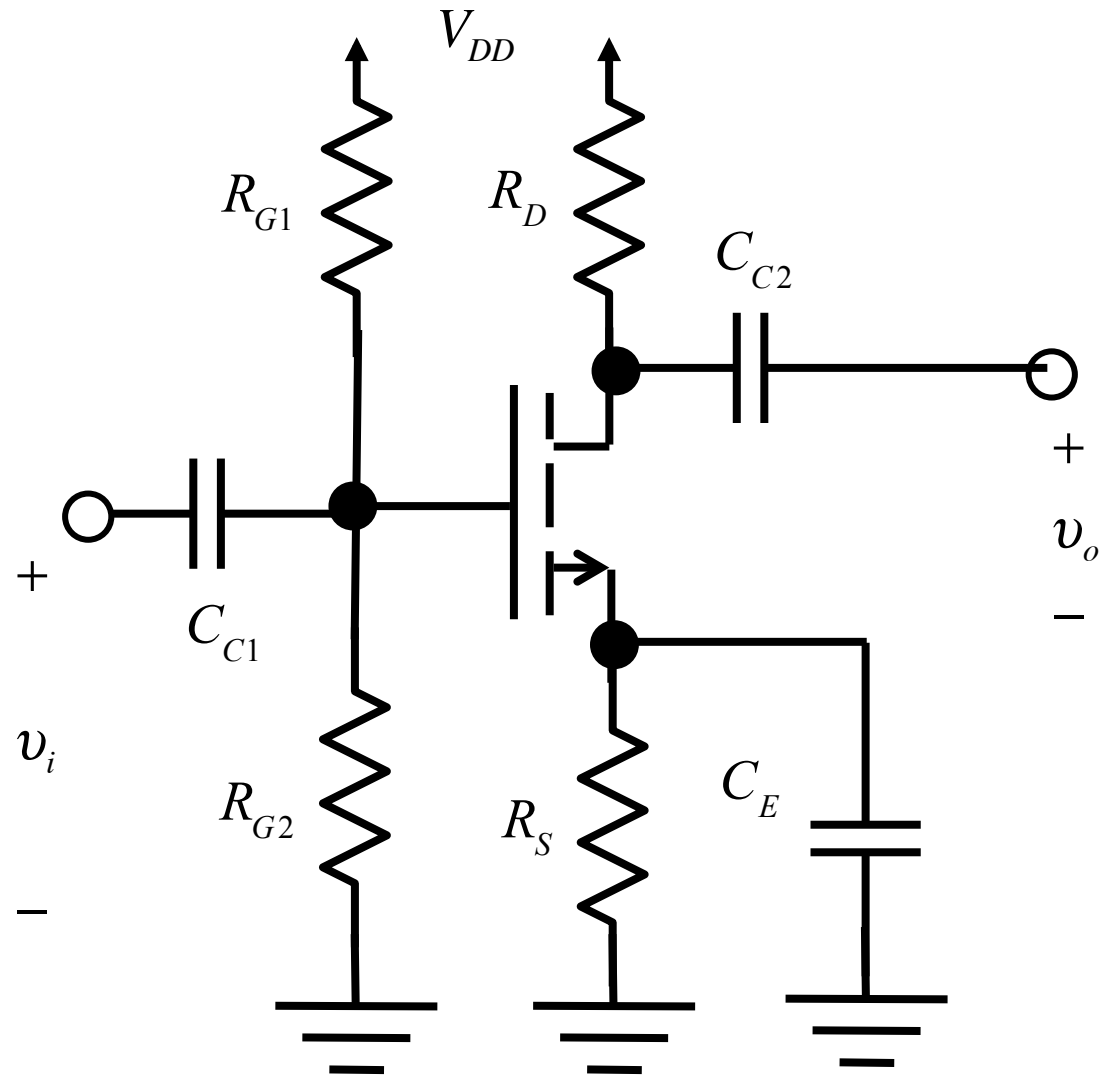


# Common Source



# Common Source w/o signal and load

---

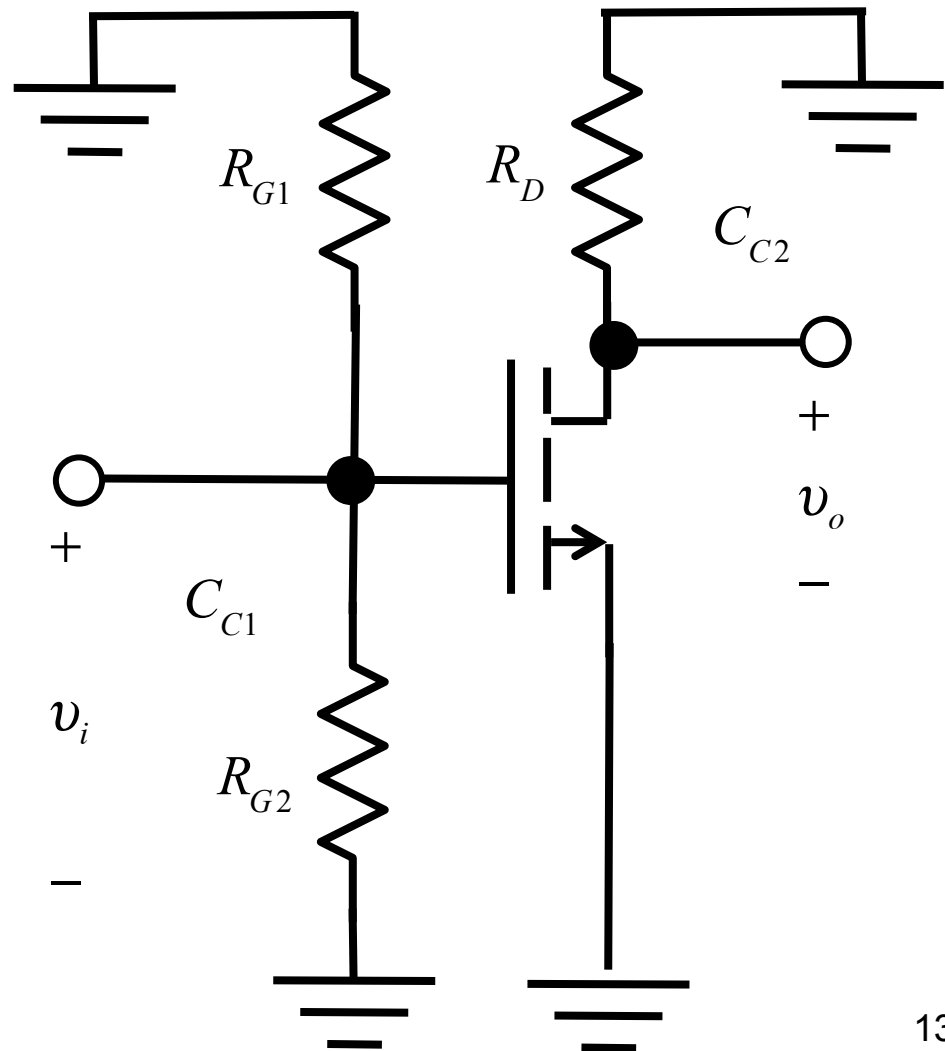


# Common Source (AC)

$$A_{v_i} = -g_m R_D$$

$$R_{in} = R_{G1} \parallel R_{G2}$$

$$R_o = R_D$$



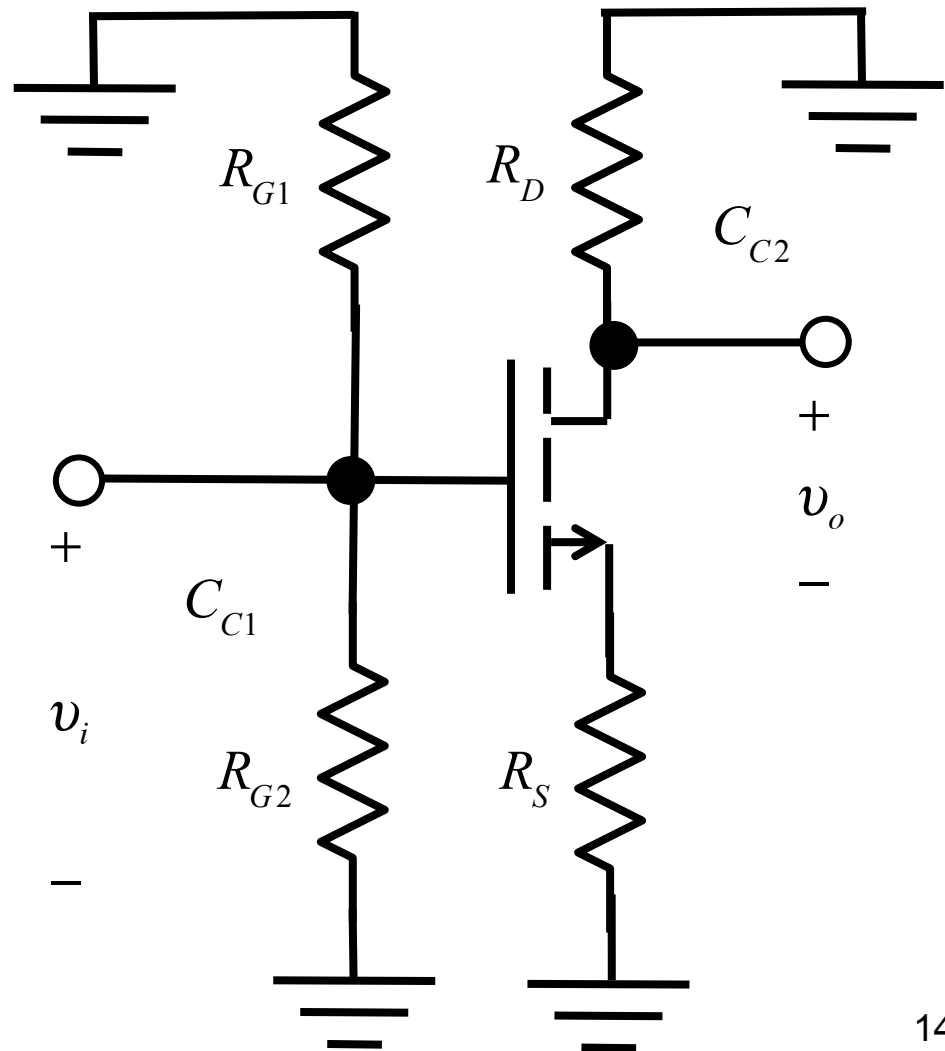
# Common Source with source degeneration (AC)

$$A_{v_i} = \frac{-g_m R_D}{1 + g_m R_S}$$

$$A_{v_i} = -\frac{R_D}{1/g_m + R_S}$$

$$R_{in} = R_{G1} \parallel R_{G2}$$

$$R_o = R_D$$



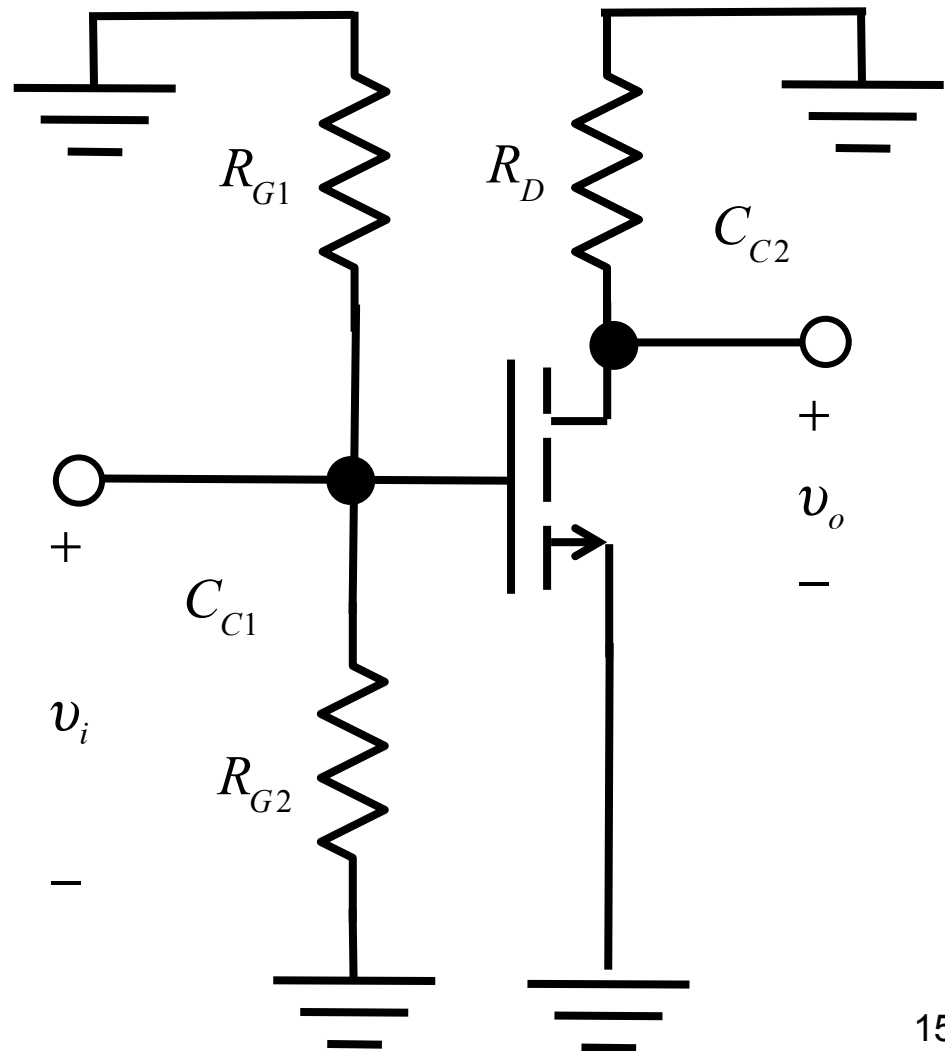
## Common Source with $R_S = 0$ (AC)

$$A_{v_i} = -g_m R_D$$

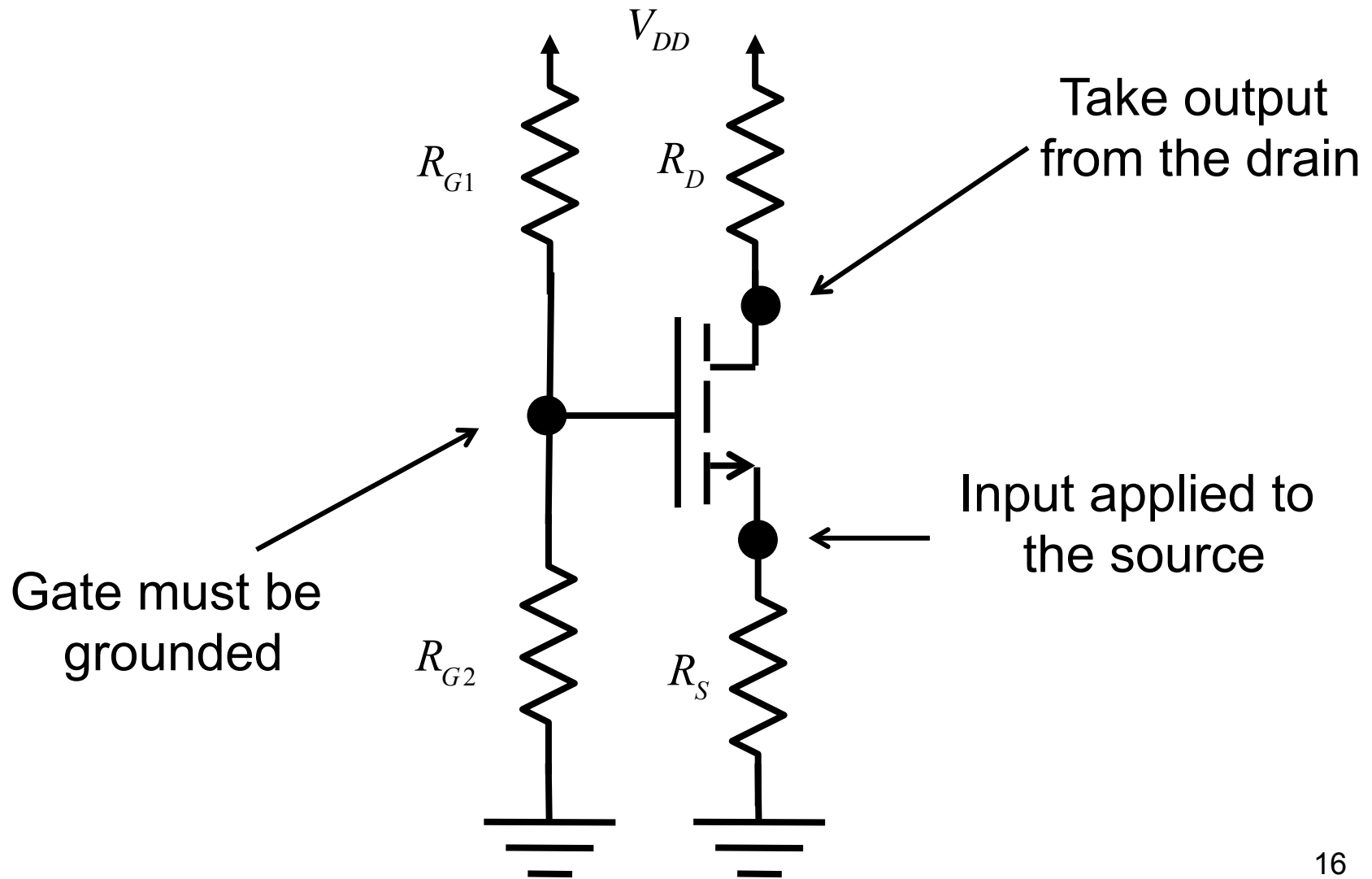
$$A_{v_i} = -\frac{R_C}{1/g_m}$$

$$R_{in} = R_{G1} \parallel R_{G2}$$

$$R_o = R_D$$

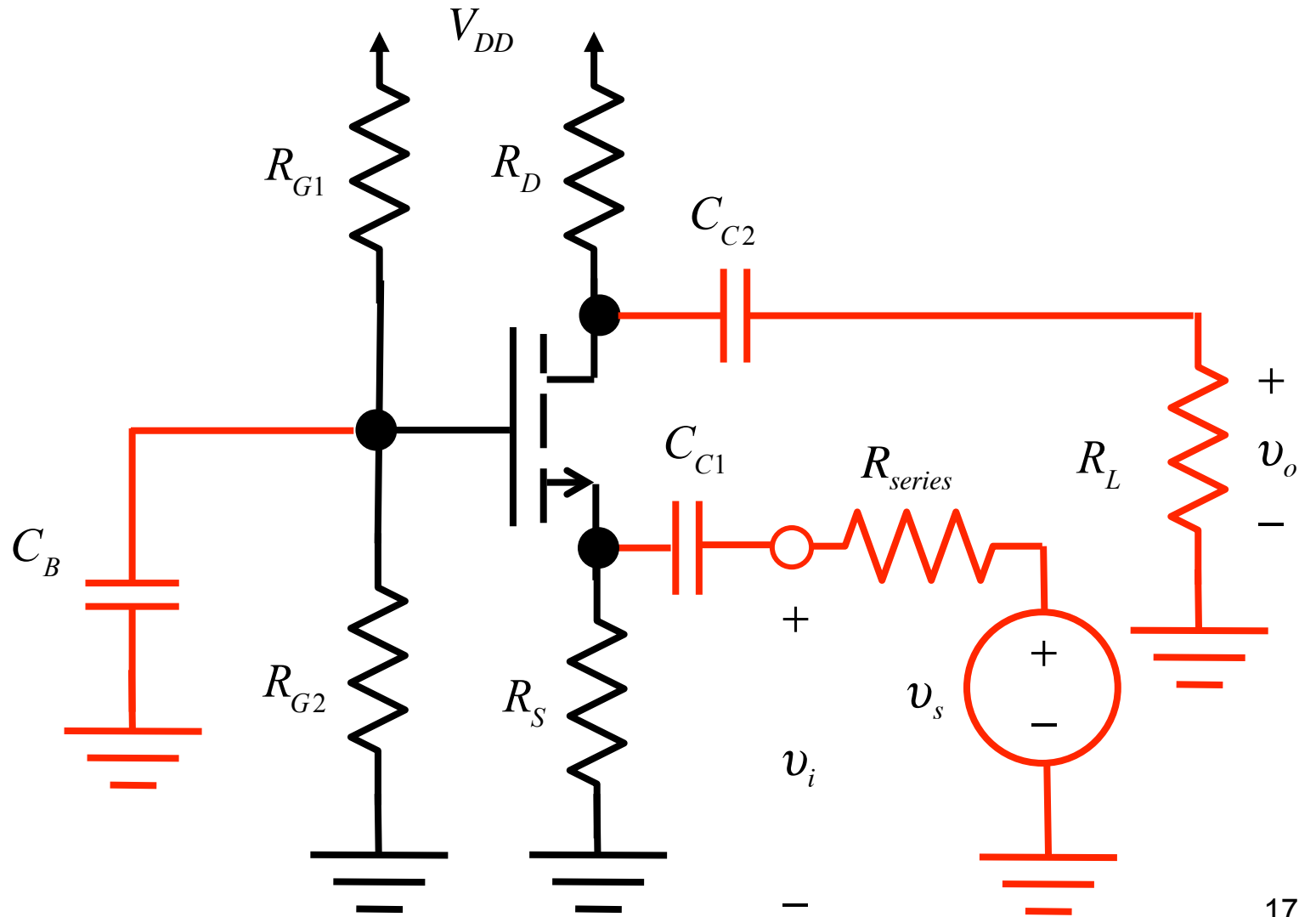


# Common Gate





# Common Gate

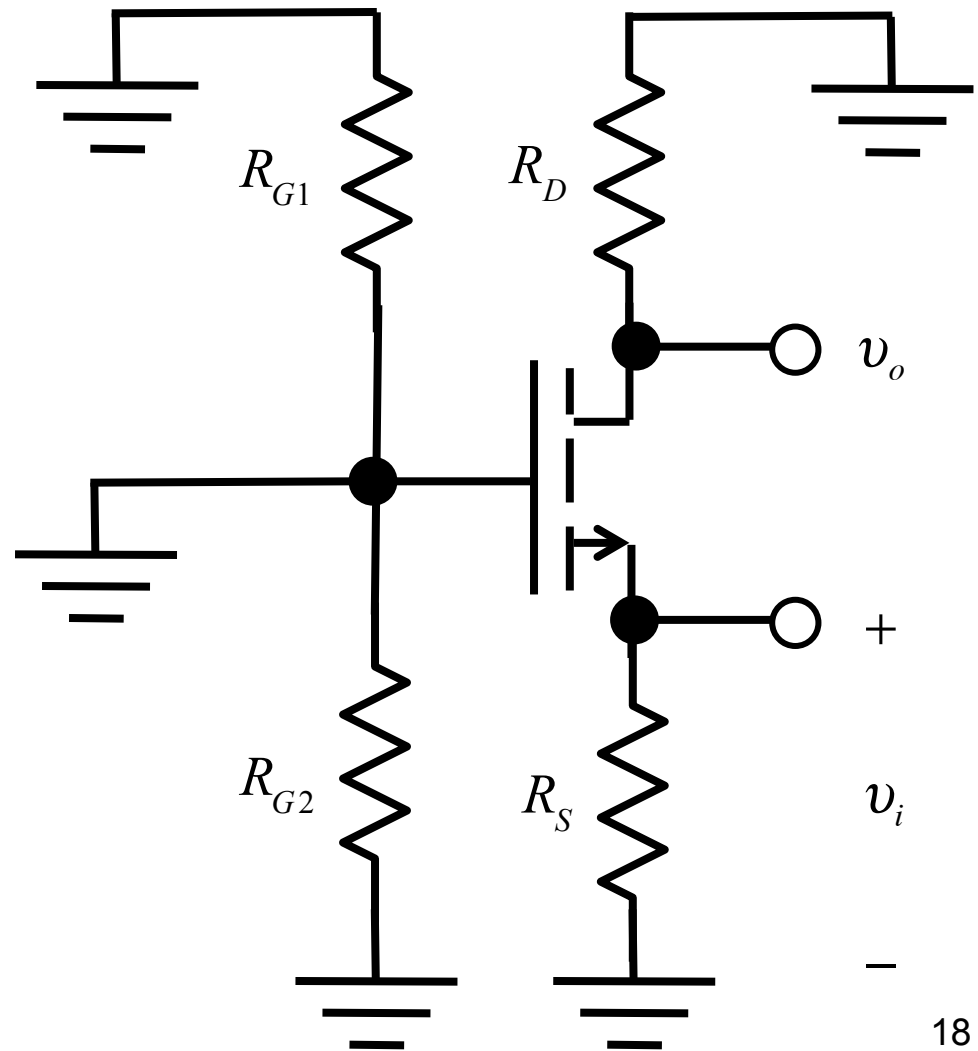


# Common Gate (AC)

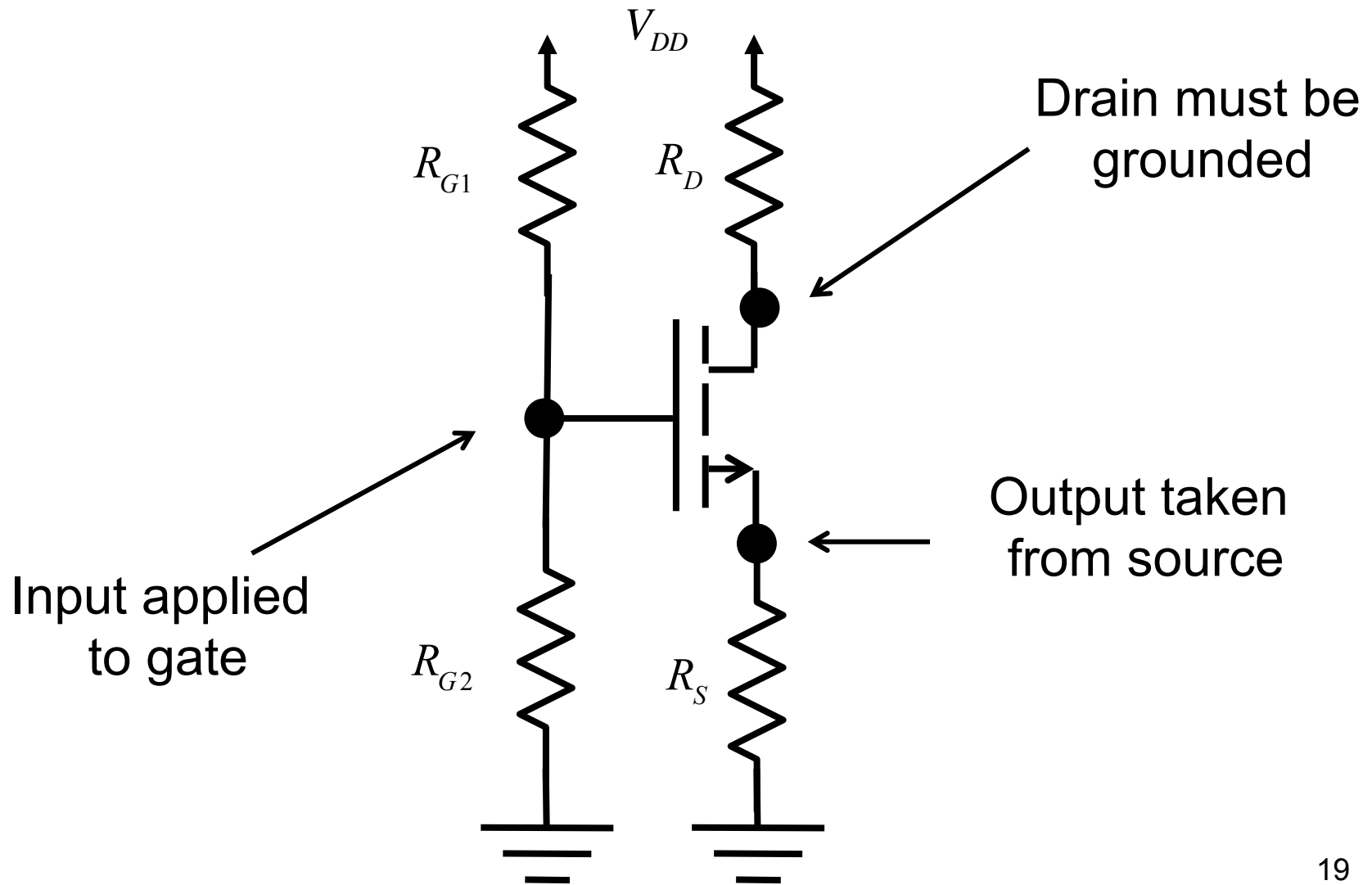
$$A_{v_i} = +g_m R_D$$

$$R_{in} = R_S \parallel \frac{1}{g_m}$$

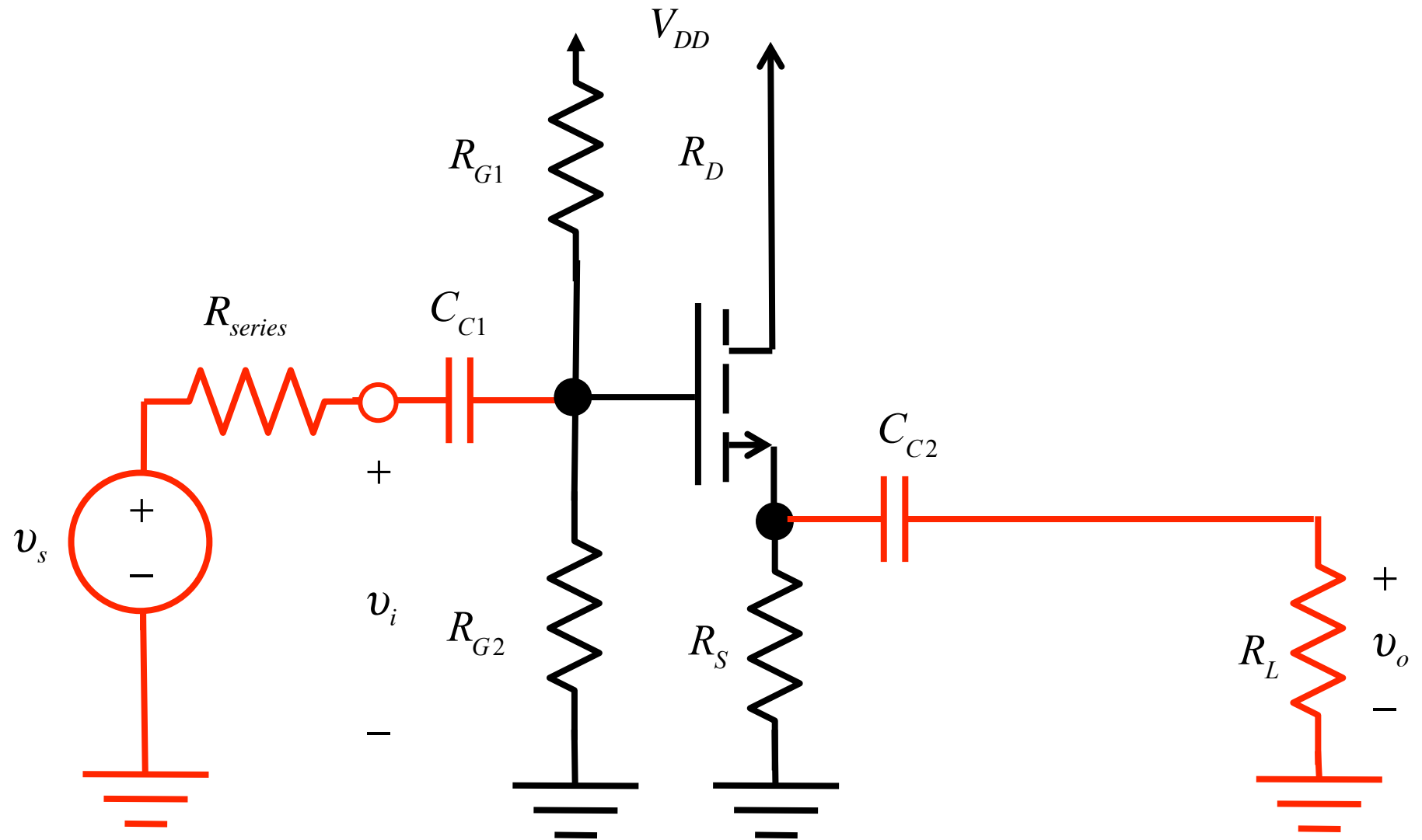
$$R_o = R_D$$



# Common Drain



# Common Drain

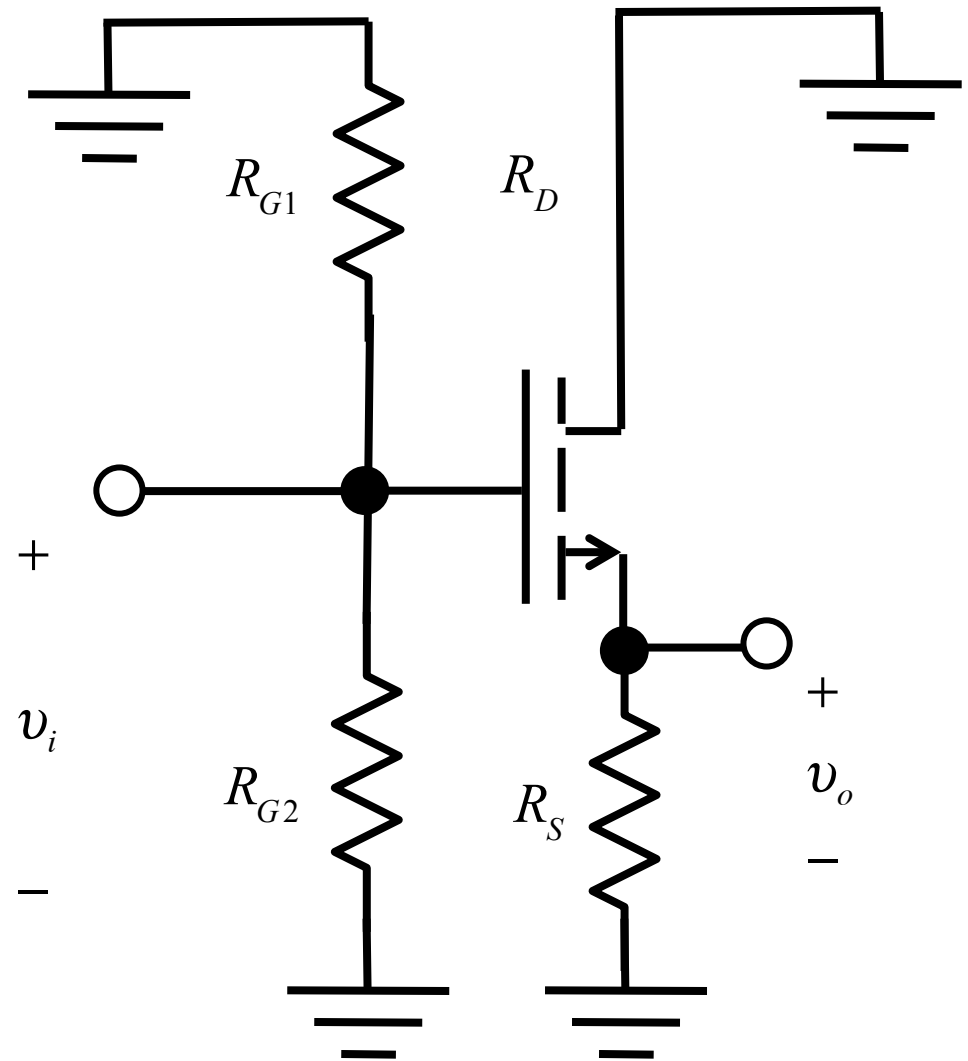


# Common Drain (AC)

$$A_{v_i} = \frac{g_m R_S}{1 + g_m R_S}$$

$$R_{in} = R_{G1} \parallel R_{G2}$$

$$R_o = \frac{1}{g_m}$$

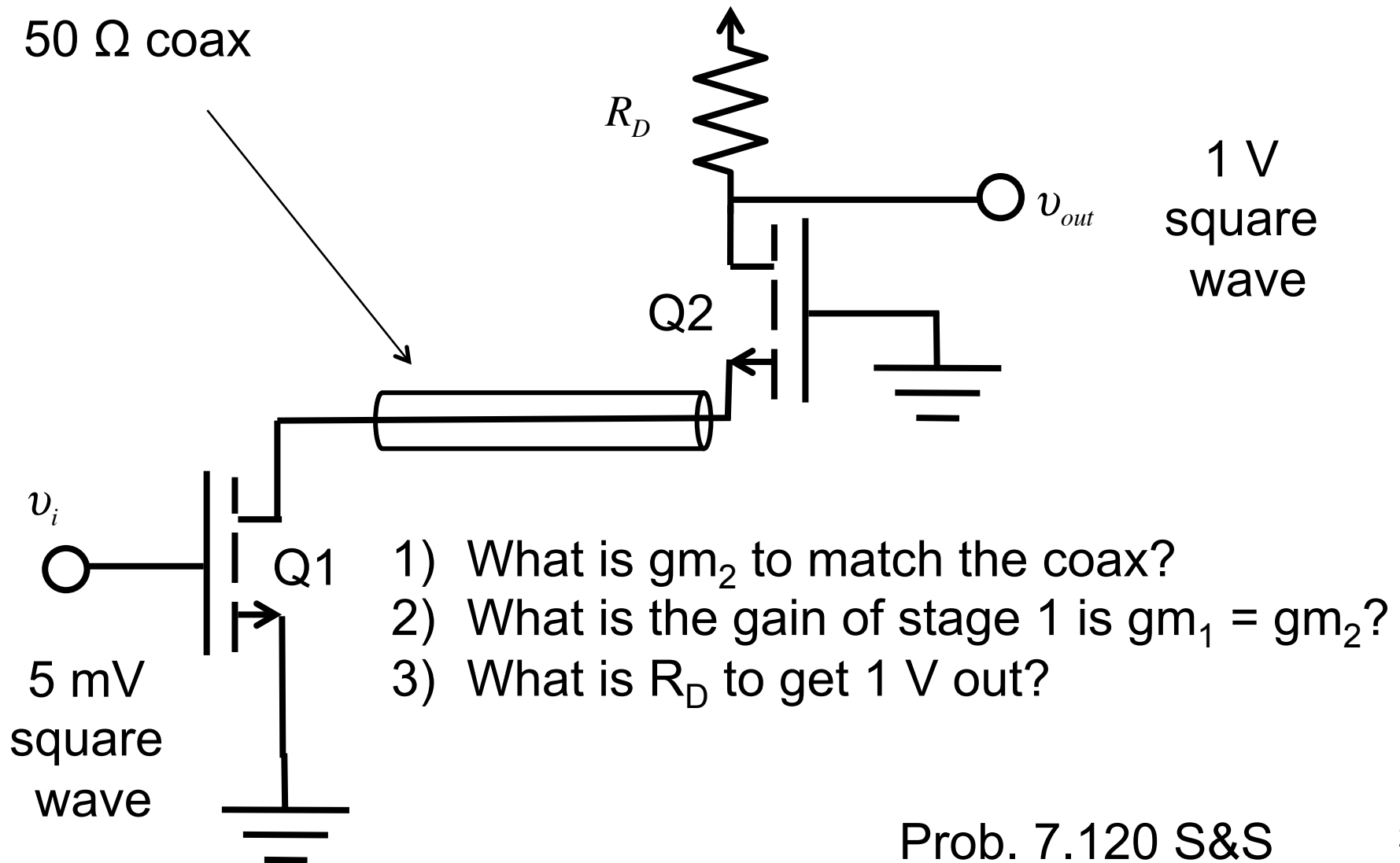


# Outline

---

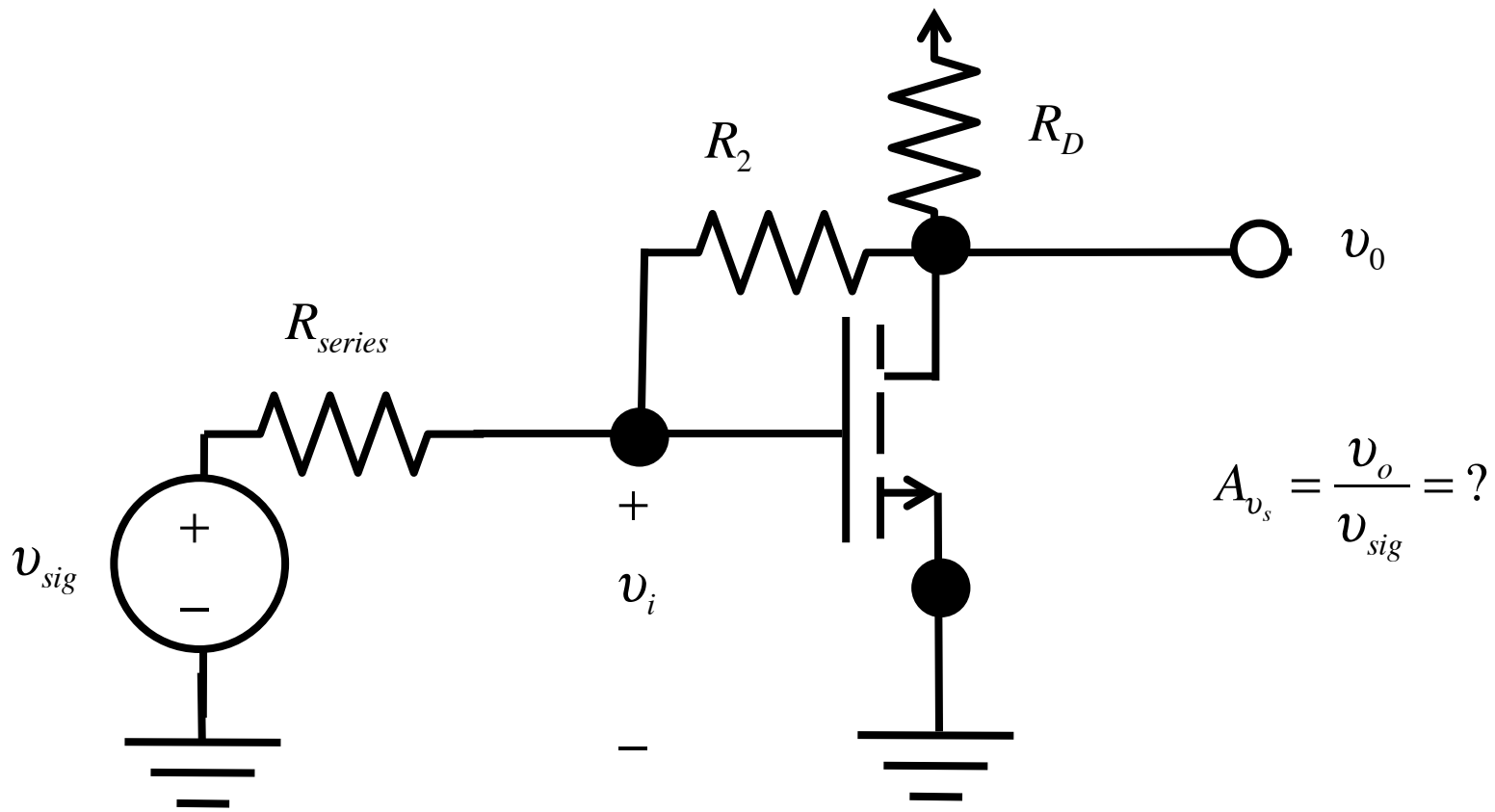
- 1) 4-resistor bias circuits
- 2) Common Source
- 3) Common Gate
- 4) Common Drain
- 5) **Amplifier analysis example**

# Amplifying high frequency pulses



# Feedback amplifier

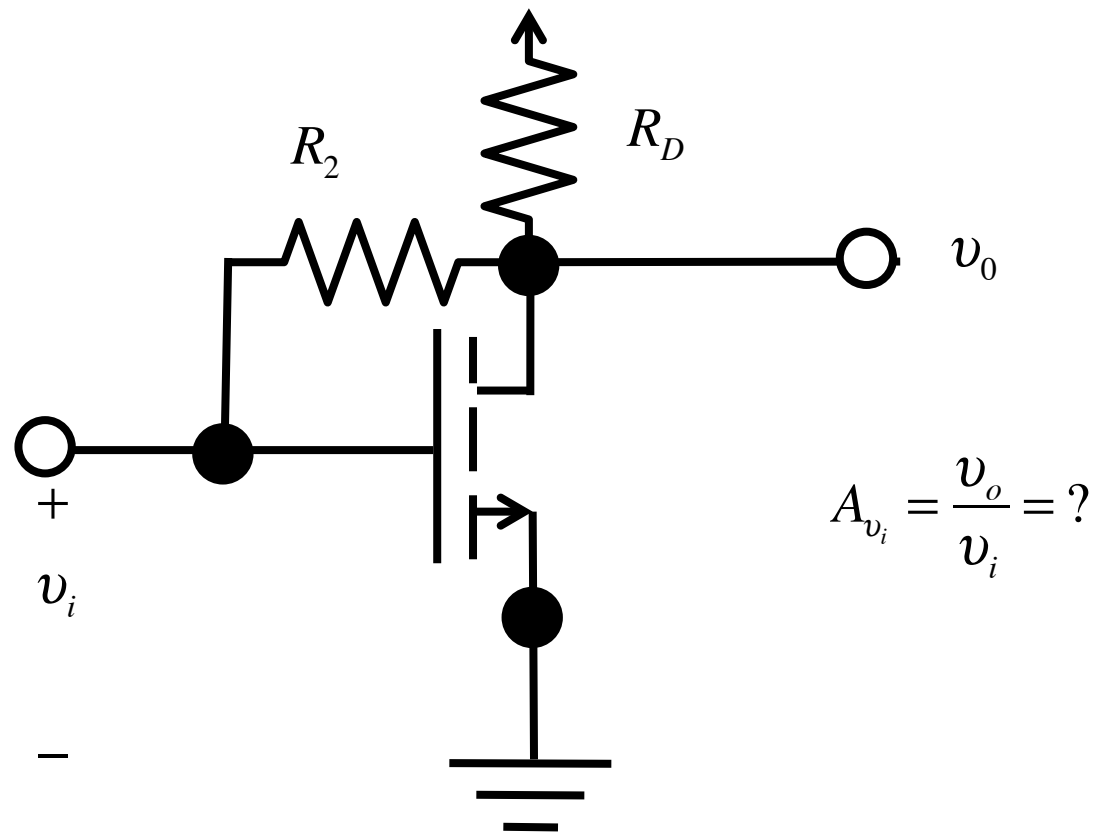
---





# Feedback amplifier

---



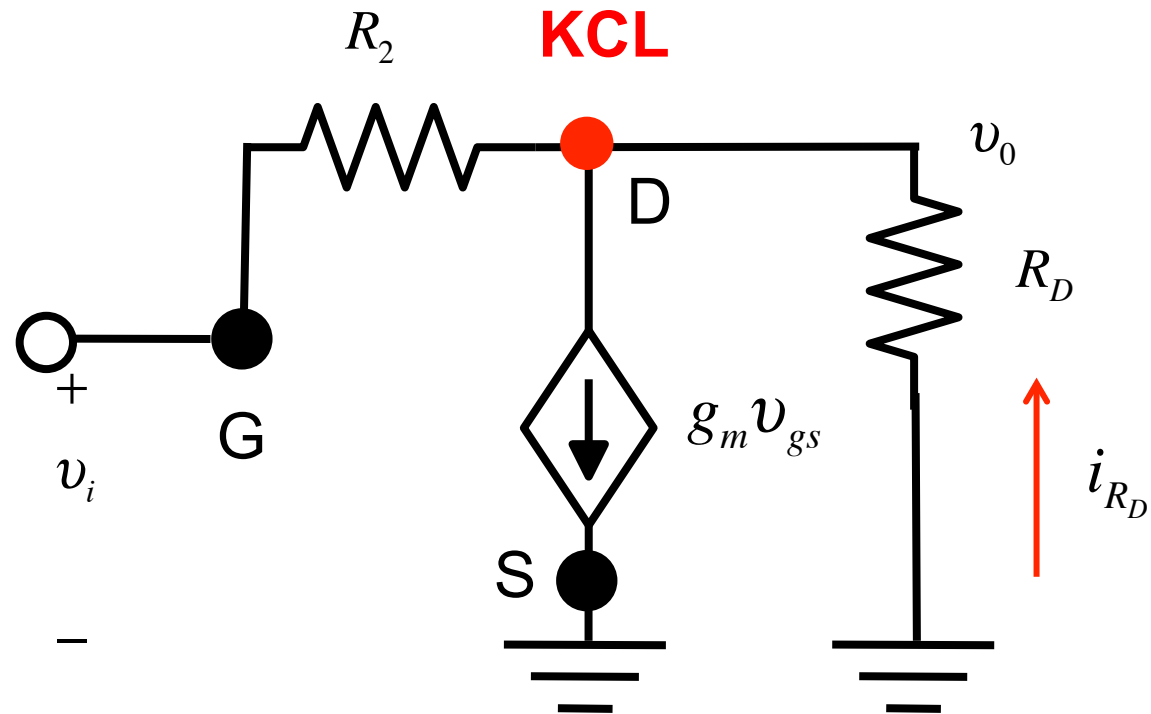
Intrinsic amplifier

## s.s. model

---

$$A_{v_o} = \frac{v_o}{v_i} = ?$$

$$v_o = -i_{R_D} R_D$$



# KCL

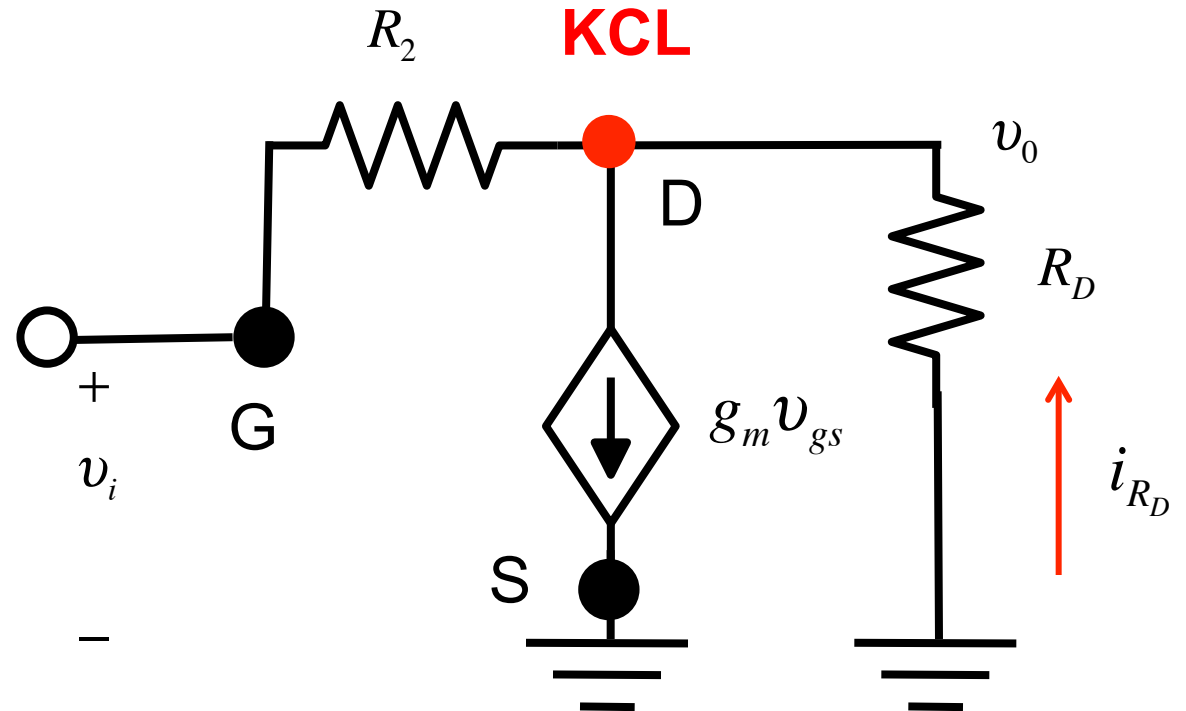
$$v_o = -i_{R_D} R_D$$

$$i_{R_D} = g_m v_{gs} + \frac{(v_o - v_i)}{R_2}$$

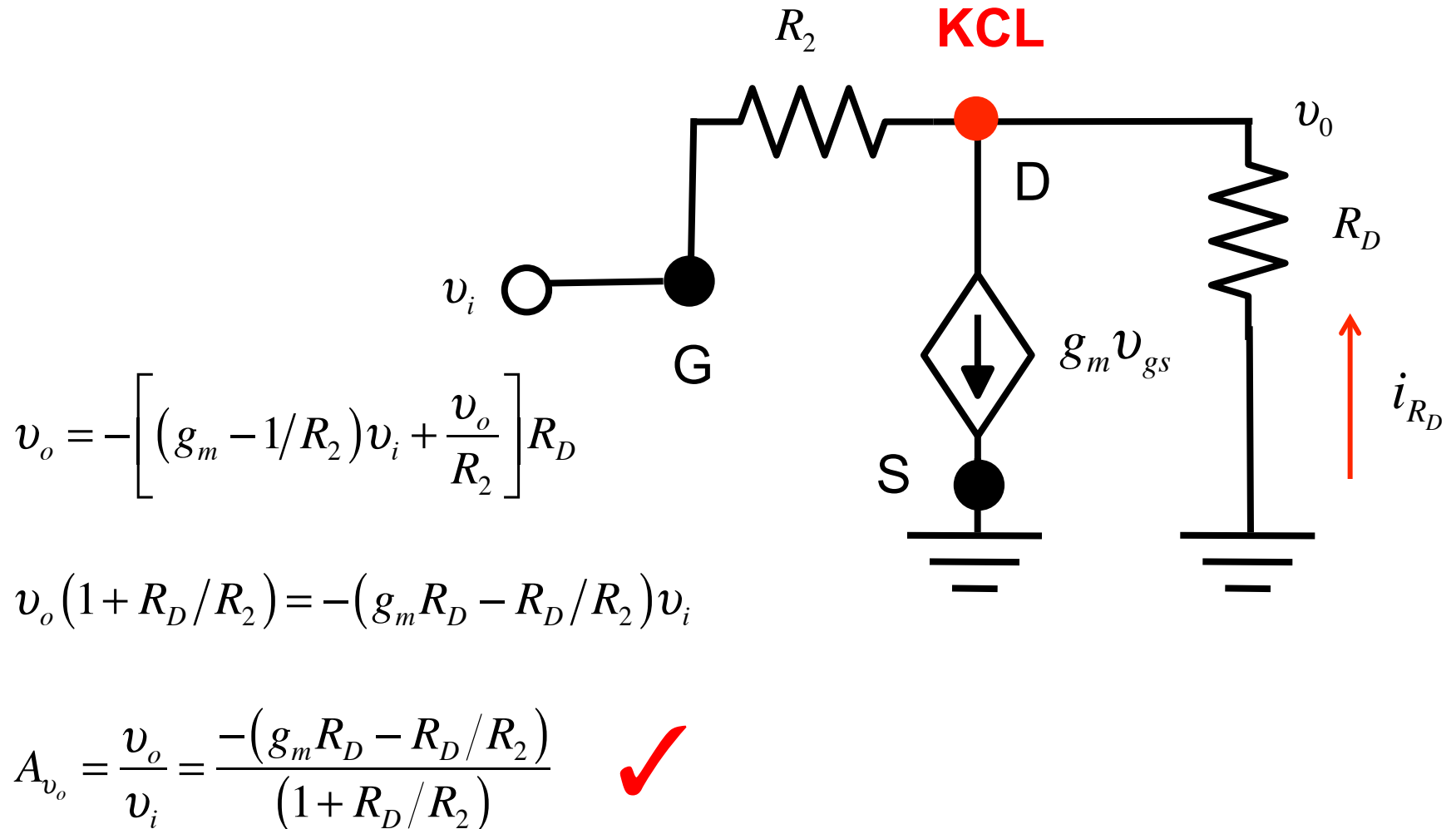
$$i_{R_D} = g_m v_i + \frac{(v_o - v_i)}{R_2}$$

$$i_{R_D} = (g_m - 1/R_2)v_i + \frac{v_o}{R_2}$$

$$v_o = -i_{R_D} R_D = -\left[ (g_m - 1/R_2)v_i + \frac{v_o}{R_2} \right] R_D$$



# Open circuit voltage gain



# Input resistance

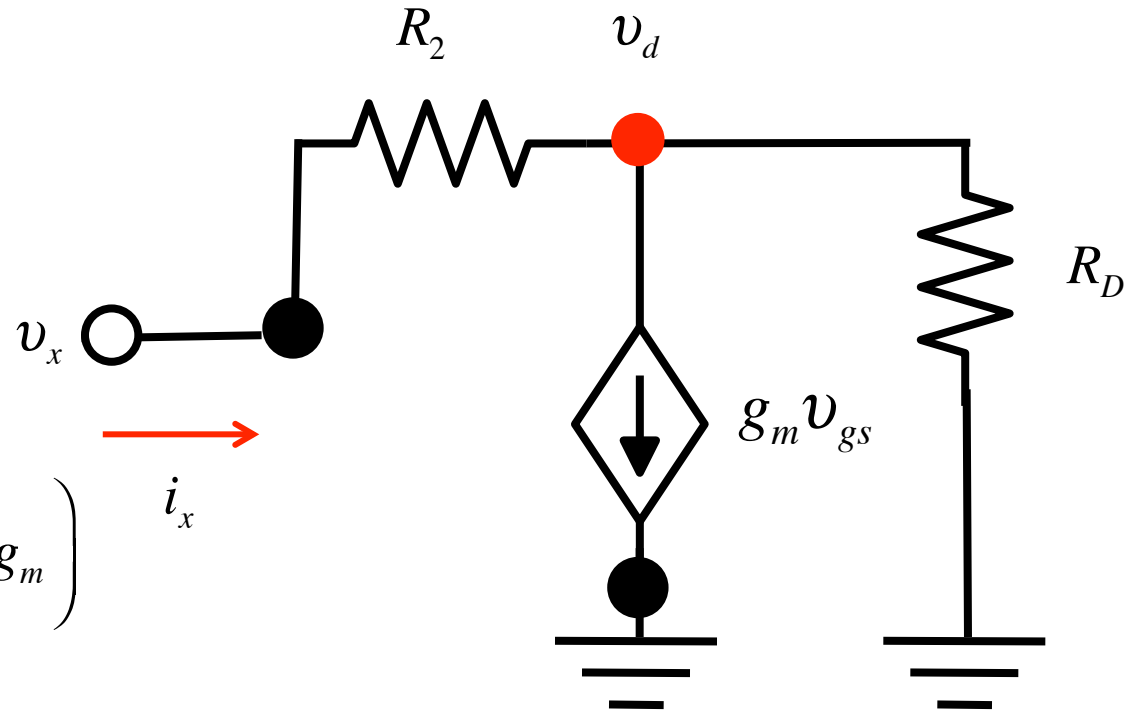
$$v_x = i_x R_2 + v_d \quad (1)$$

$$\frac{v_d - v_x}{R_2} + g_m v_x + \frac{v_d}{R_D} = 0$$

$$v_d \left[ \frac{1}{R_2} + \frac{1}{R_D} \right] = v_x \left( \frac{1}{R_2} - g_m \right) \quad i_x$$

$$v_d = v_x \frac{(1/R_2 - g_m)}{(1/R_2 + 1/R_D)} \quad \text{Return to (1)}$$

$$v_x = i_x R_2 + v_x \frac{(1/R_2 - g_m)}{(1/R_2 + 1/R_D)}$$



# Input resistance

---

$$v_x = i_x R_2 + v_x \frac{(1/R_2 - g_m)}{(1/R_2 + 1/R_D)}$$

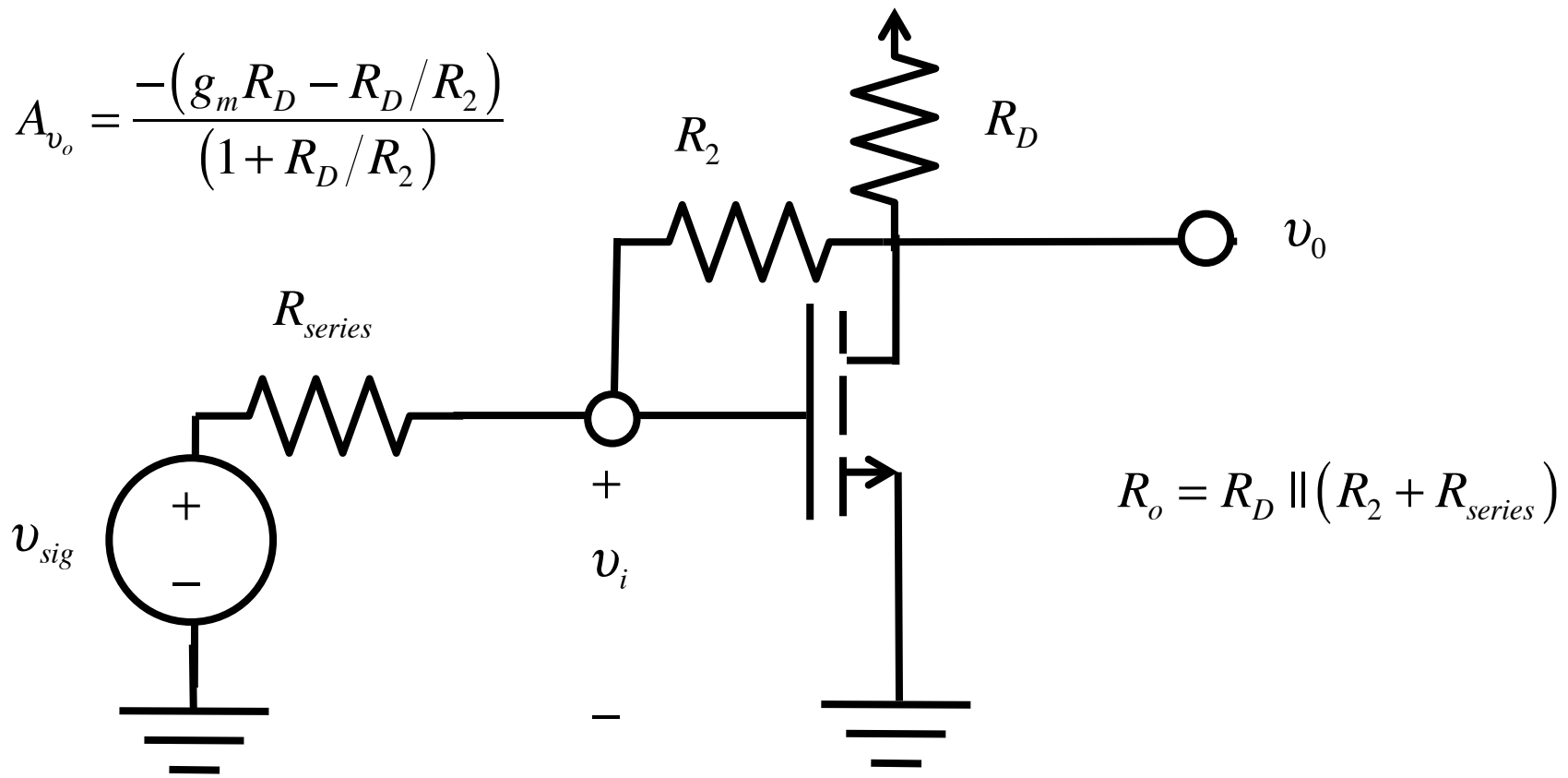
$$v_x \left[ 1 - \frac{(1/R_2 - g_m)}{(1/R_2 + 1/R_D)} \right] = i_x R_2$$

$$v_x \left[ \frac{(1/R_D + g_m)}{(1/R_2 + 1/R_D)} \right] = i_x R_2$$

$$\frac{v_x}{i_x} = R_{in} = \frac{(1 + R_2/R_D)}{(1/R_D + g_m)} \quad \checkmark$$

# Feedback amplifier

$$A_{v_o} = \frac{-(g_m R_D - R_D/R_2)}{(1 + R_D/R_2)}$$



$$R_o = R_D \parallel (R_2 + R_{series})$$

$$R_{in} = \frac{(1 + R_2/R_D)}{(1/R_D + g_m)}$$

# Summary

---

The 4-resistor bias circuit can be used to make discrete transistor CS, CG, CD, CE, CB, and CC amplifiers.

Using the hybrid- $\pi$  small signal model for transistors, we can analyze the performance of **any** amplifier.



# Discrete Amplifiers

---

- 1) 4-resistor bias circuits
- 2) Common Source
- 3) Common Gate
- 4) Common Drain
- 5) Amplifier analysis examples

