Spring 2019 Purdue University

ECE 255: L22

MOS Current Mirrors and Basic Gain Cell

(Sedra and Smith, 7th Ed., Secs. 8.1-8.3)

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Announcements

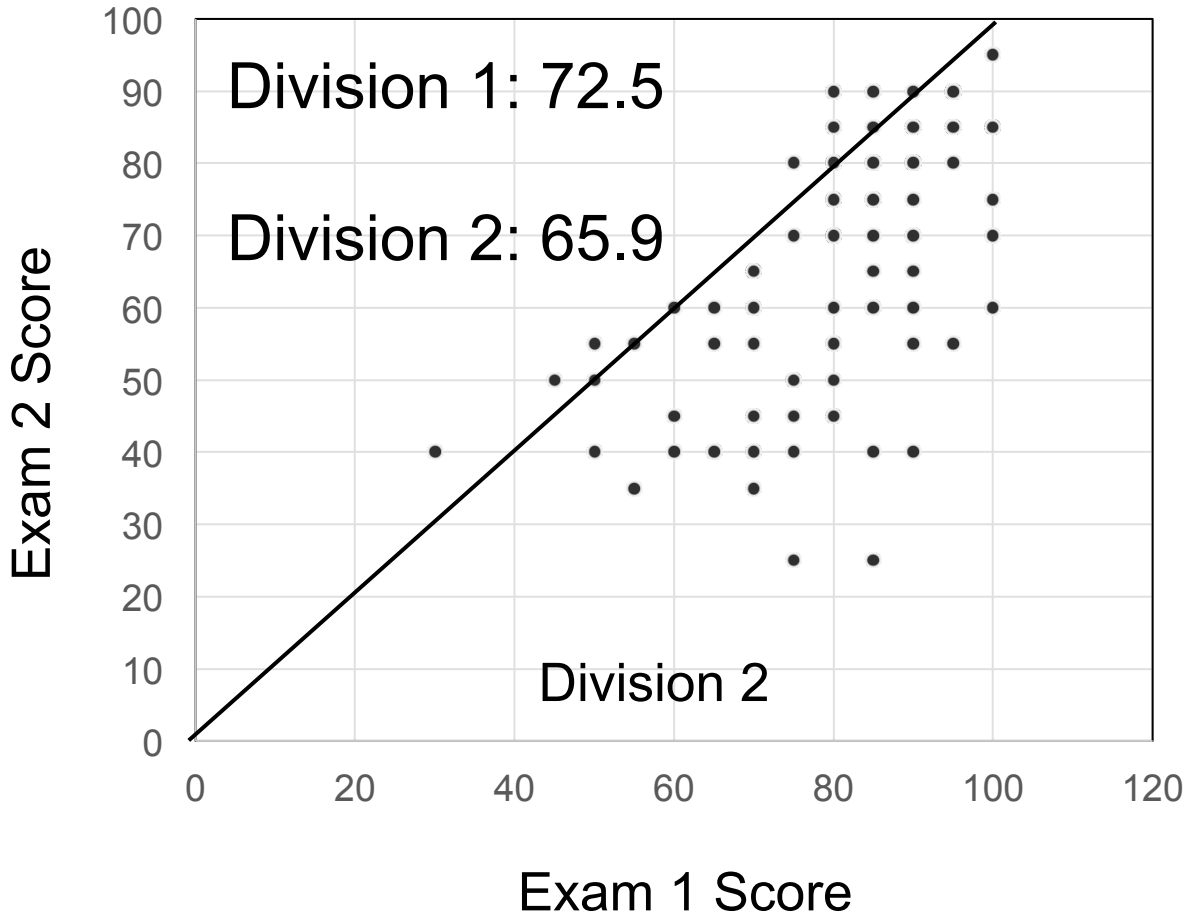
1) HW7 due at 5:00 PM Friday, March 22

2) HW8 due at 5:00 PM Friday, March 29

3) Exam 3 is at 6:30 PM, Tuesday, April 2

4) Spice Project 2 will be due on April ?.

Exam 2 Results



Google Official: on “ideal recruits”

"There is no single set of discrete skills one can learn that will last an entire career in high-tech," Johnson writes. Instead, "**ideal recruits are creative, adaptable and autonomous, and they have achieved a deep understanding of core subjects such as math, physics and computer science** that make it possible to have a razor-sharp intuition and an ability to assimilate new subjects and technologies quickly, without even the expectation of being trained; they train themselves on the skills du jour as the need arises and with minimum help or structure.”

Bruce Johnson, the Atlanta site and engineering director for Google, in the Atlanta Journal-Constitution (12/23/11).

Steven Chu on learning science:

"Learning science is not about learning what a person did. You have to do that, but to really absorb it, you have to turn it around and cast it in a form **as if you invented it yourself**. You try to internalize it in such a way that it really becomes intuitive."

Muhammad Ali:

"I hated every minute of training, but I said, 'Don't quit. Suffer now and live the rest of your life as a champion."

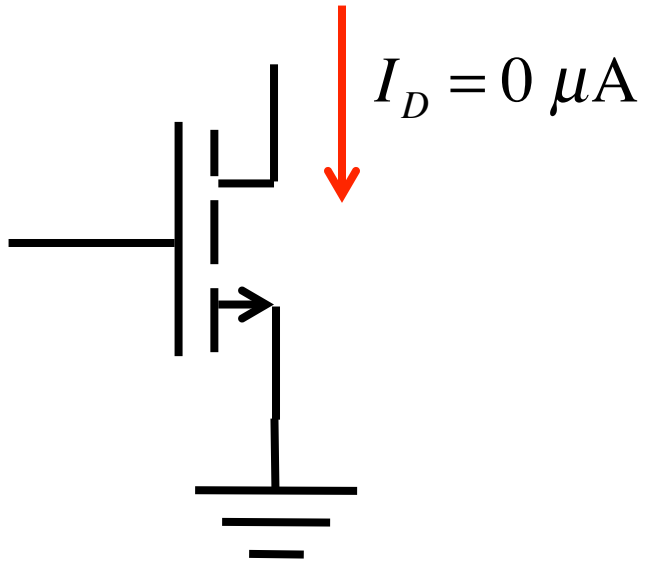
-Muhammad Ali

http://www.brainyquote.com/quotes/quotes/m/muhammadal148629.html.

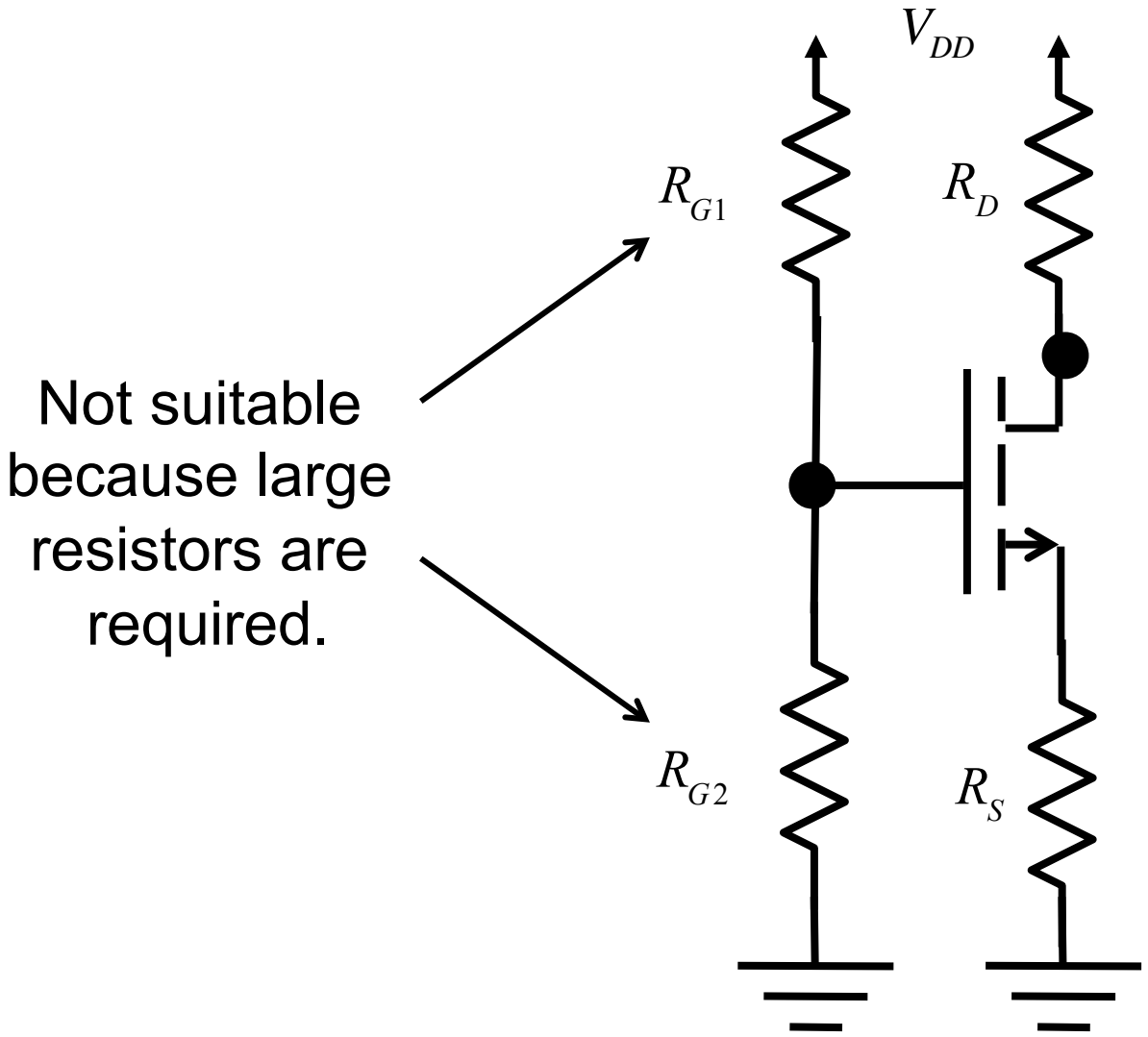
IC Amplifiers

For the rest of the course, we will shift our focus to integrated circuit electronics.

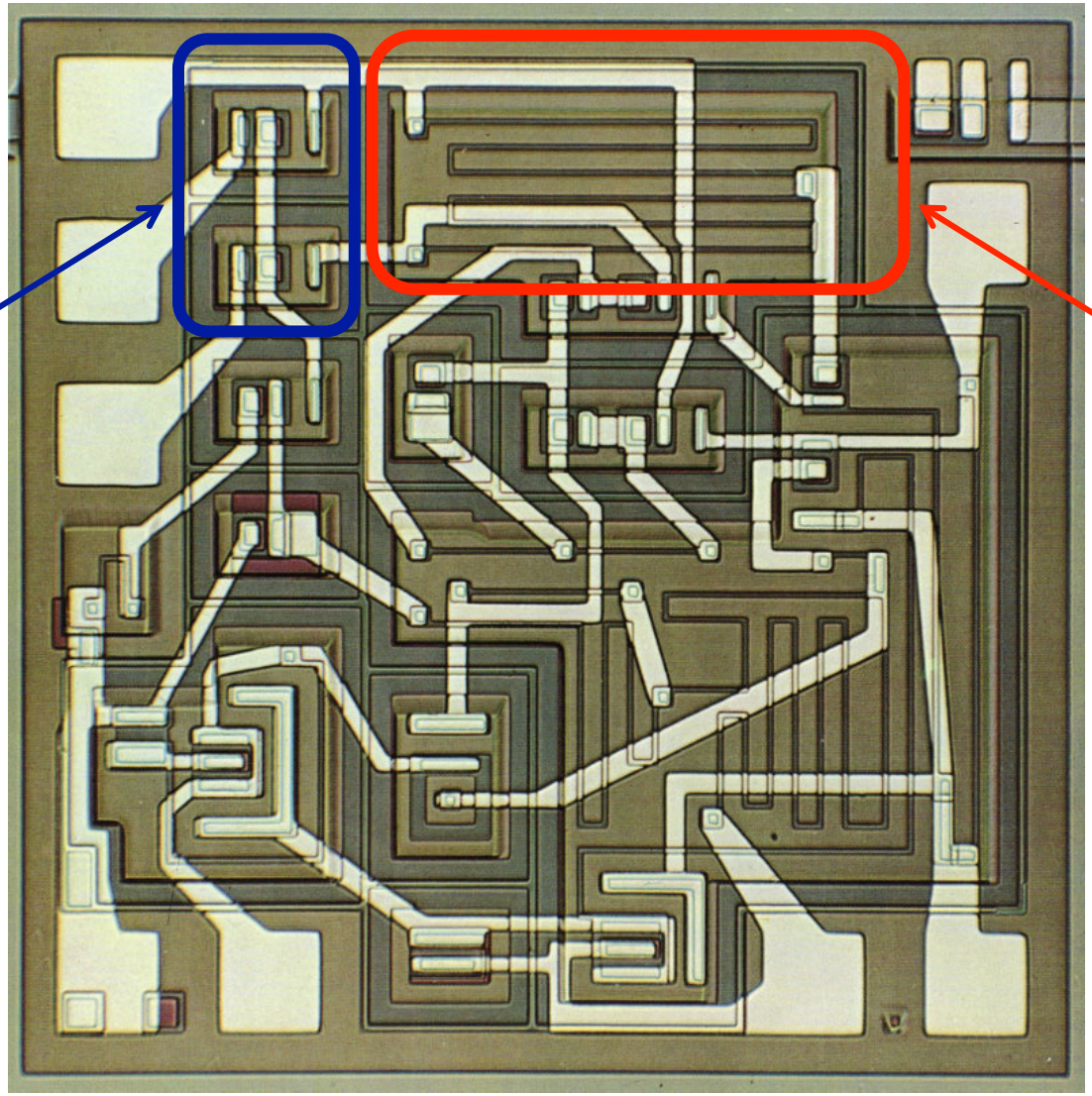
First question: How do we bias a MOSFET when it's on an a Si chip?



Classic 4-resistor bias circuit



Why avoid large resistors?



2 transistors

2 resistors

μA 709 op amp
Designed by
Robert Widlar

http://www.computerhistory.org/revolution/digital-logic/12/281

Principles of IC Design

1) Avoid large or moderate value resistors

2) Avoid large capacitors (but small ones, pF or less, are fine)

3) Use low voltage power supplies

4) Exploit the ability to “size” transistors (W/L for MOSFETs, A_E for bipolar)

5) Use CMOS unless bipolar is essential

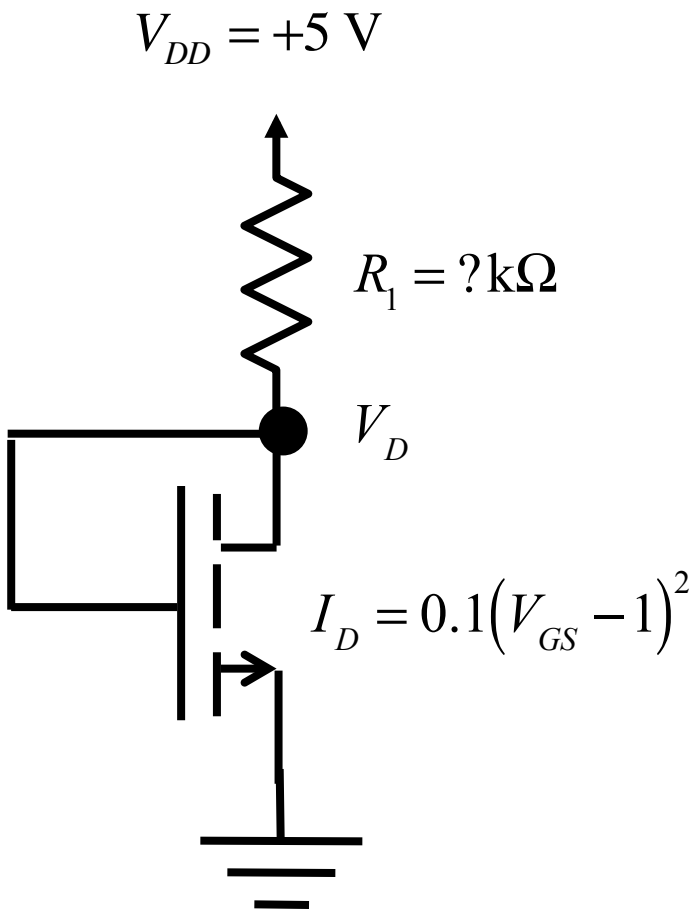
Outline

1) Introduction

2) MOS Current Mirrors

3) CS Amplifiers with Active Loads

Review: MOSFET DC Design



Design for: $I_D = 0.5\,\text{mA}$

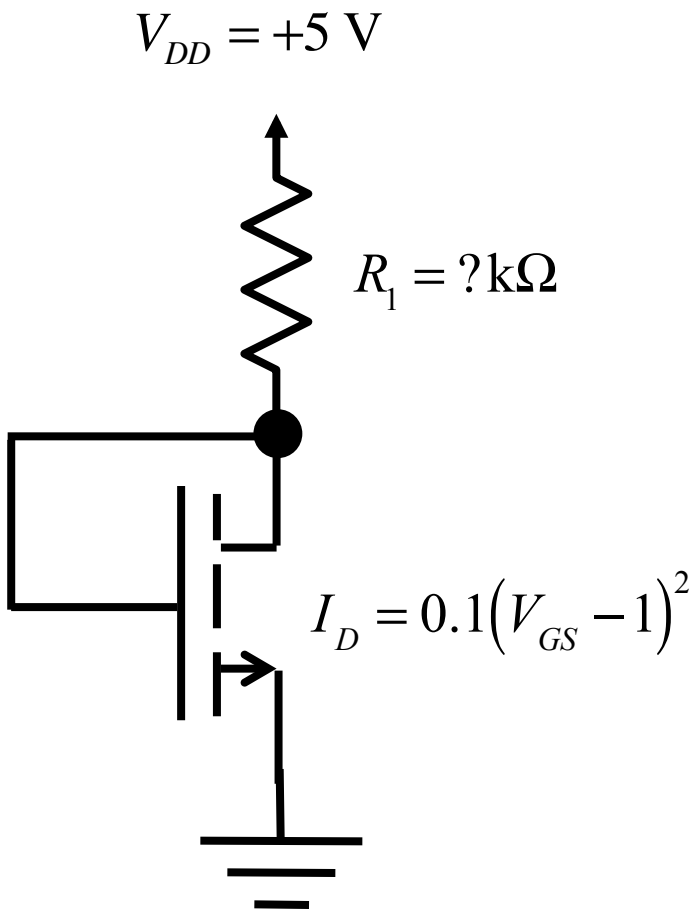
What region is this MOSFET operating in?

Is $V_{DS} \geq \left(V_{GS} - V_{tn}\right)$

$V_D \geq \left(V_D - 1\right)$ ✓

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

Review: MOSFET DC Design



Design for: $I_D = 0.5$ mA

$$I_D = 0.1\left(V_{GS} - 1\right)^2$$

$$0.5 = 0.1\left(V_{GS} - 1\right)^2$$

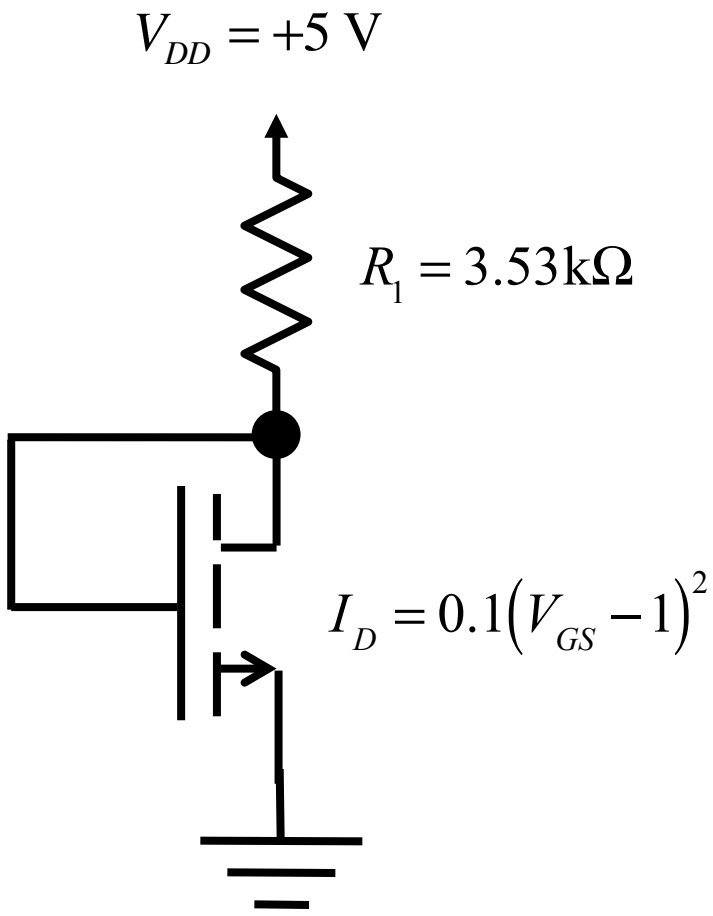
$$V_{GS} = 3.24 \text{ V}$$

$$V_{GS} = V_D = 3.24 \text{ V}$$

$$R_1 = \frac{5 - 3.24}{0.5} = 3.53\,\text{k}\Omega$$

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

Review: MOSFET DC **Analysis**



$$I_D = ?\ \text{mA}$$

$$I_D = 0.1\left(V_{GS} - 1\right)^2$$

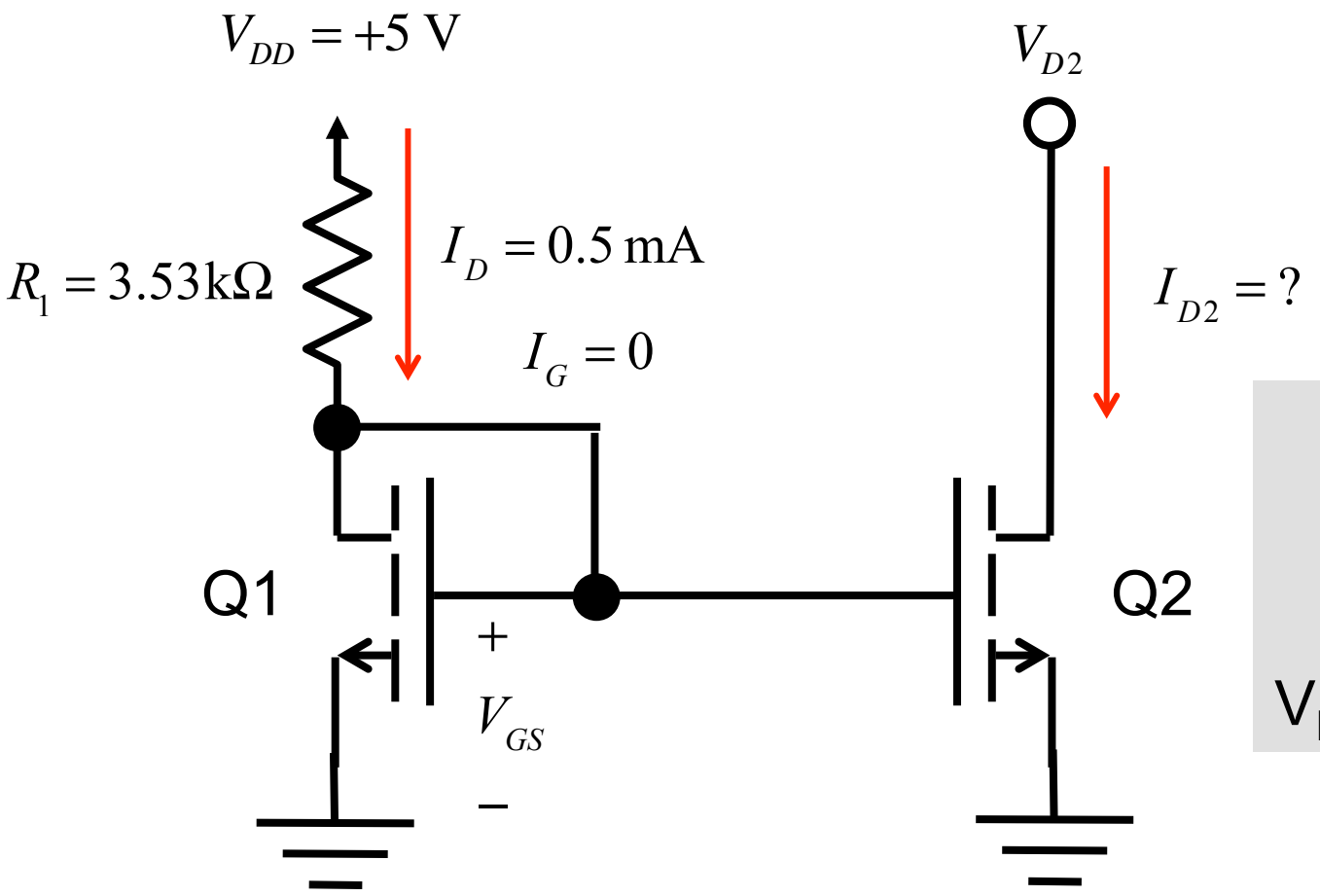
$$V_{GS} = V_{DD} - I_D R_1$$

2 equations in 2 unknowns

Solve quadratic eqn.

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

MOSFET “current mirror”



$I_{D2} = I_{D1}$

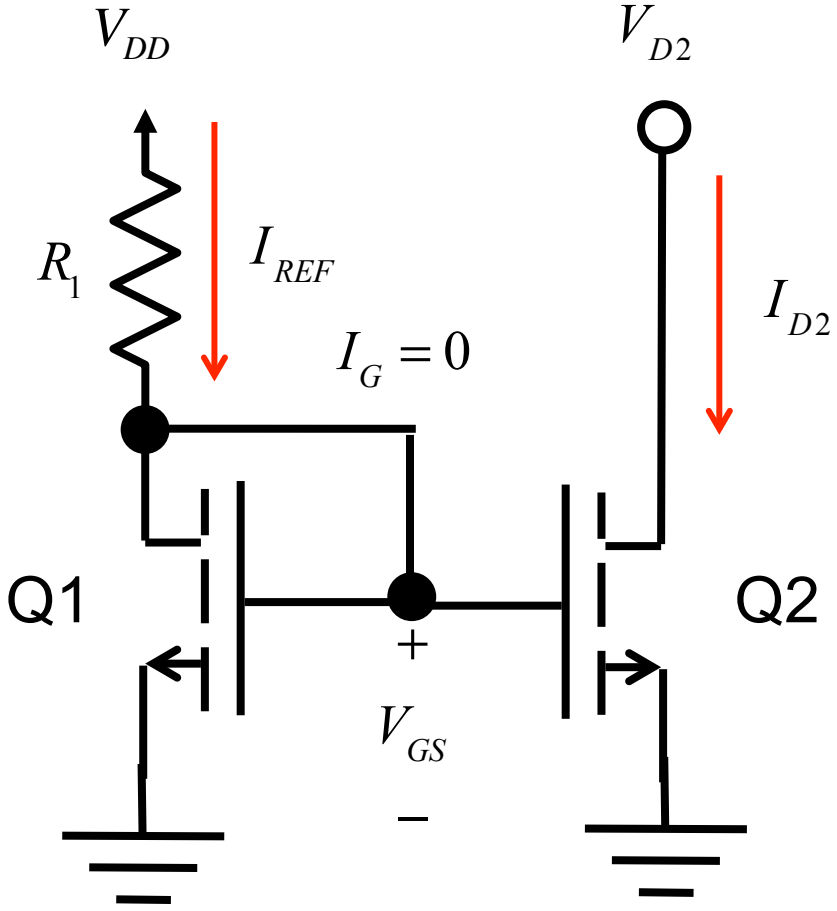
if

$V_{D2} > V_{GS} - V_{tn}$

$$I_D = 0.1\left(V_{GS} - 1\right)^2$$

$$I_D = 0.1\left(V_{GS} - 1\right)^2$$

MOSFET “current mirror”



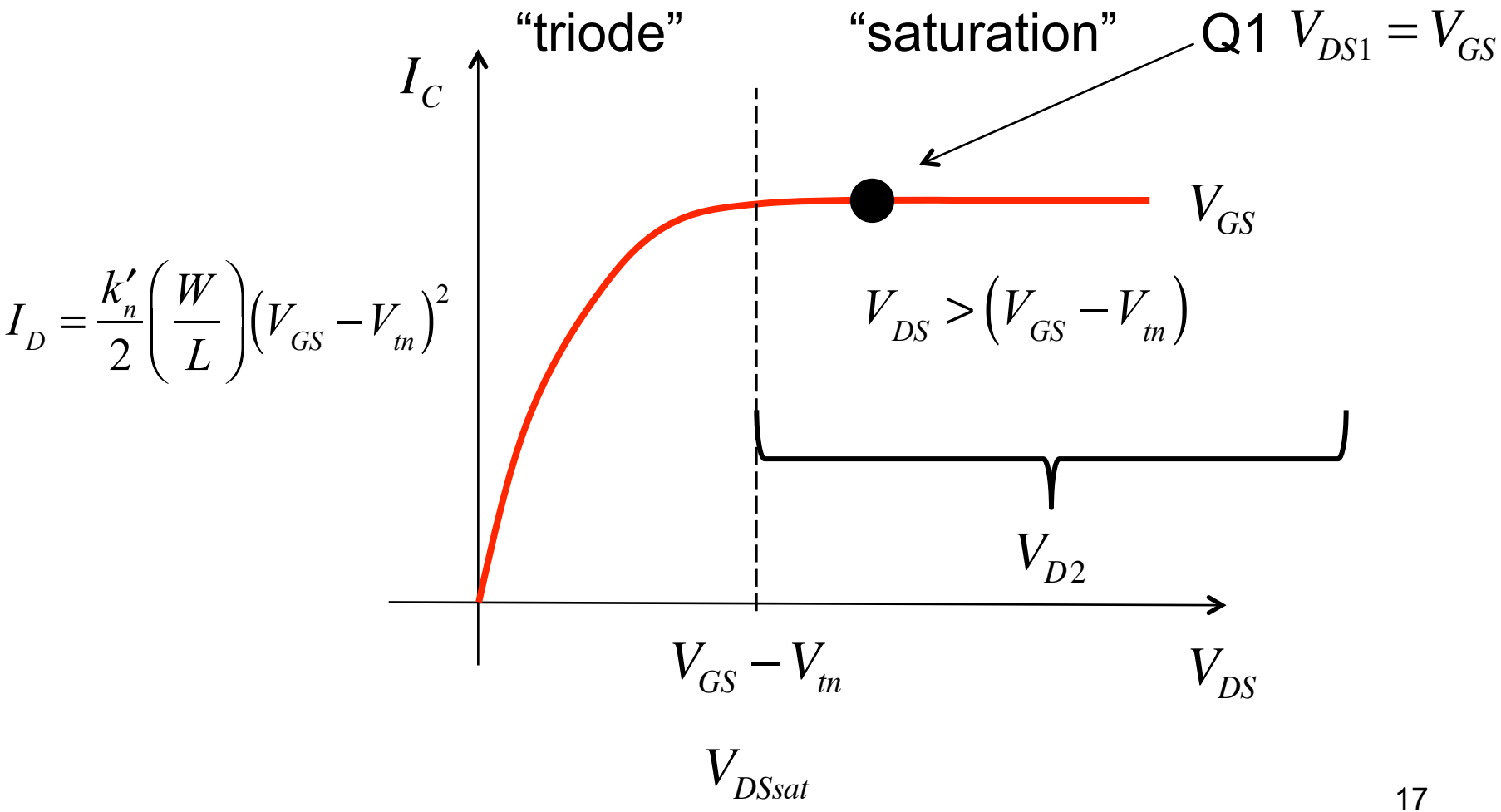
$$\frac{I_{D2}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

$$\left(V_{D2} > V_{GS} - V_{tn}\right)$$

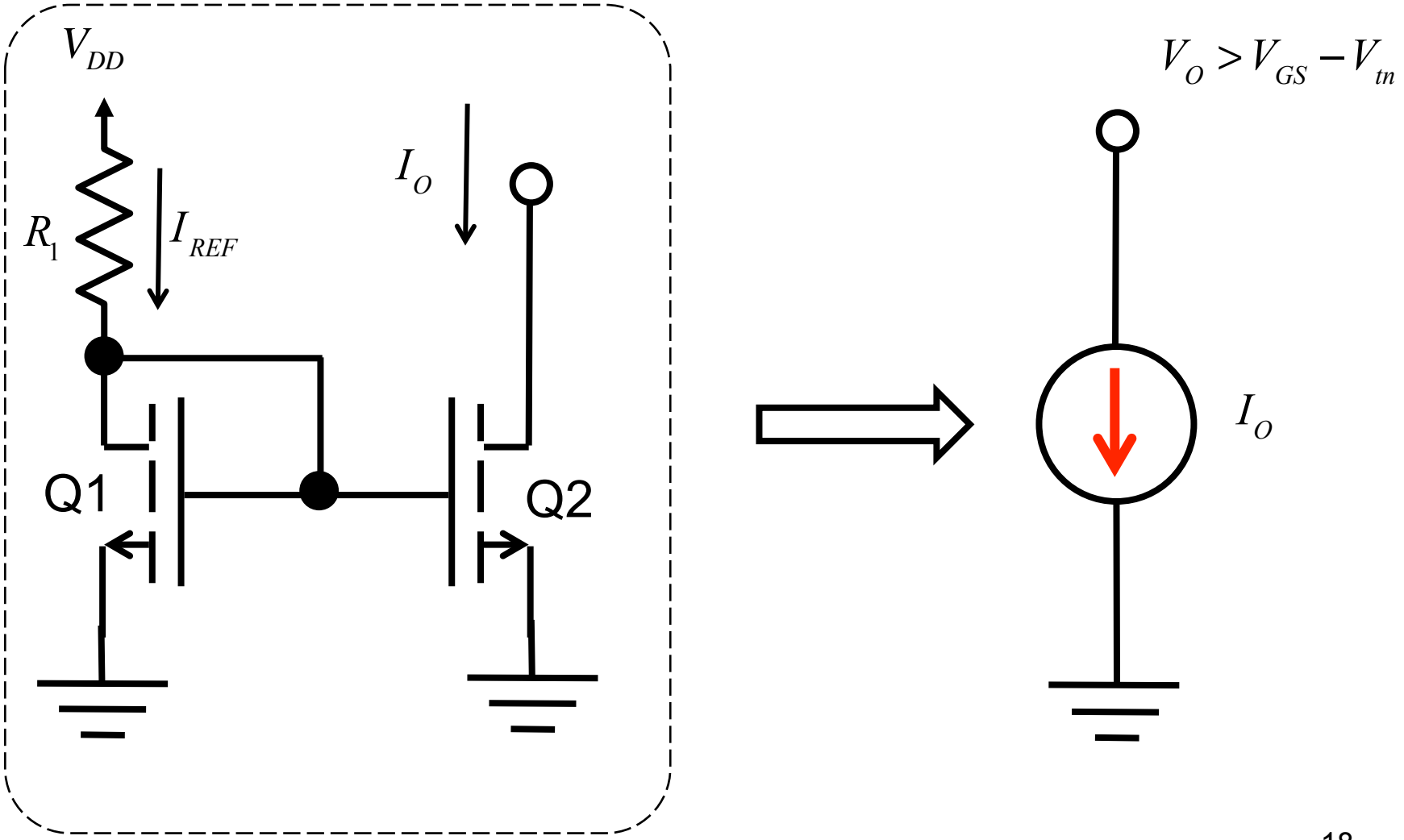
Now, let’s look more closely at the effect of V_{D2}.

$$I_{D1} = \frac{k'_n}{2}\left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{tn}\right)^2 \qquad I_{D2} = \frac{k'_n}{2}\left(\frac{W}{L}\right)_2 \left(V_{GS} - V_{tn}\right)^2$$

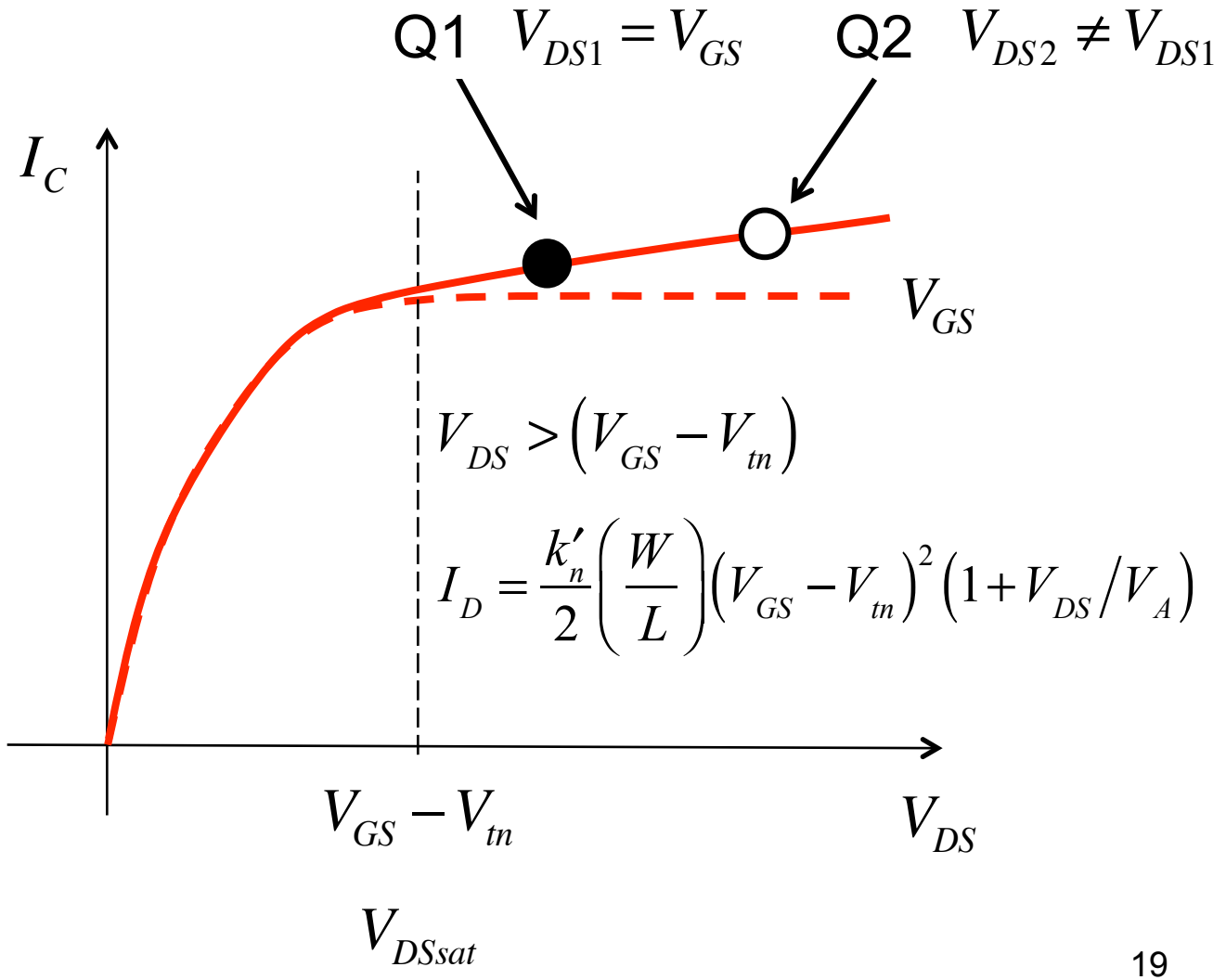
MOSFETs


"triode"
"saturation"
Q1 $V_{DS1} = V_{GS}$
I_C
V_{GS}
$I_D = \frac{k'_n}{2}\left(\frac{W}{L}\right)\left(V_{GS} - V_{tn}\right)^2$
$V_{DS} > \left(V_{GS} - V_{tn}\right)$
V_{D2}
$V_{GS} - V_{tn}$
V_{DS}
V_{DSsat}

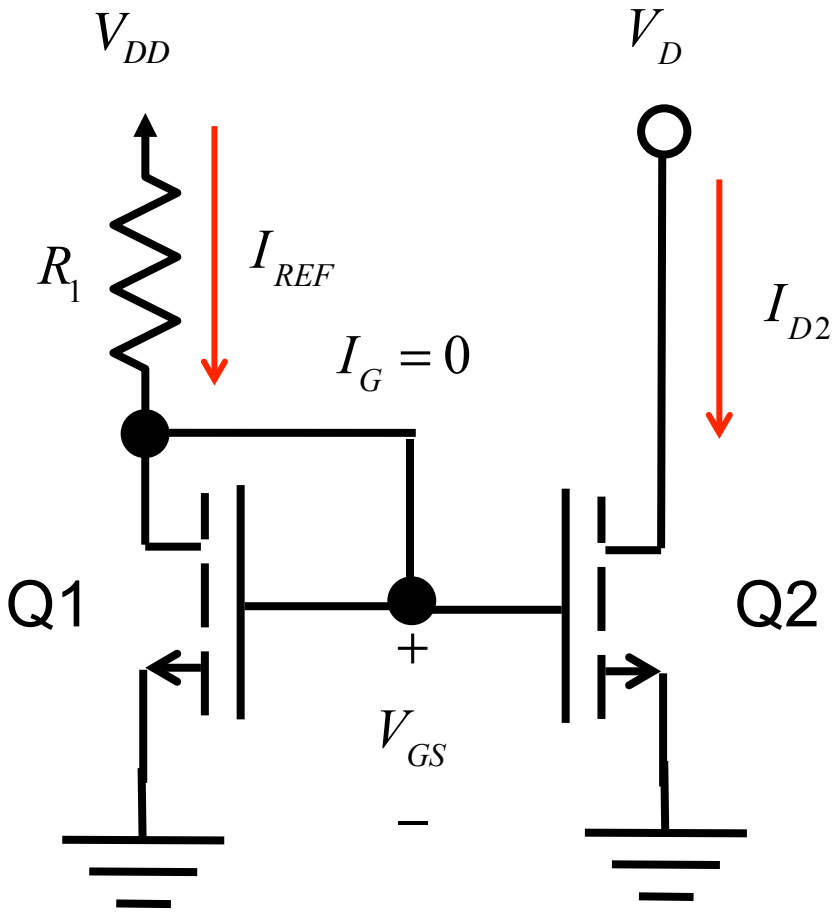
MOSFET current source



MOSFETs with output conductance



Real MOSFET current mirror



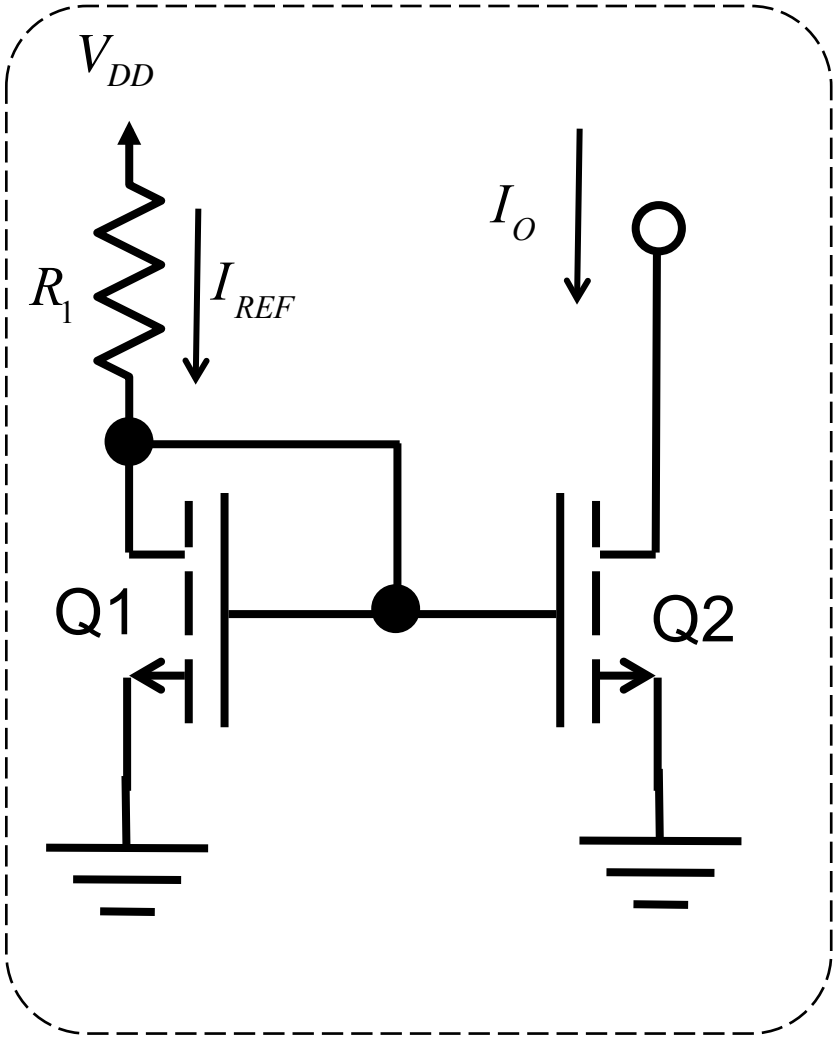
$$I_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)\left(V_{GS} - V_{tn}\right)^2\left(1 + V_{DS}/V_A\right)$$

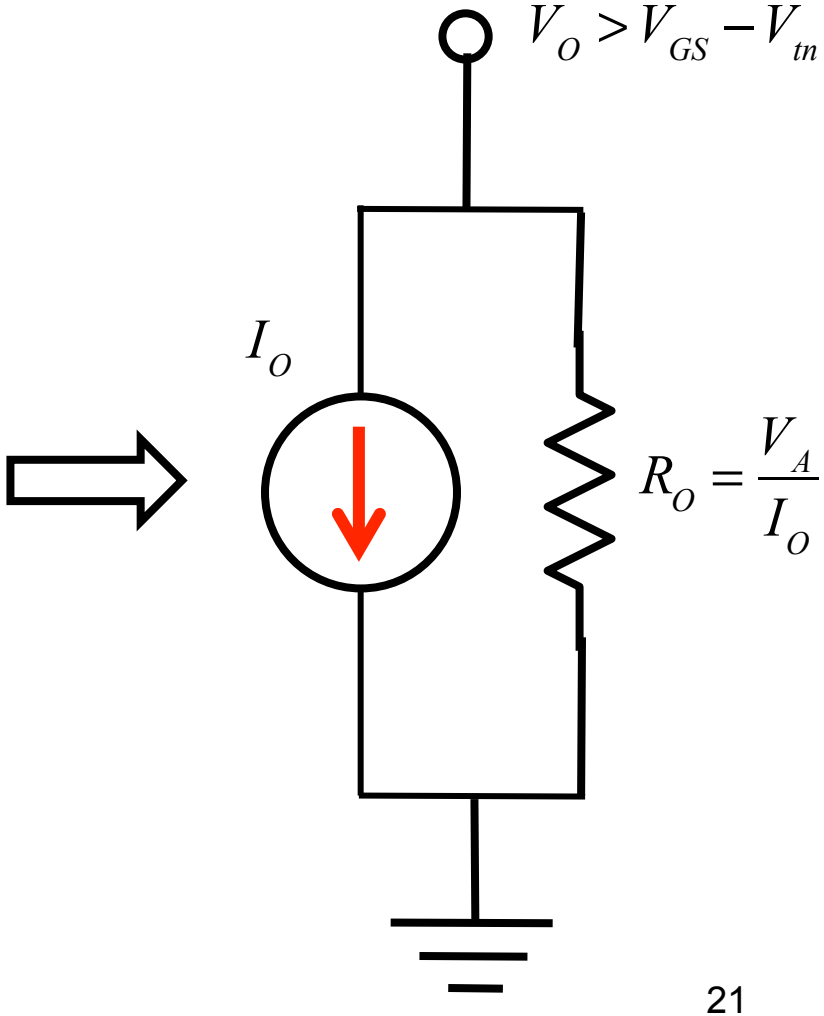
$$I_{D1} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_1\left(V_{GS} - V_{tn}\right)^2\left(1 + V_{GS}/V_{A1}\right)$$

$$I_{D2} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_2\left(V_{GS} - V_{tn}\right)^2\left(1 + V_{D2}/V_{A2}\right)$$

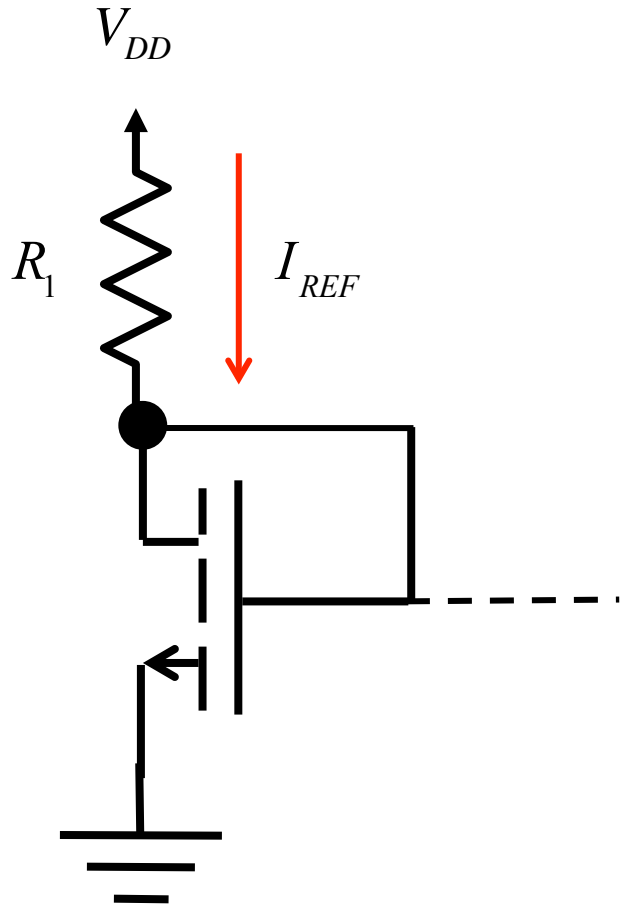
$$\frac{I_{D2}}{I_{REF}} = \frac{\left(W/L\right)_2}{\left(W/L\right)_1}\frac{\left(1 + V_{D2}/V_{A2}\right)}{\left(1 + V_{GS}/V_{A1}\right)}$$

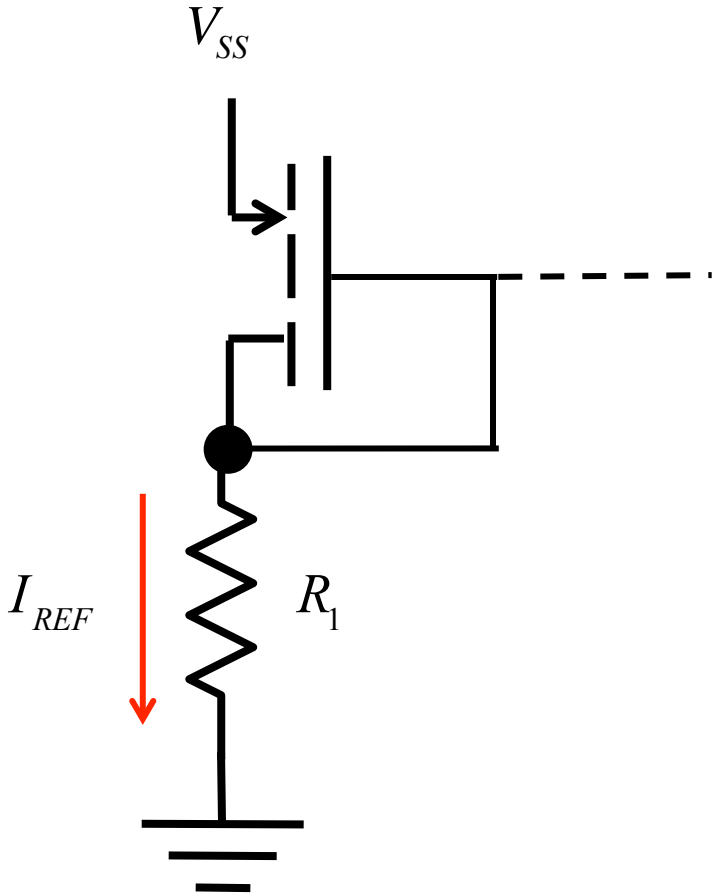
RealMOSFET current source





NMOS vs. PMOS

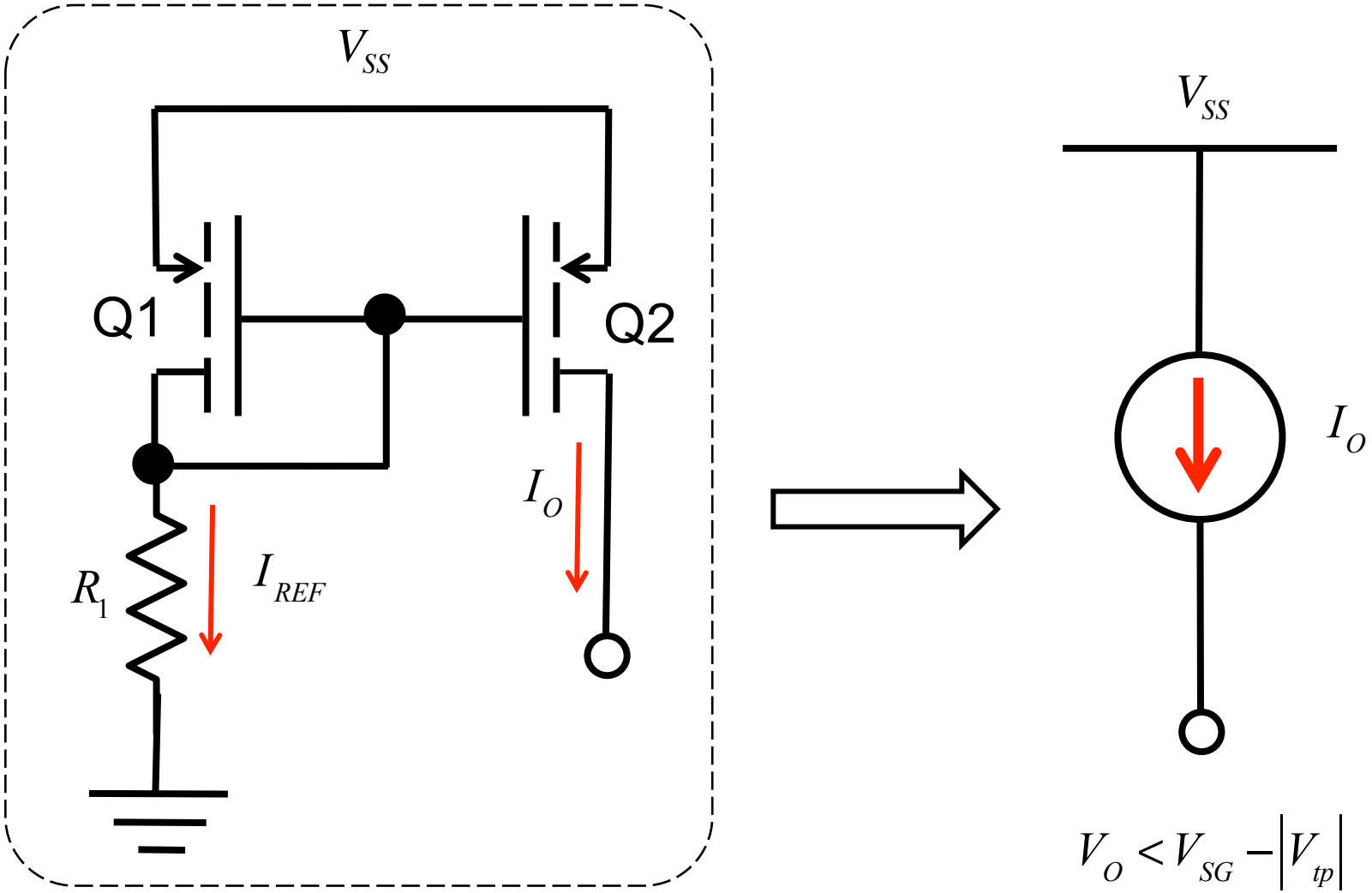




$$I_D = \frac{k'_n}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

$$I_D = \frac{k'_p}{2}\frac{W}{L}\left(V_{SG} - \left|V_{tp}\right|\right)^2$$

PNP MOSFET current source



$$V_O < V_{SG} - |V_{tp}|$$

Current Mirror Comments

Many sophisticated current mirror / current source circuits exist (e.g. to maximize output resistance).

See: Sedra and Smith 7th Ed. Sec. 8.6

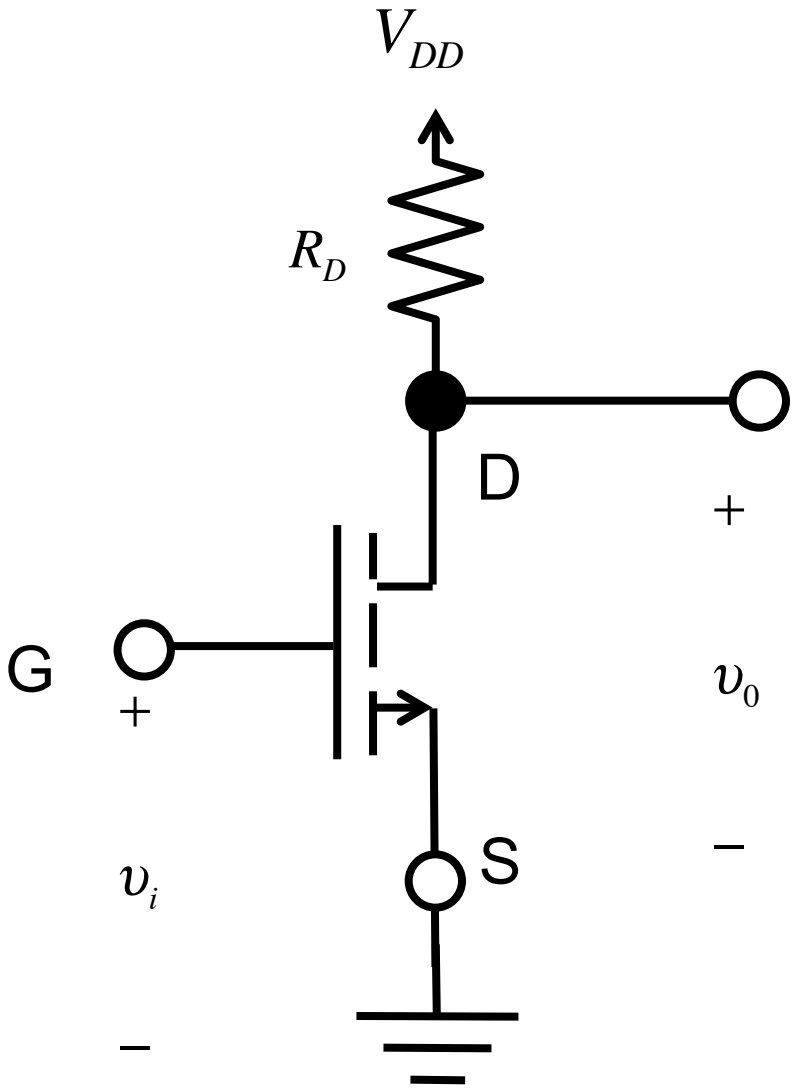
Outline

1) Introduction

2) MOS Current Mirror

3) CS Amplifiers with Active Loads

Common Source amplifier



$$A_{\upsilon_o} = \frac{\upsilon_o}{\upsilon_i} = -g_m R_D$$

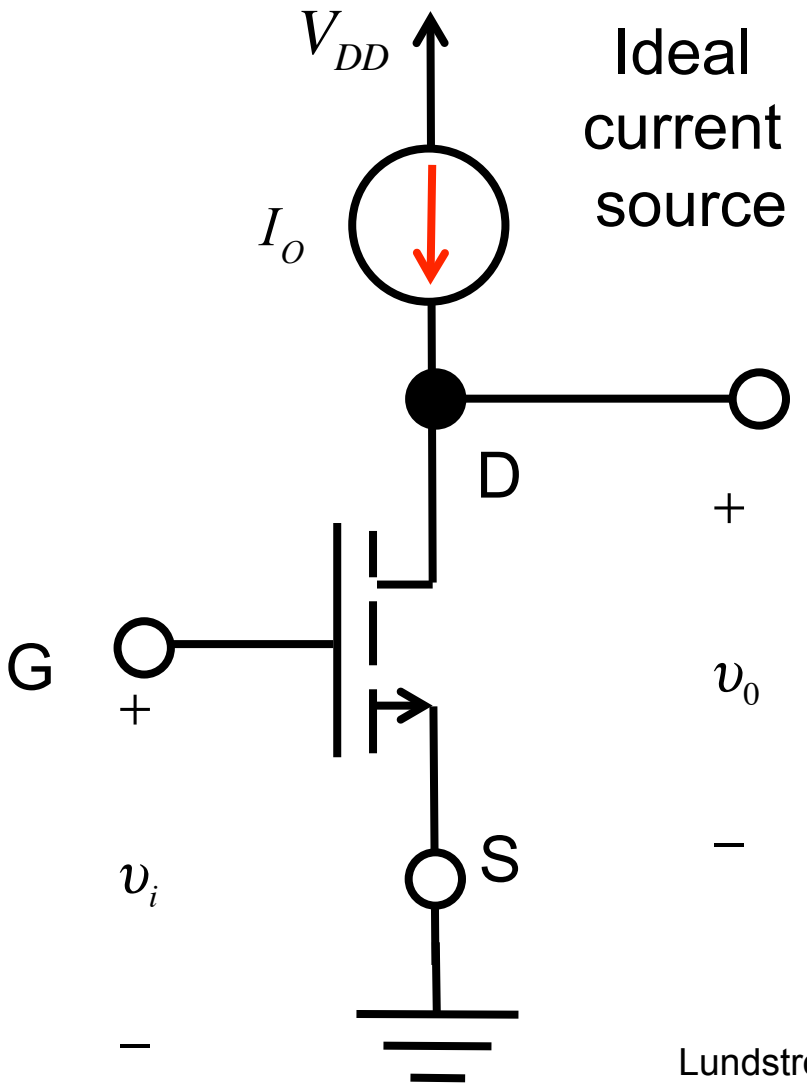
$$R_{in} = \infty$$

$$R_o = R_D$$

MOSFETs have modest g_m, so we need a very large drain resistor.

Two problems: ?

Basic IC gain cell



Ideal current source

$R_O = \infty$

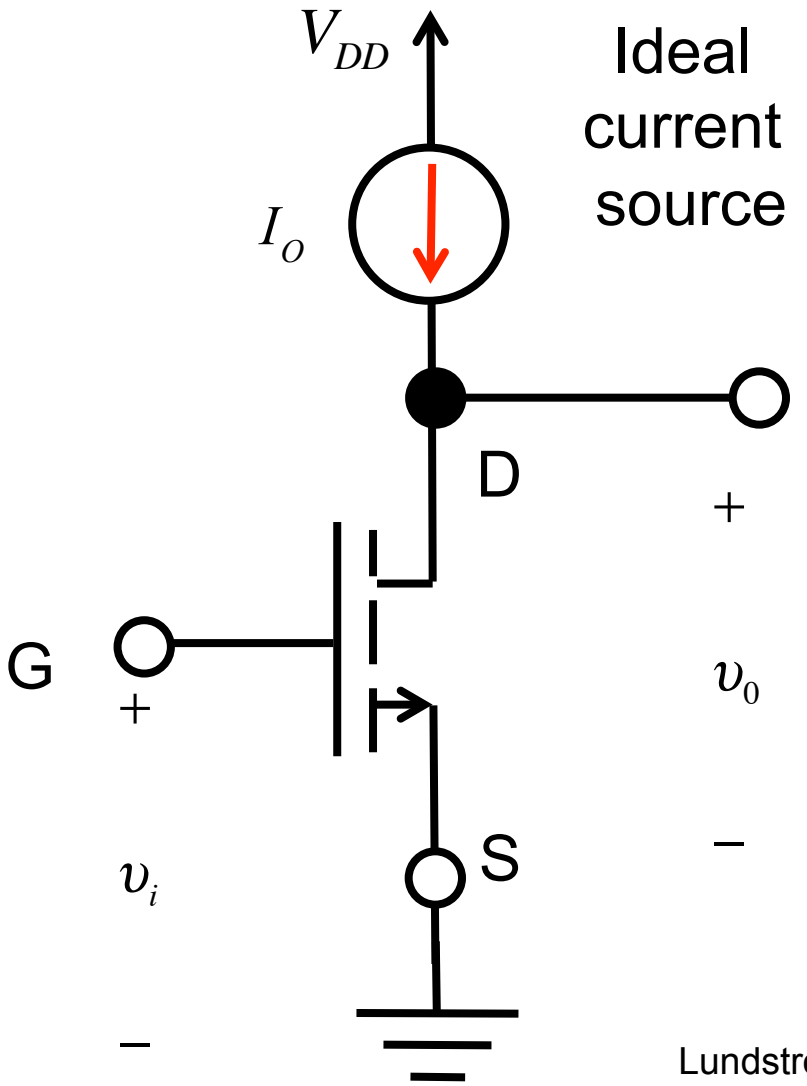
$$A_{\upsilon_o} = \frac{\upsilon_o}{\upsilon_i} = -g_m r_o$$

$$R_{in} = \infty$$

$$R_o = r_o$$

Draw s.s. circuit to see this

Maximum gain ("intrinsic gain" / "self gain")



Ideal current source

$R_O = \infty$

$$A_{\upsilon_o} = -g_m r_o$$

$$A_0 = \left|A_{\upsilon_o}\right| = g_m r_o$$

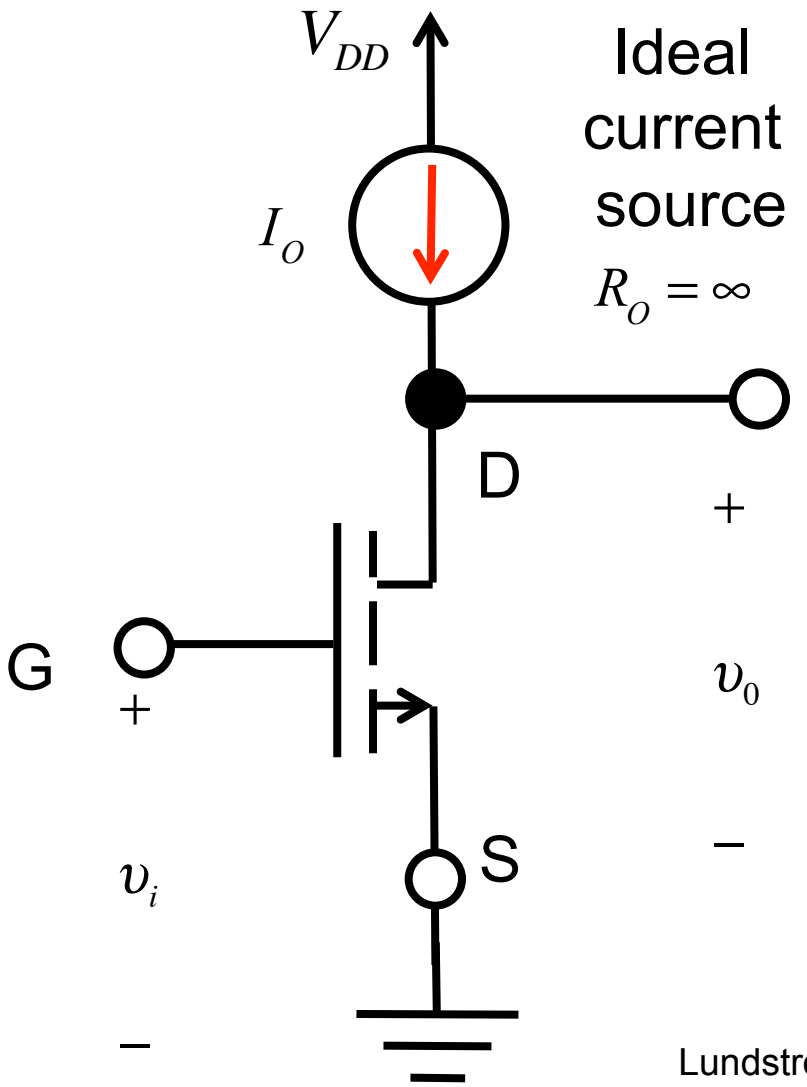
$$g_m = \frac{I_D}{\left(V_{GS} - V_{tn}\right)/2}$$

$$g_m = \sqrt{2k_n I_D}$$

$$r_o = \frac{V_A}{I_D}$$

$$V_A = V_A' L \propto L$$

Maximum (intrinsic/self) gain



$$A_0 = \frac{V_A}{(V_{GS} - V_{tn})/2} = \frac{V'_A L}{(V_{GS} - V_{tn})/2}$$

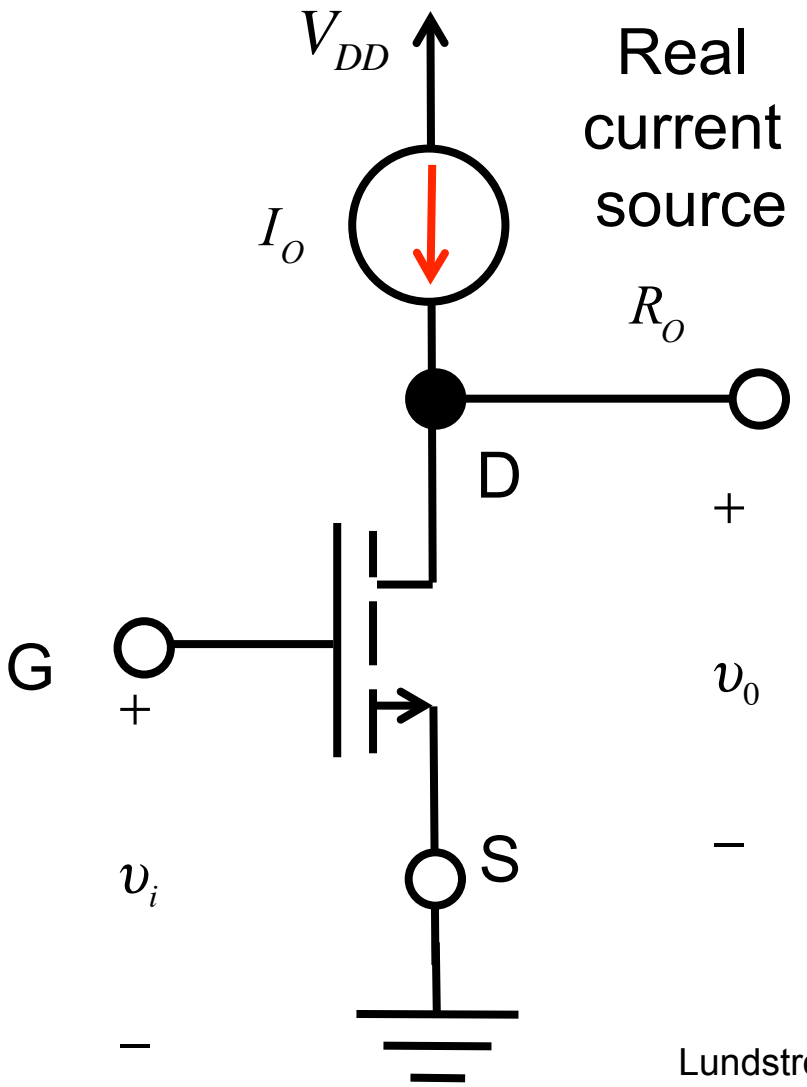
$$A_0 = \frac{V_A}{\sqrt{2k_n I_D}} = \frac{V'_A L}{\sqrt{2k_n I_D}}$$

Low currents and long channels give high gain

But, they give low transconductance and bandwidth

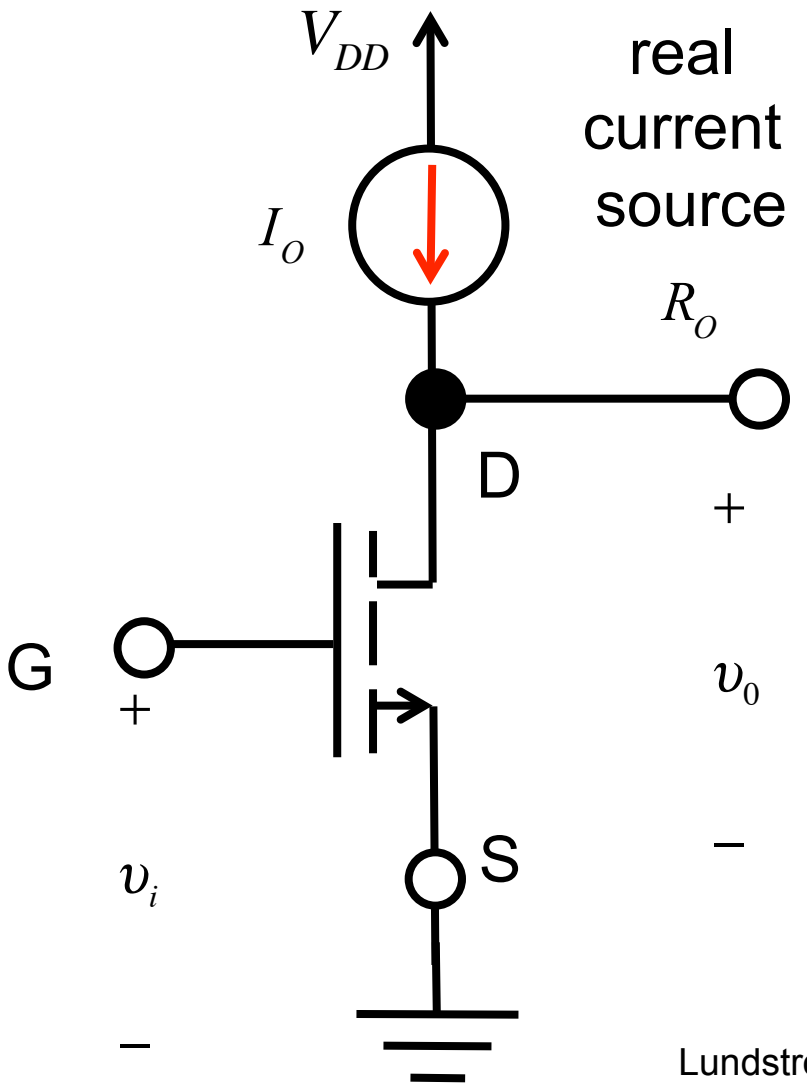
$$10 < A_0 < 40$$

Non-ideal current source



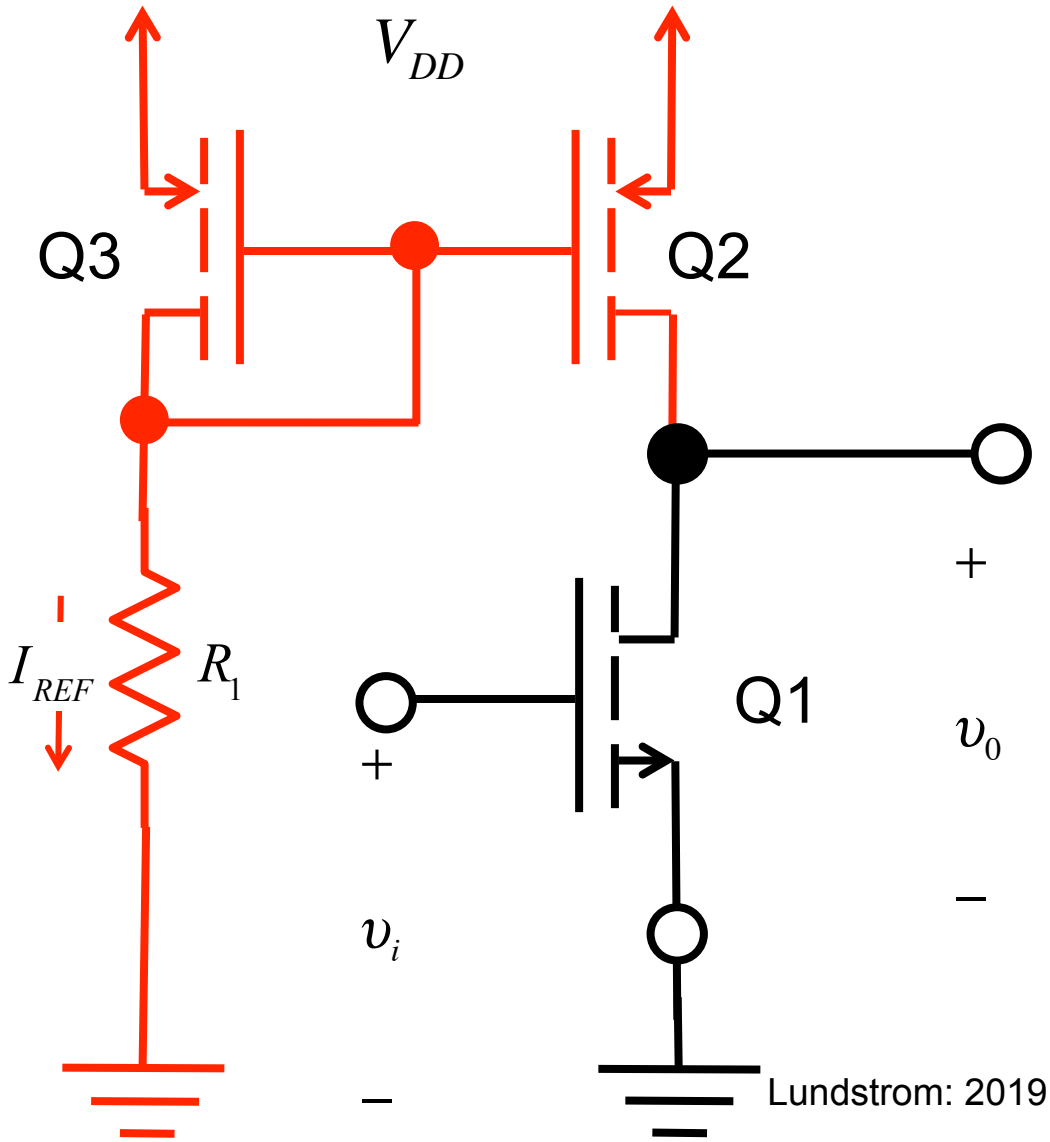
$$A_{\upsilon_o} = -g_m\left(r_o \,\|\, R_O\right)$$

Implementation



How do we implement the current source?

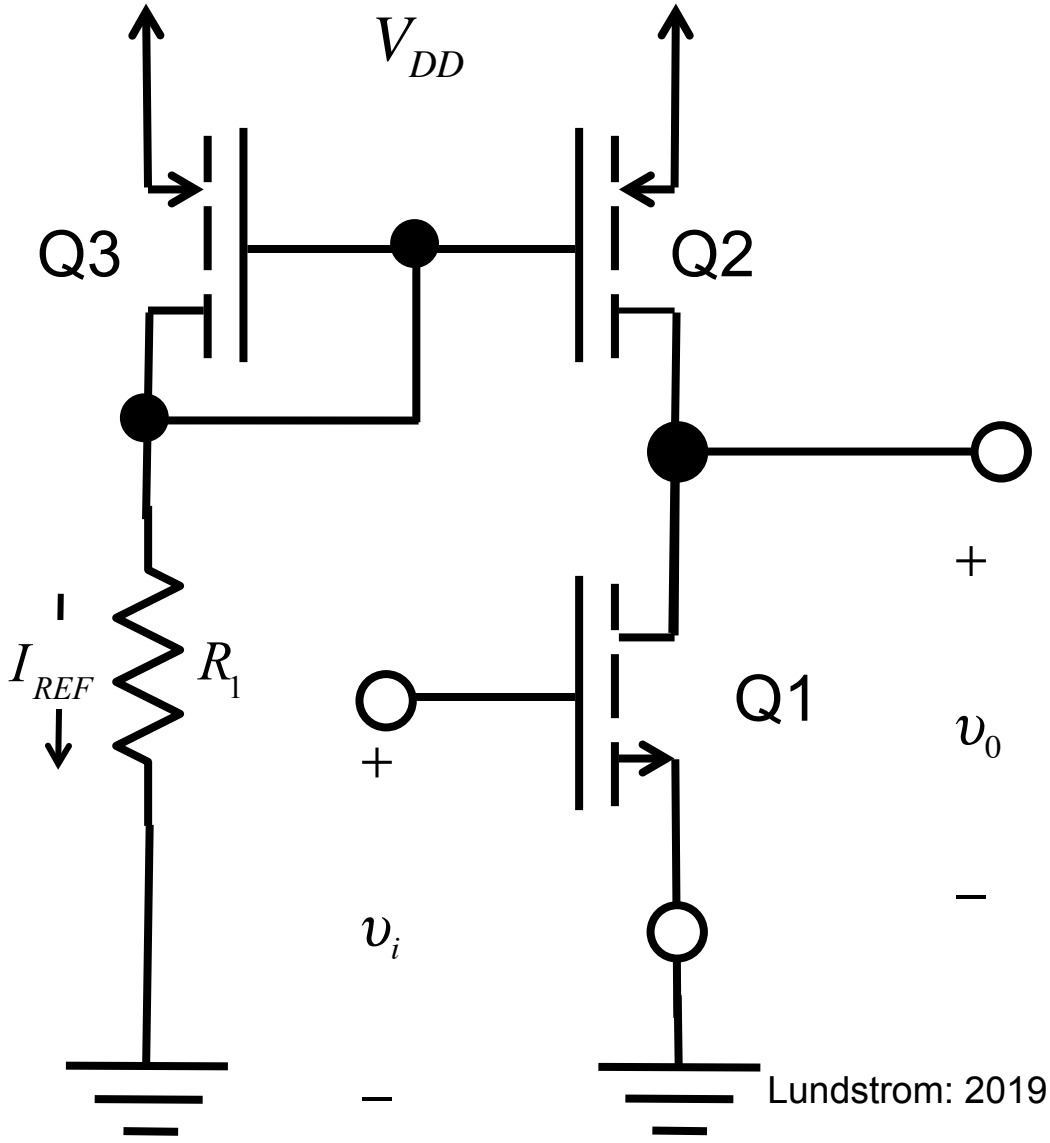
Implementation



$$A_{\upsilon_o} = -g_m\left(r_{oN} \parallel r_{oP}\right)$$

$$A_0 \approx (10-40)/2$$

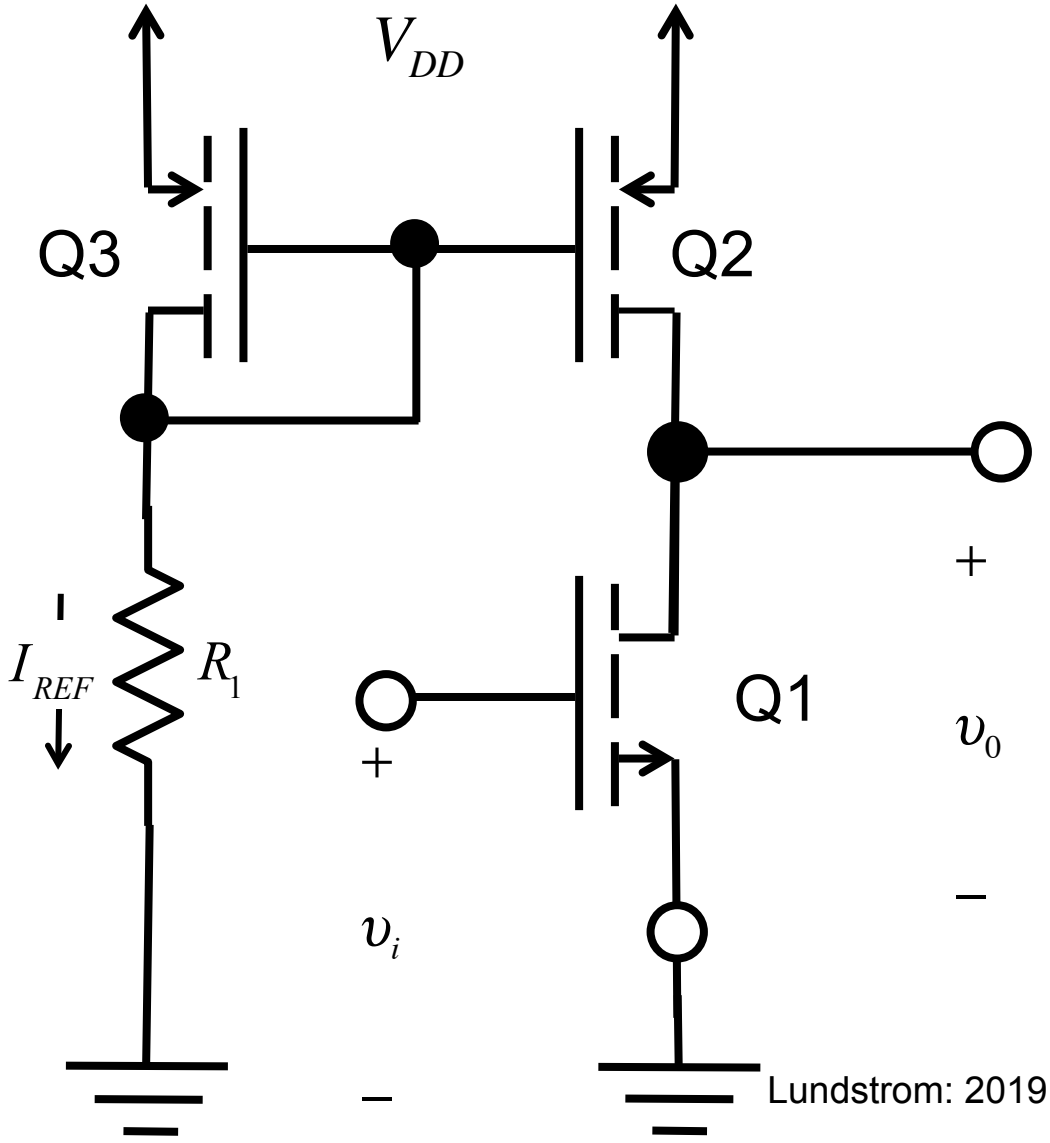
Implementation



$$A_{\upsilon_o} = -g_m\left(r_{oN} \parallel r_{oP}\right)$$

Question:
How would we design this circuit for a gain of 5?

Implementation



$$A_{\upsilon_o} = -g_m\left(r_{oN} \parallel r_{oP}\right)$$

$$A_0 \approx (10-40)/2$$

Question:
How can we increase the gain of the basic cell?

Answer: Cascode

Summary

Current mirrors are used extensively in analog IC design.

The basic common source amplifier suffers from low gain when implemented in Si. A solution must be found.

Current Mirrors and Basic Gain Cell

1) Introduction

2) MOS Current Mirror

3) CS Amplifiers with Active Loads