Spring 2019 Purdue University

ECE 255: L23

BJT Current Mirrors, Self-Gain and CB/CG Reprise

Sedra and Smith
Sec. 8.2, 8.3 (7th Ed.)

School of ECE
Purdue University
West Lafayette, IN USA

PURDUE UNIVERSITY

Announcements

A1:

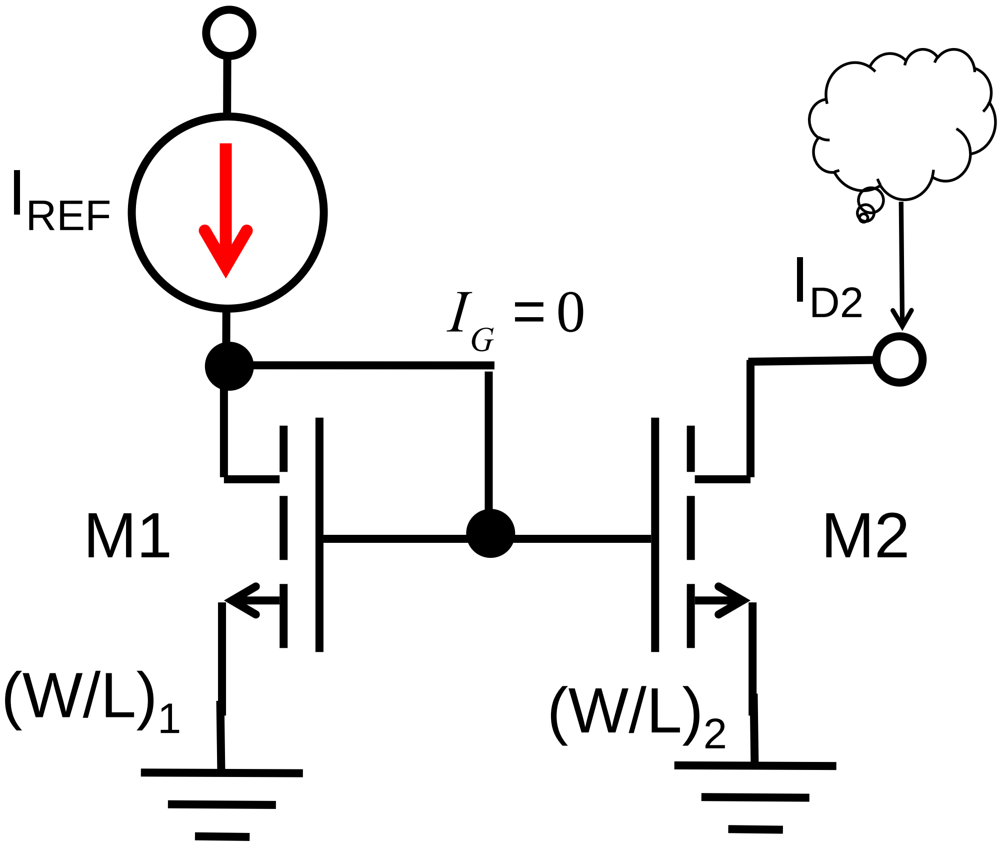
Outline

1) Finish MOSFET Current Mirrors

2) BJT Current Mirrors

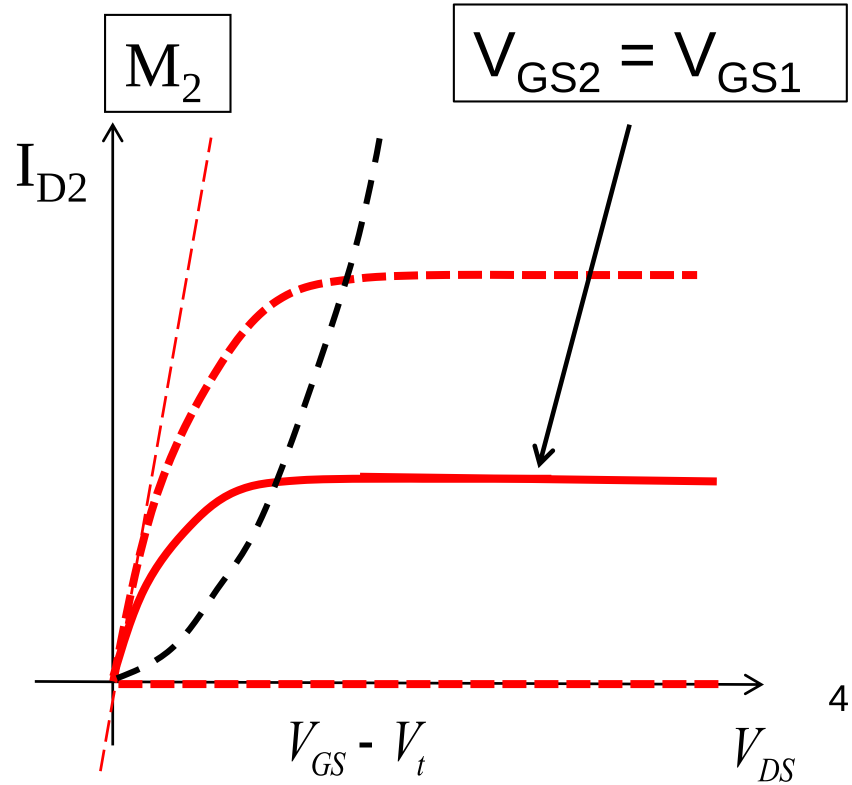
3) CB/GG with Active Load

MOSFET current mirror – ideal I_{REF}



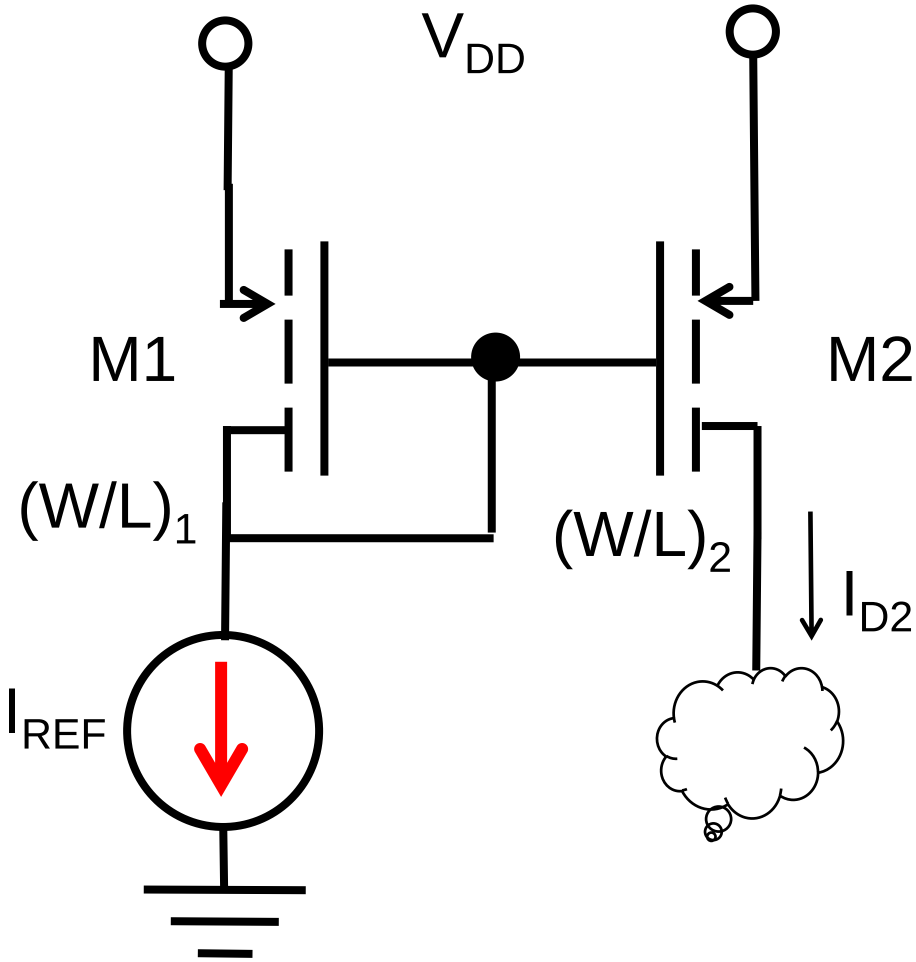
$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

$I_{D2} = I_{D1}[(W/L)_2/ (W/L)_1]$



(As long as $V_{DS2} > V_{DSsat}$,
Ignoring effect of λ)

MOSFET current mirror – PMOS

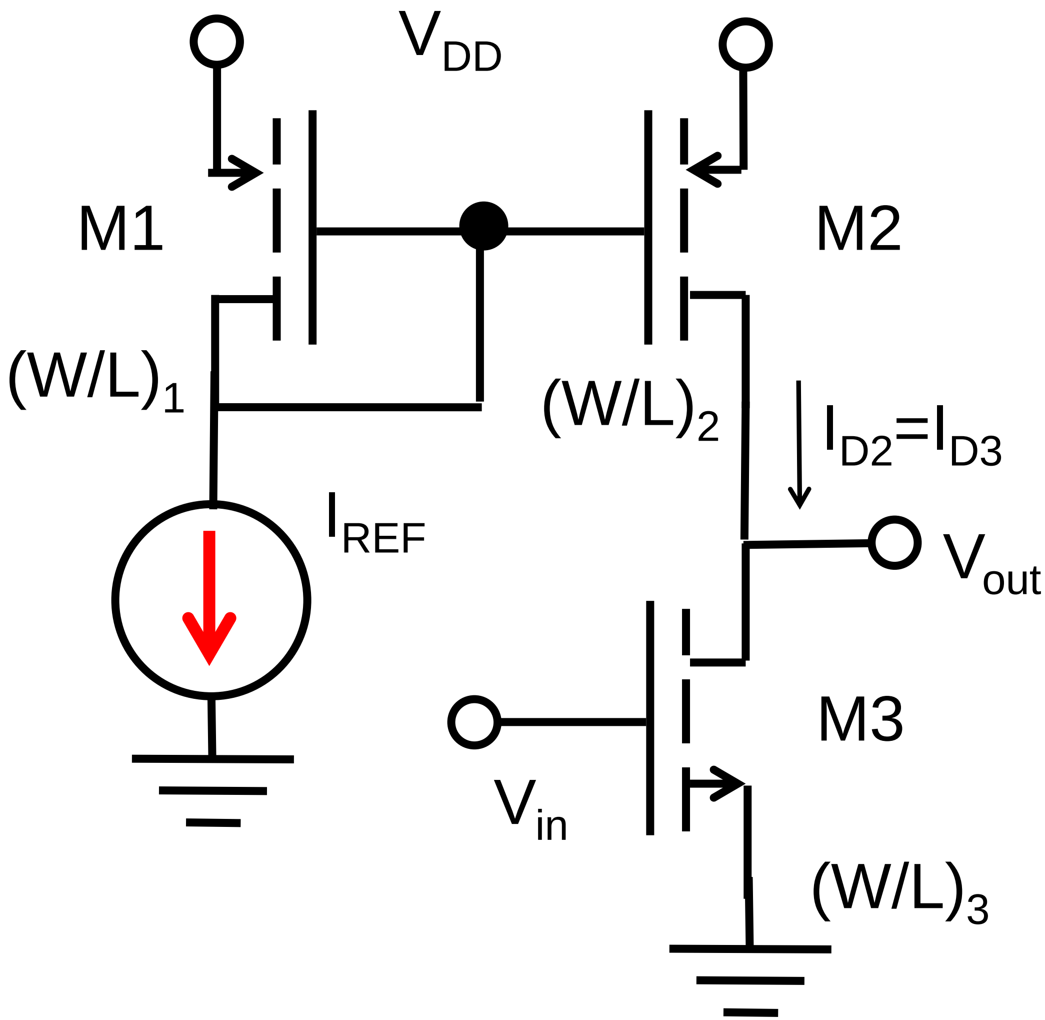


$I_{D2} = I_{D1}[(W/L)_2/ (W/L)_1]$

$V_{SG2} = V_{SG1}$

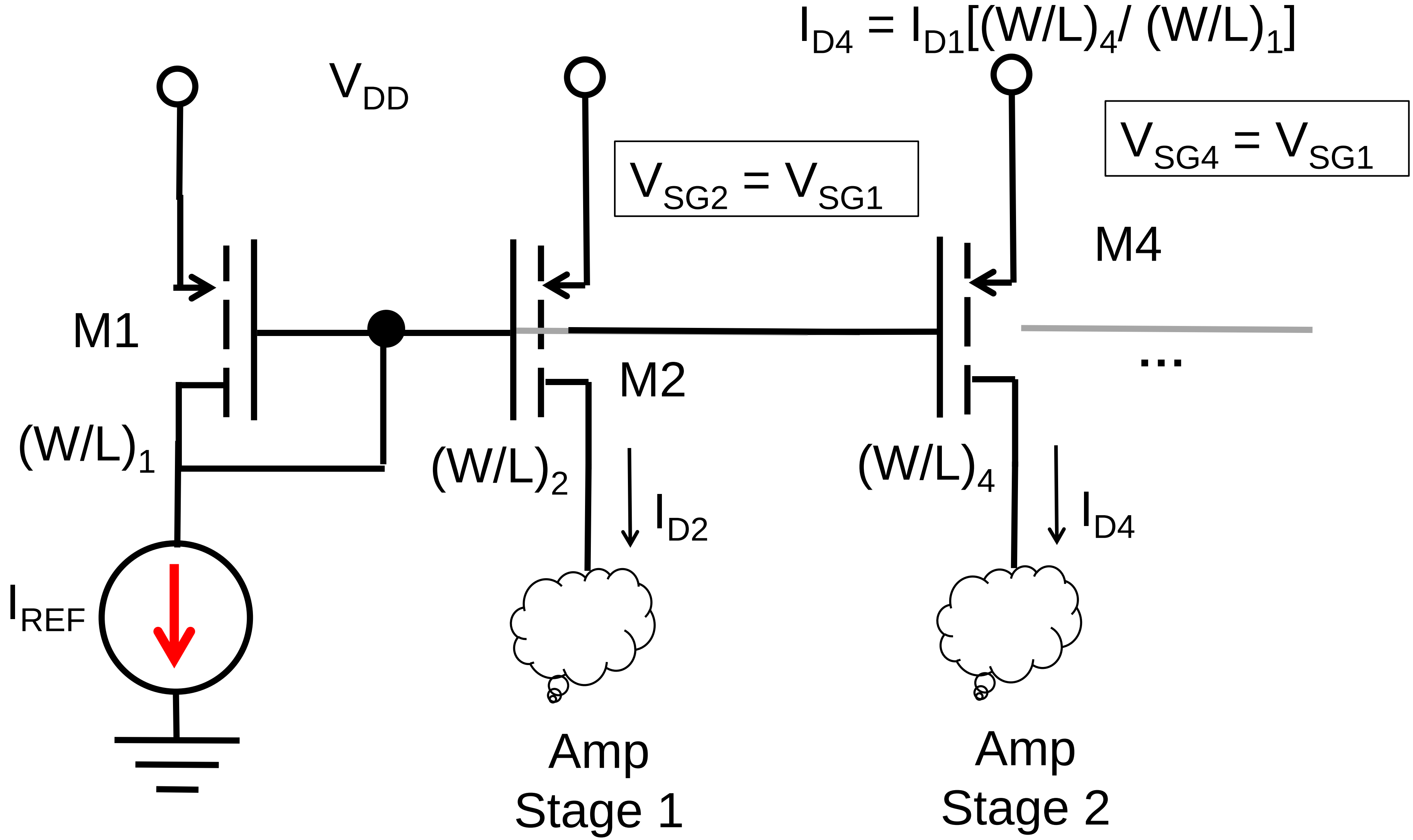
(As long as $V_{SD2} > V_{SDsat}$, Ignoring effect of λ)

MOSFET current mirror – as Active Load (in CS)

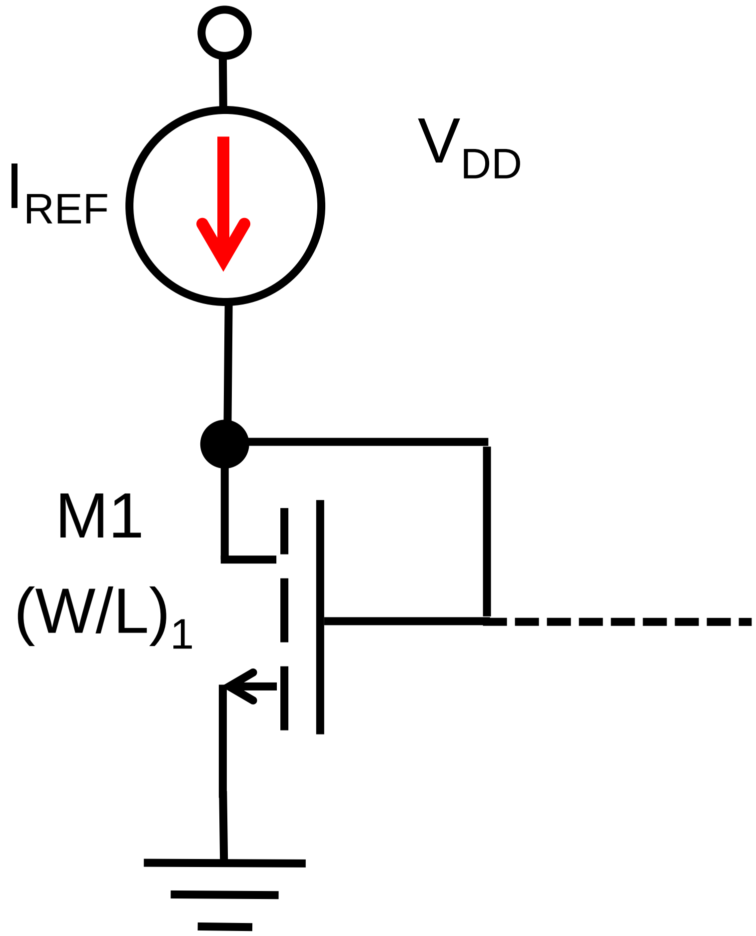


CS used for illustration, but also works for other amplifier topologies.

MOSFET current mirror – Extending to multiple stages

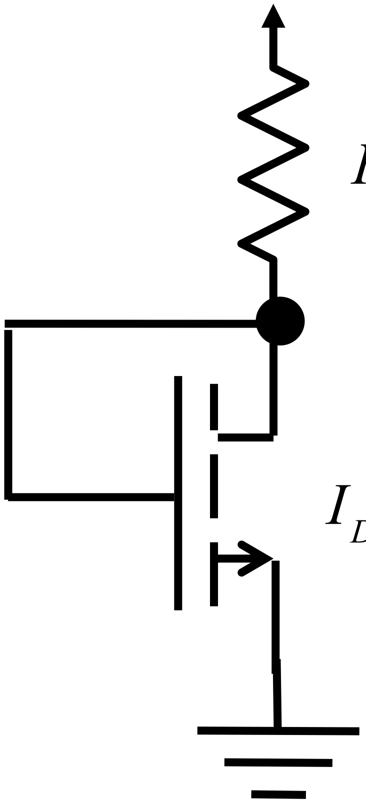


Practical Components in place of I_{REF}



MOSFET: Design

$V_{DD} = +5\ \text{V}$



$R_1 = ?\ \text{k}\Omega$

$I_D = 0.1\left(V_{GS} - 1\right)^2$

Design for: $I_D = 0.5\ \text{mA}$

$$I_D = 0.1\left(V_{GS} - 1\right)^2$$

$$0.5 = 0.1\left(V_{GS} - 1\right)^2$$

$$V_{GS} = 3.24\ \text{V}$$

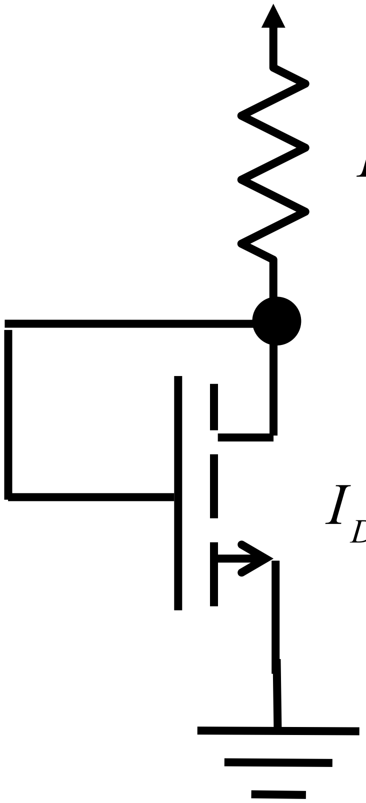
$$V_{GS} = V_D = 3.24\ \text{V}$$

$$R_1 = \frac{5 - 3.24}{0.5} = 3.53\ \text{k}\Omega$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

MOSFET: Analysis

$V_{DD} = +5\text{ V}$



$R_1 = 3.53\text{k}\Omega$

$I_D = 0.1\left(V_{GS} - 1\right)^2$

$I_D = ?\text{ mA}$

$I_D = 0.1\left(V_{GS} - 1\right)^2$

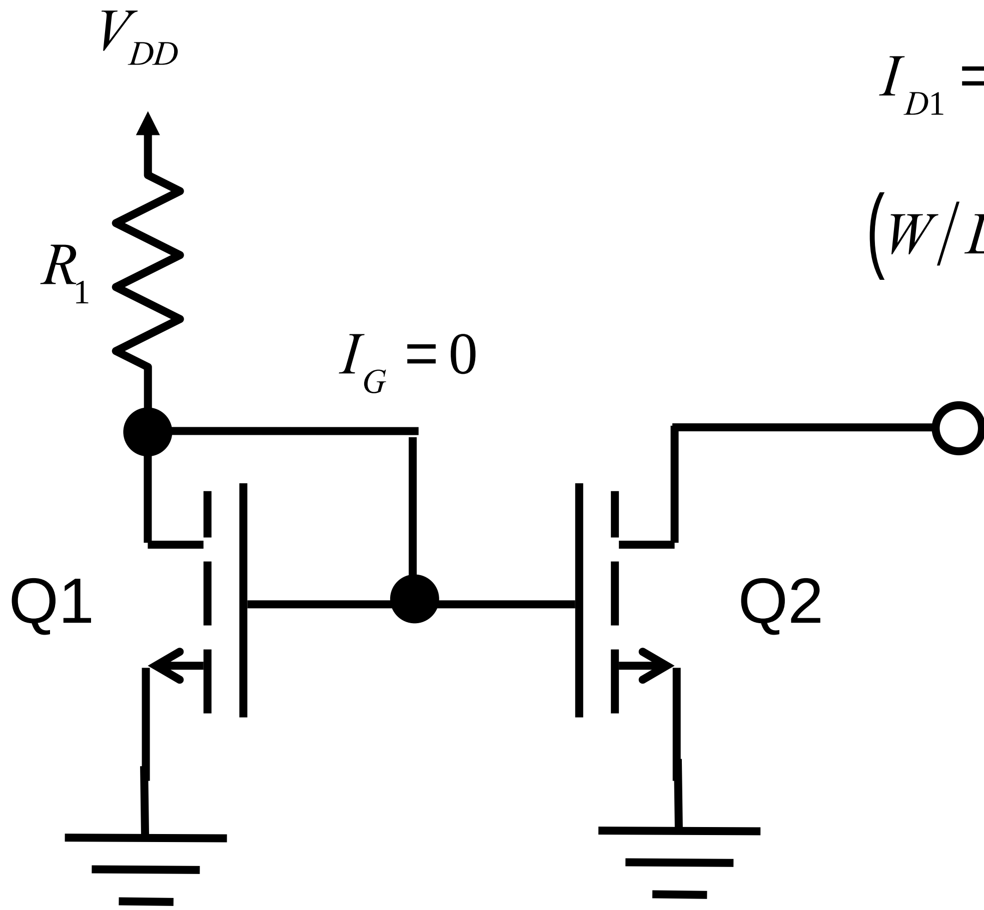
$V_{GS} = V_{DD} - I_D R_1$

2 equations in 2 unknowns

Solve quadratic eqn.

$$I_D = \frac{k_n'}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

MOSFET current mirror



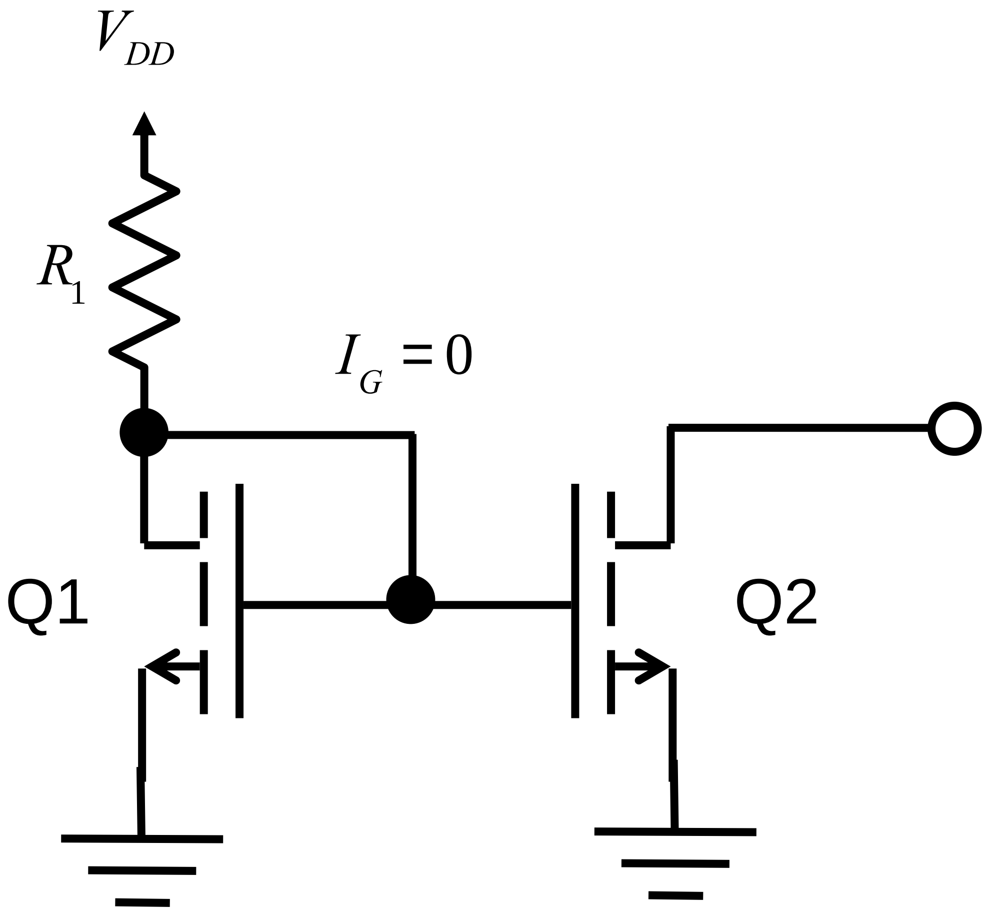
$$I_{D1} = I_{D2} = I_{R_1} = I_{REF}$$

$$(W/L)_1 = (W/L)_2 \quad V_{D1} = V_{D2}$$

$$\neg \quad R_o = r_{o2} = \frac{V_{A2}}{I_{D2}}$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

MOSFET current mirror



$$I_{D1} = I_{REF}$$

$$m = \frac{(W/L)_2}{(W/L)_1}$$

$I_{D2}/I_{REF} \approx m$

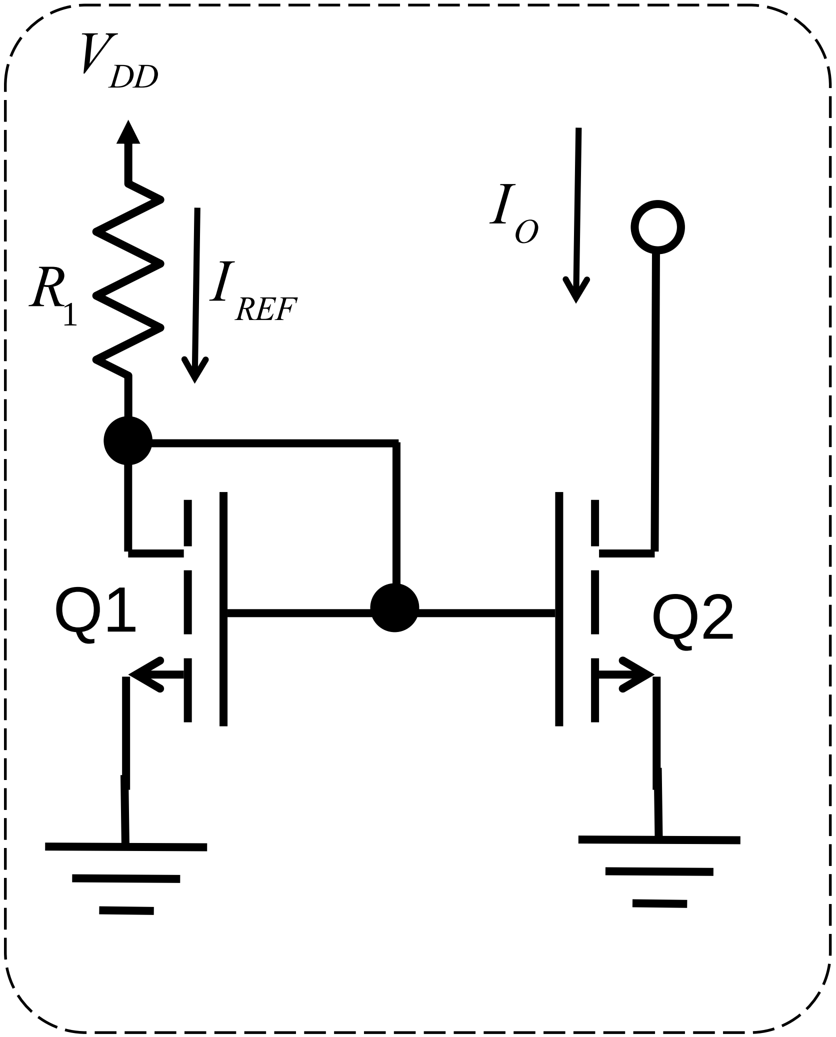
$$I_{D2}/I_{REF} = m\,(1 + (V_{DS2} - V_{GS})/V_{A2})$$

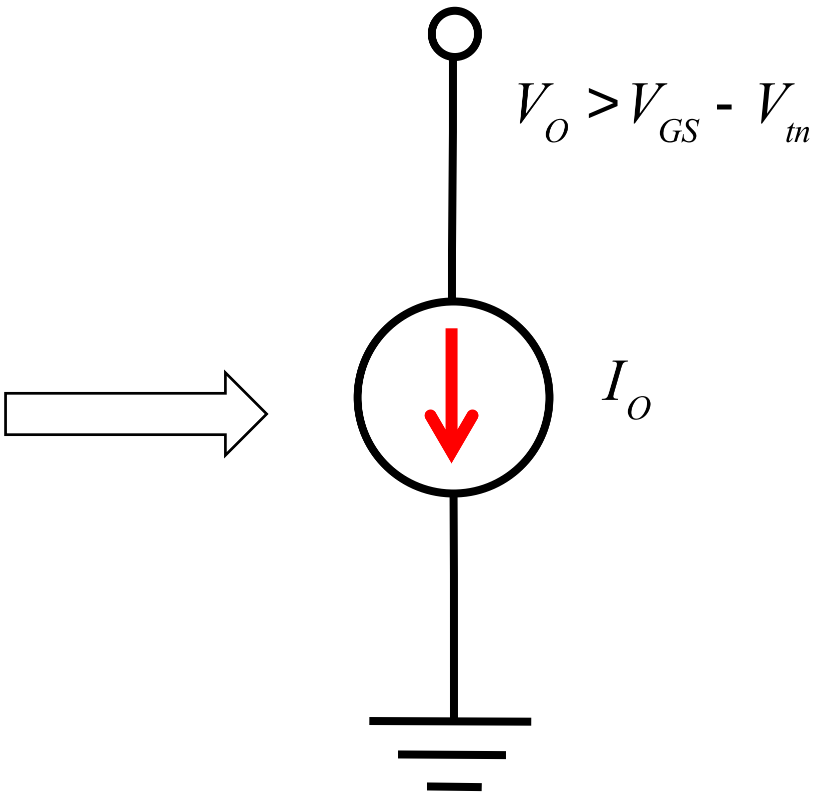
PMOS:

$$\frac{I_{D2}}{I_{REF}} = m\left(1 + \frac{V_{SD2} - V_{GS}}{V_{A2}}\right)$$

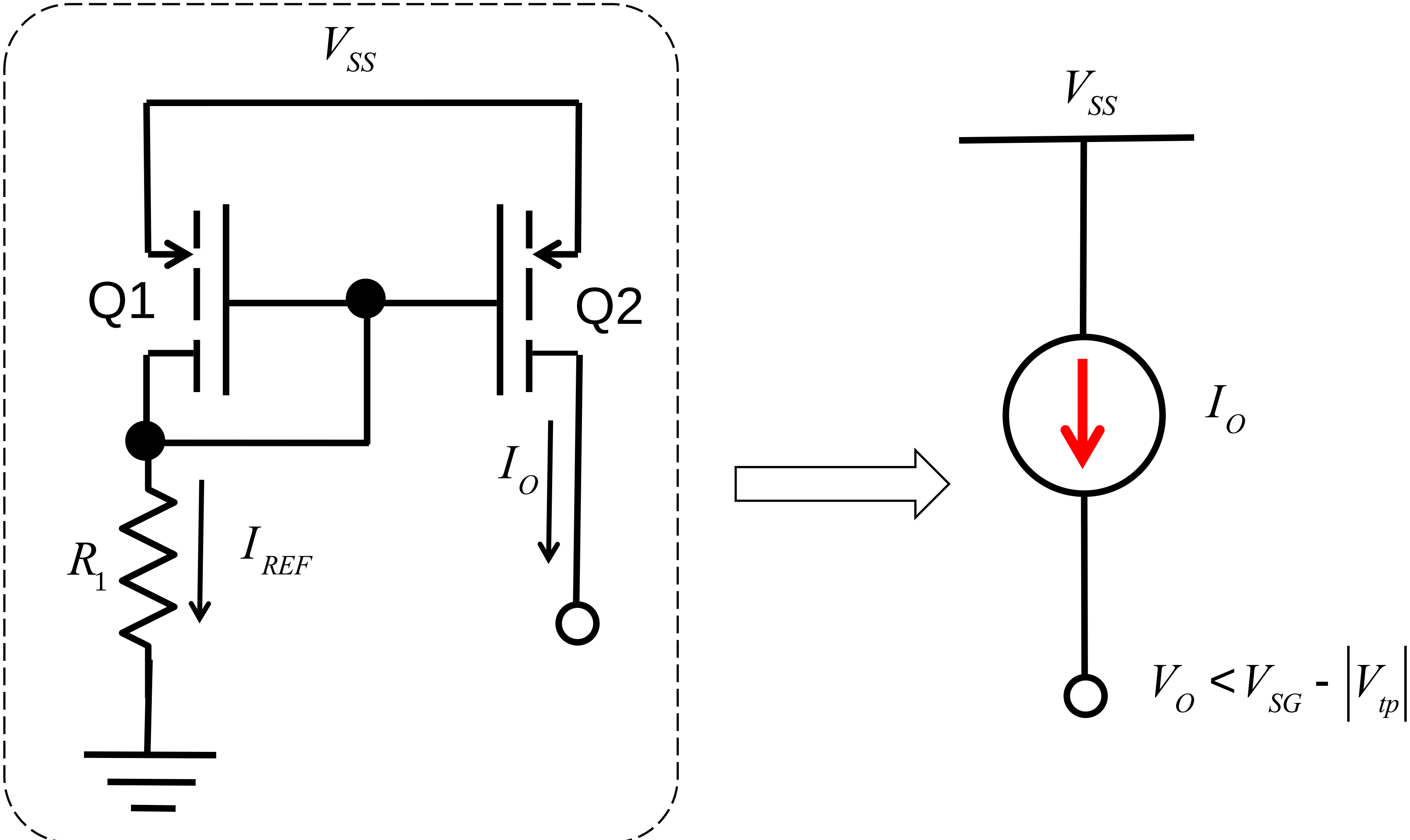
$$I_D = \frac{k'_n}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

MOSFET current source

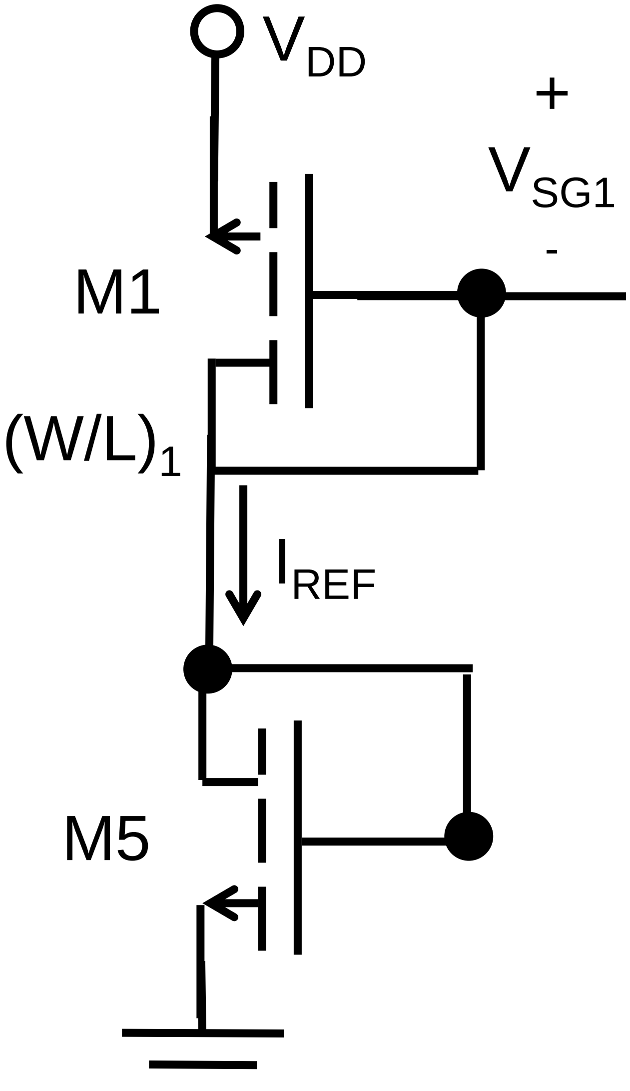


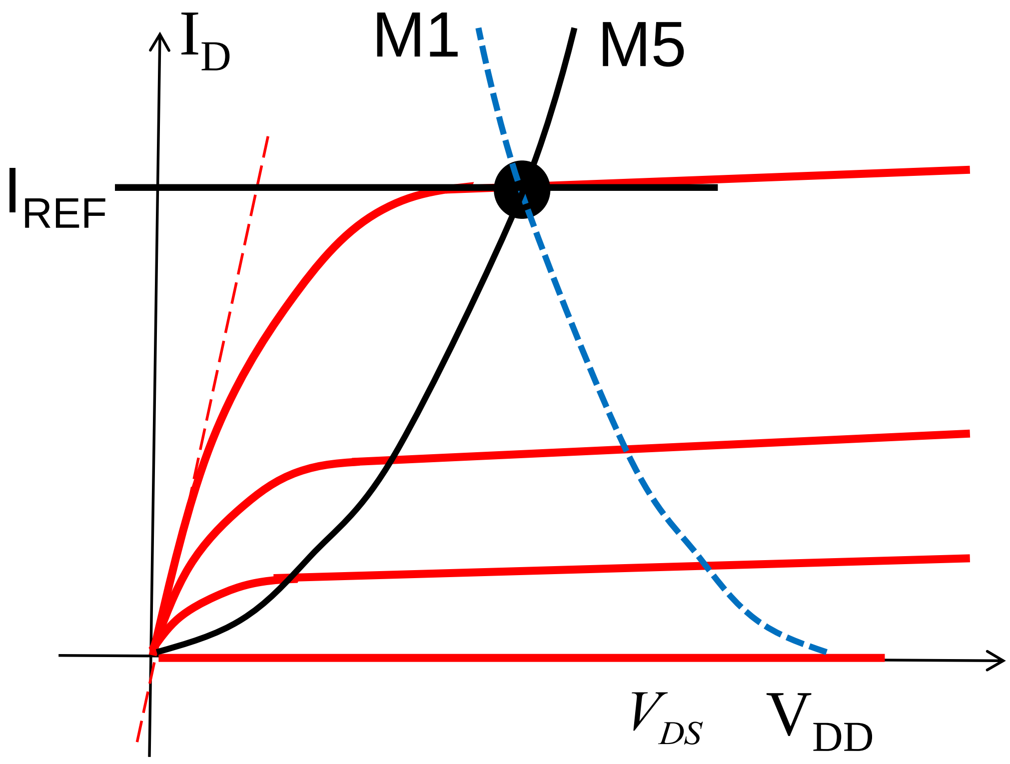


P- MOSFET current source



Can also set I_{REF} with Transistors





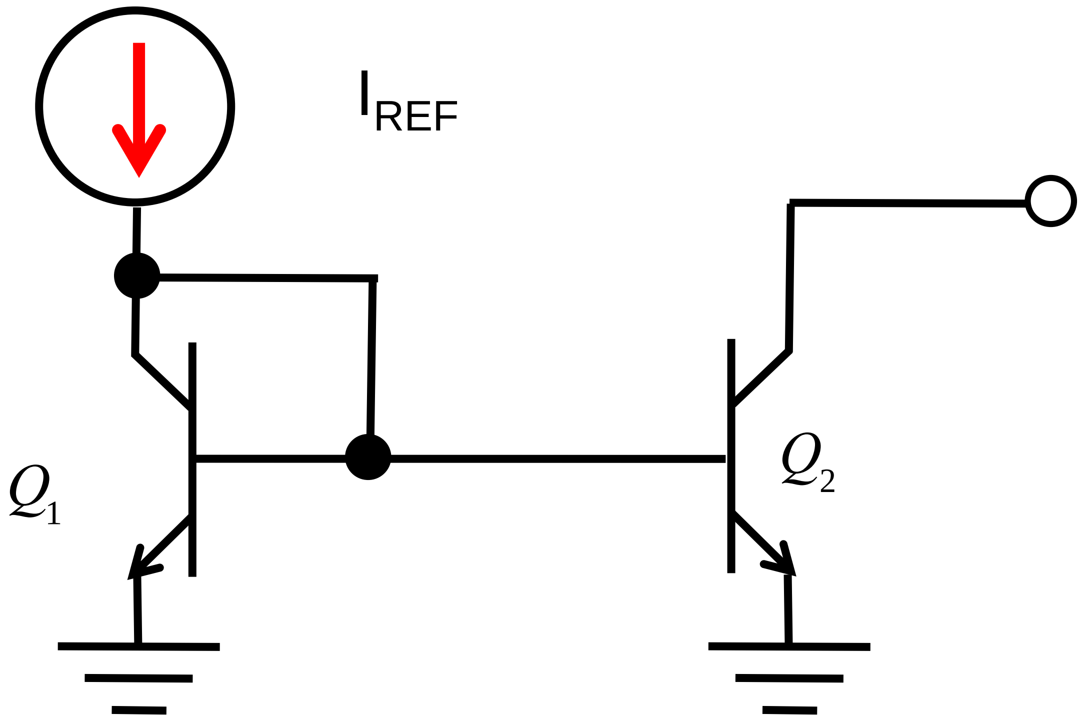
Outline

1) Finish MOSFET Current Mirrors

2) BJT Current Mirrors

3) CB/GG with Active Load

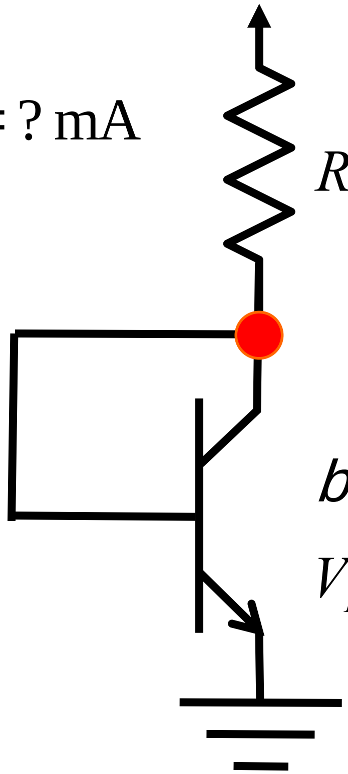
BJT Current Mirror



Analysis

$V_{CC} = +5\ \mathrm{V}$

$I_C = ?\ \mathrm{mA}$



$R_1 = 4.5\ \mathrm{k\Omega}$

$\beta = 75$

$V_{BE} = 0.7\ \mathrm{V}$

$$I_R = \frac{5 - 0.7}{4.3\ \mathrm{k\Omega}} = 1.0\ \mathrm{mA}$$

KCL:

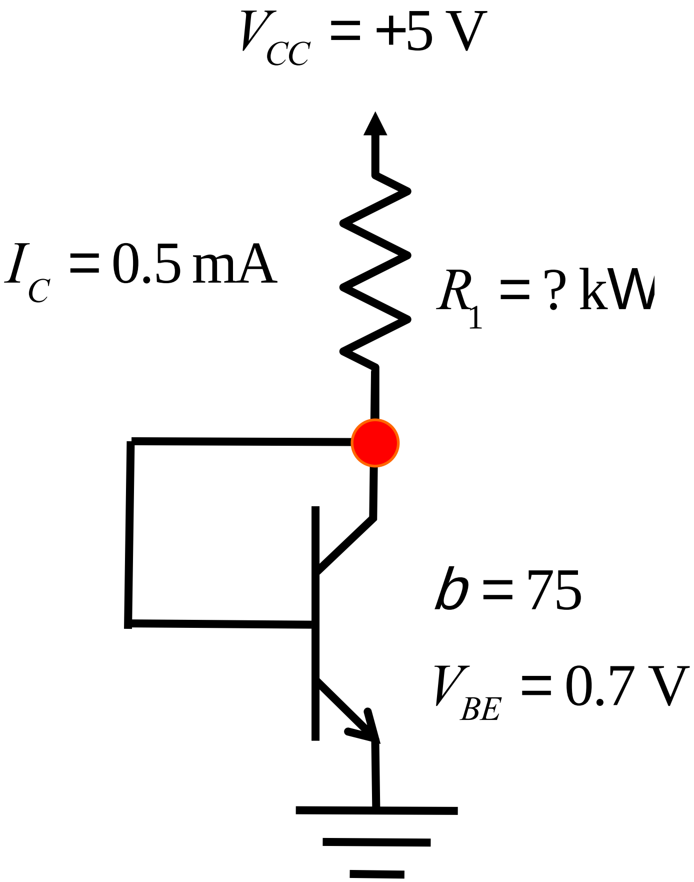
$$I_C + I_B = I_R = 1\ \mathrm{mA}$$

$$I_C + I_C/\beta = I_R$$

$$I_C = \frac{I_R}{1 + 1/\beta}$$

$$I_C = \frac{1}{1 + 1/75} = 0.987\ \mathrm{mA}$$

Design



$$I_C = \frac{I_R}{1 + 1/\beta} = 0.5\text{ mA}$$

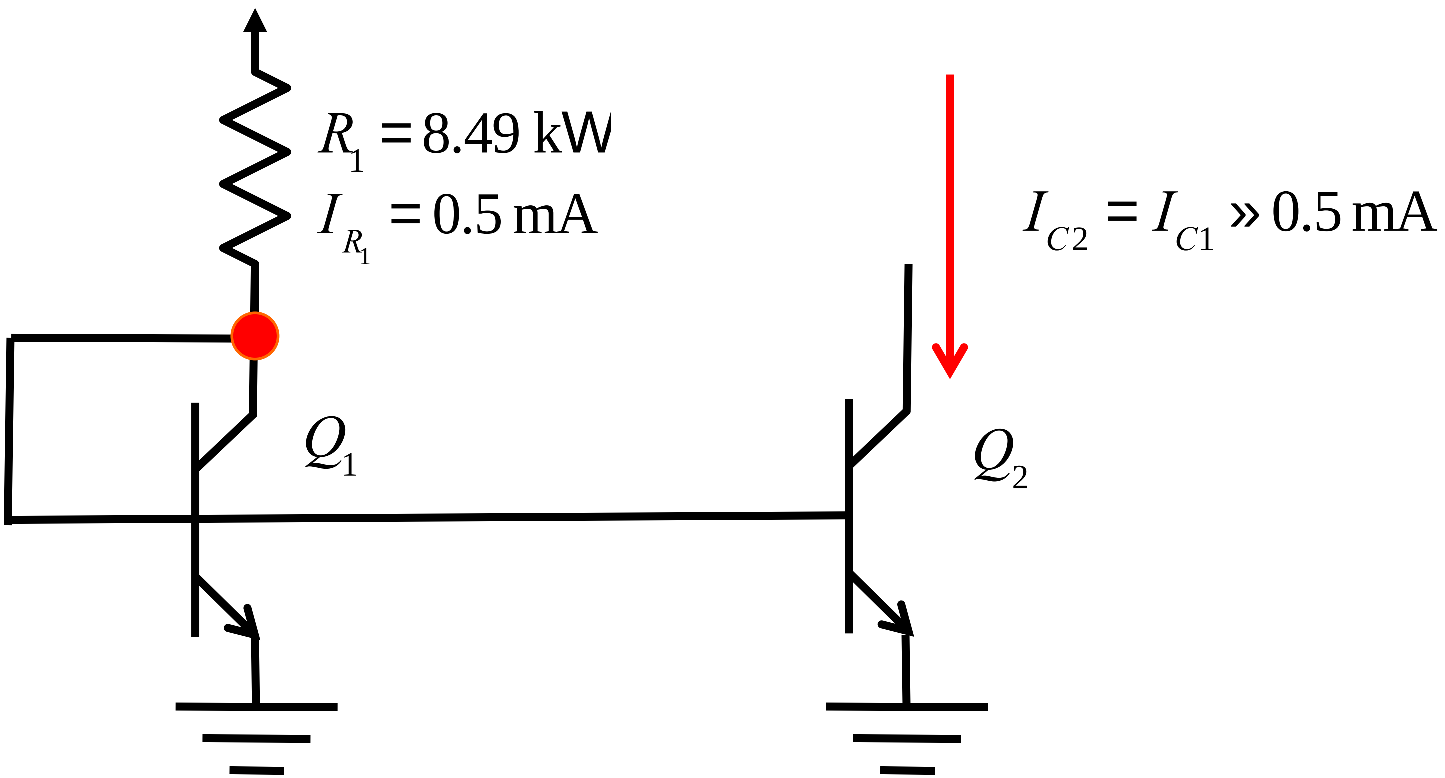
$$I_R = I_C\left(1 + 1/\beta\right) = 0.507\text{ mA}$$

$$R_1 = \frac{V_{R_1}}{I_{R1}} = \frac{5 - 0.7}{0.507\text{ mA}} = 8.487\text{ k}\Omega$$

BJT “Current Mirror”

$V_{CC} = +5\ \text{V}$

$$I_C = I_S e^{qV_{BE}/k_BT}\left(1 + V_{CE}/V_A\right)$$



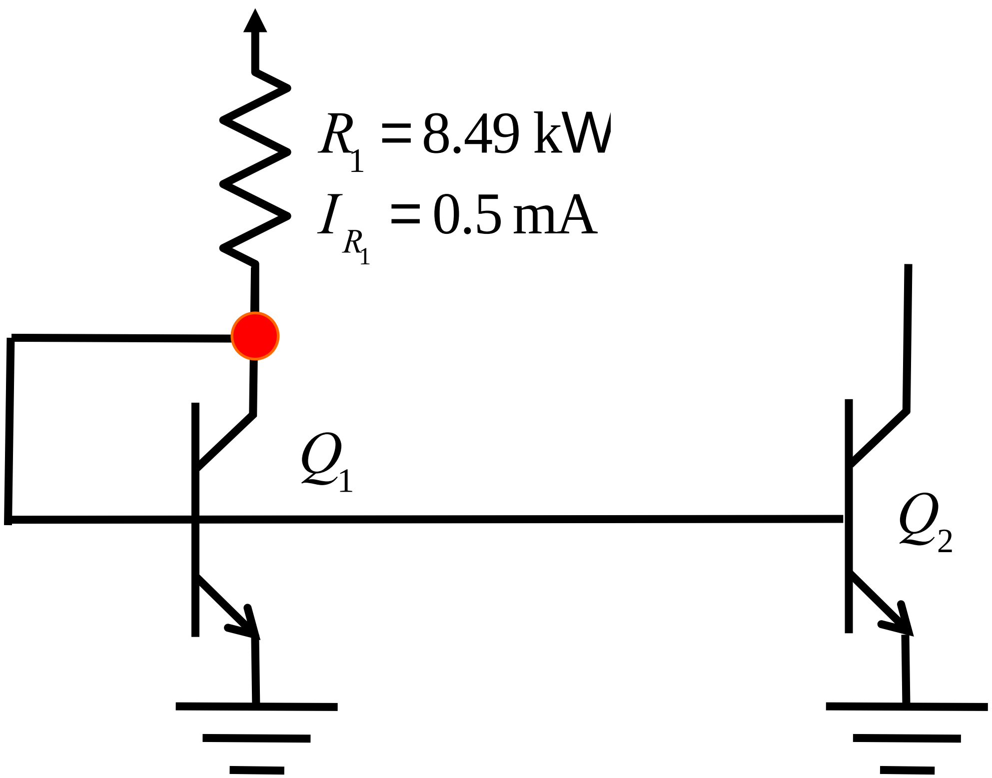
$b = 75$

$V_{BE} = 0.7\ \text{V}$

Initially, assume Q_2 identical to Q_1
(same emitter area, same I_s)

BJT Current Mirror

$V_{CC} = +5\text{ V}$



$b = 75$

$I_{C2} = I_{C1} = ?\text{ mA}$

$V_{BE} = 0.7\text{ V}$

KCL:

$$I_C + 2I_B = I_{R_1} = 0.5\text{ mA}$$

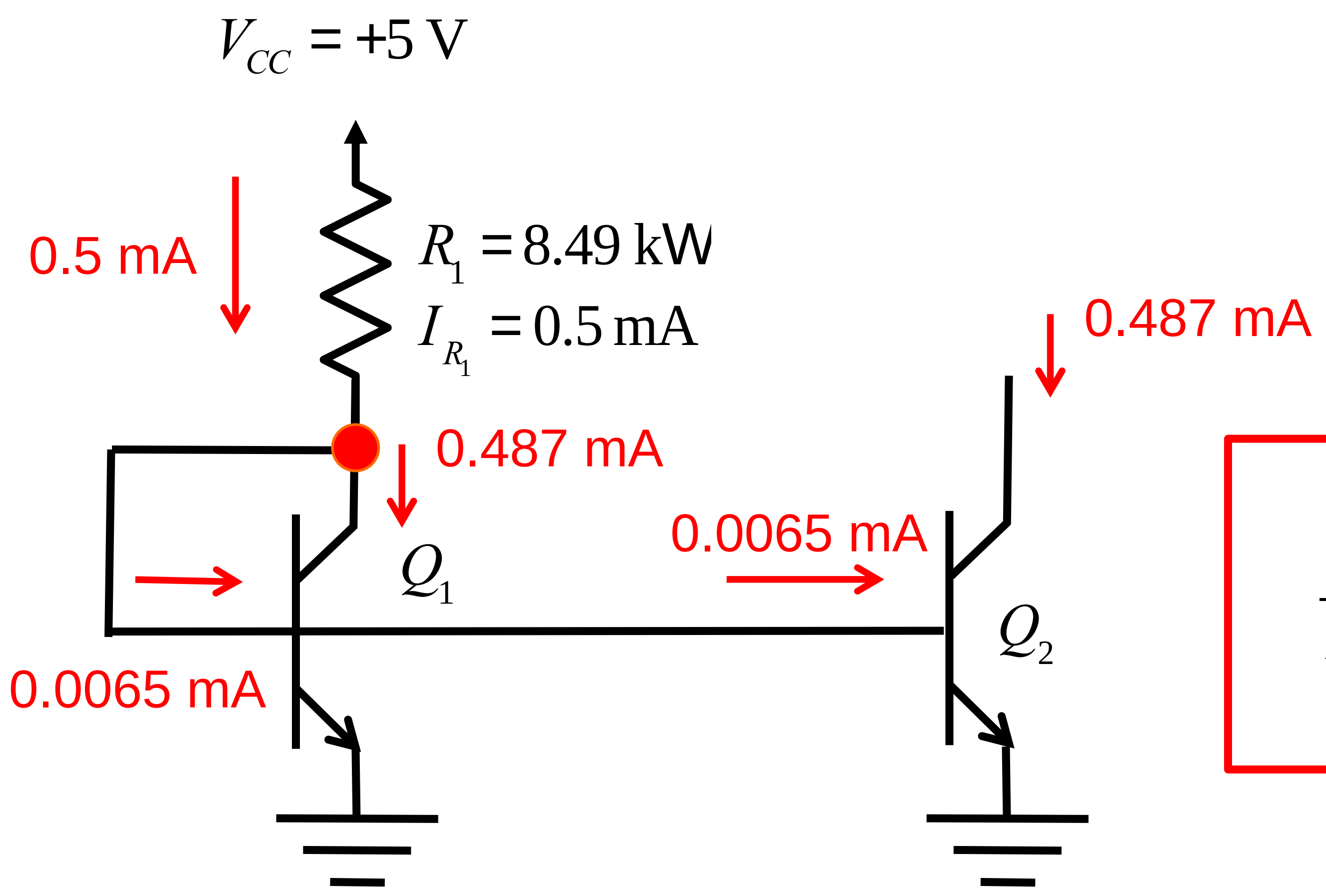
$$I_C + 2I_C/b = I_R$$

$$I_C = \frac{I_{R_1}}{1+2/b}$$

$$I_C = \frac{0.5}{1+2/75} = 0.487\text{ mA}$$

$$I_{C_1} = I_{C2} = 0.487\text{ mA}$$

BJT Current Mirror (discussion)

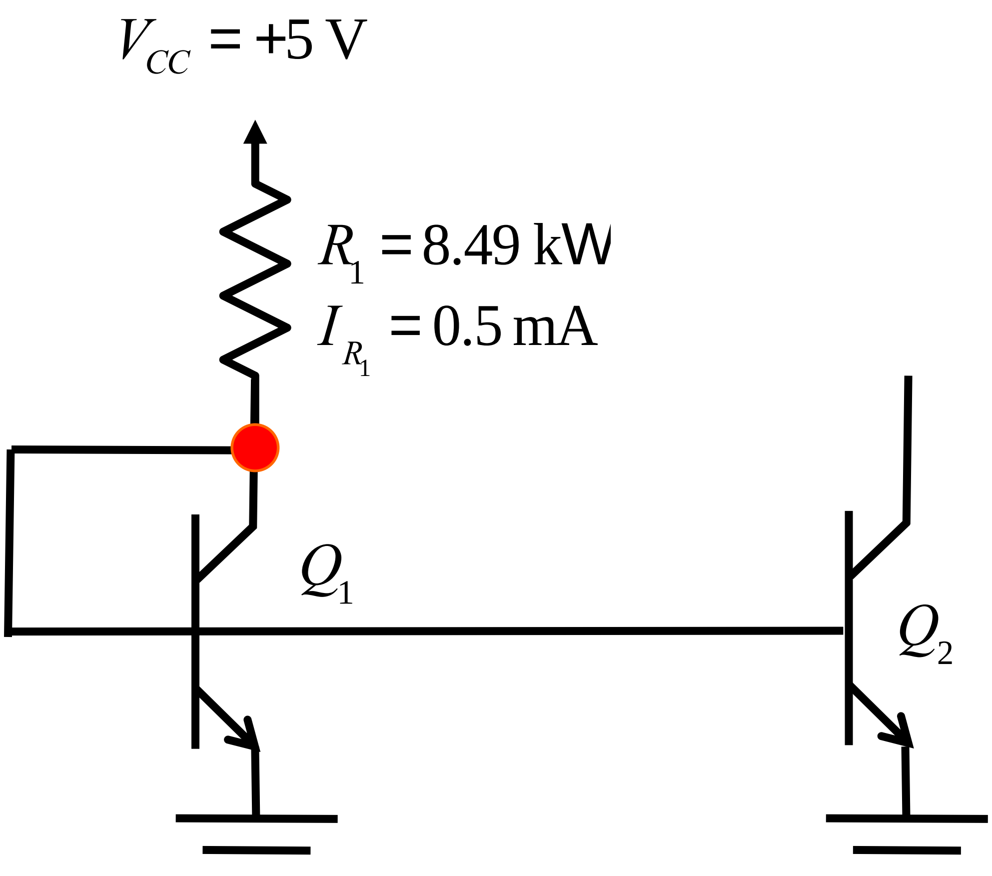


$$\frac{I_C}{I_{R_1}} = \frac{1}{1 + 2/b}$$

$b = 75$

$V_{BE} = 0.7$ V

BJT Current Mirror (discussion)



$$I_C = I_S e^{qV_{BE}/k_BT}\left(1 + V_{CE}/V_A\right)$$

We have **ignored** the Early effect

And we have assumed that the transistors have equal areas.

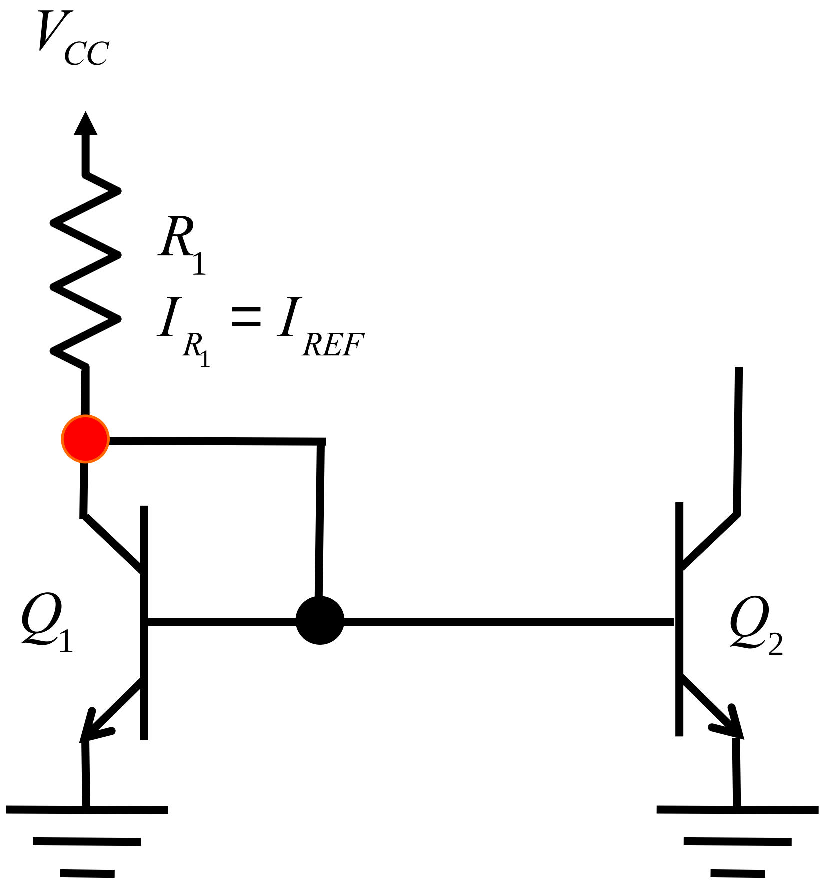
$$I_S = A_{EB} I¢_S$$

$b = 75$

$V_{BE} = 0.7\ \text{V}$

$$I_{C2} = I_{C1} = ?\ \text{mA}$$

BJT Current Mirror (different areas)



$$I_C = I_S e^{qV_{BE}/k_B T}\left(1 + V_{CE}/V_A\right)$$

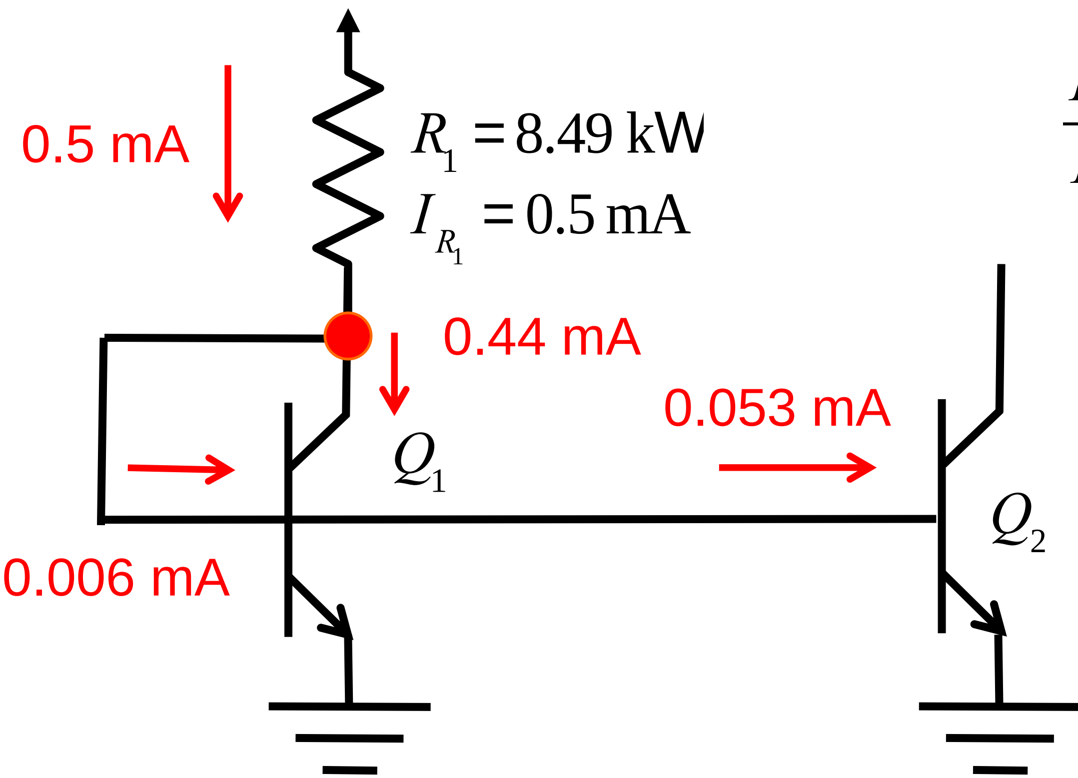
$$m = \frac{A_{EB2}}{A_{EB1}}$$

$$\frac{I_{C2}}{I_{R_1}} = \frac{m}{1 + (m+1)/b}\left(1 + \frac{V_{CE} - V_{BE}}{V_{A2}}\right)$$

Now considering Q_2 with different emitter area than Q_1 (different I_s).
At same V_{BE}, $I_{B2} = m\, I_{B1}$.

BJT Current Mirror – Numerical Example

$V_{CC} = +5\text{ V}$



$b = 75$

$V_{BE} = 0.7\text{ V}$

m = 9

$V_{A2} = \infty$

$$m = \frac{A_{EB2}}{A_{EB1}}$$

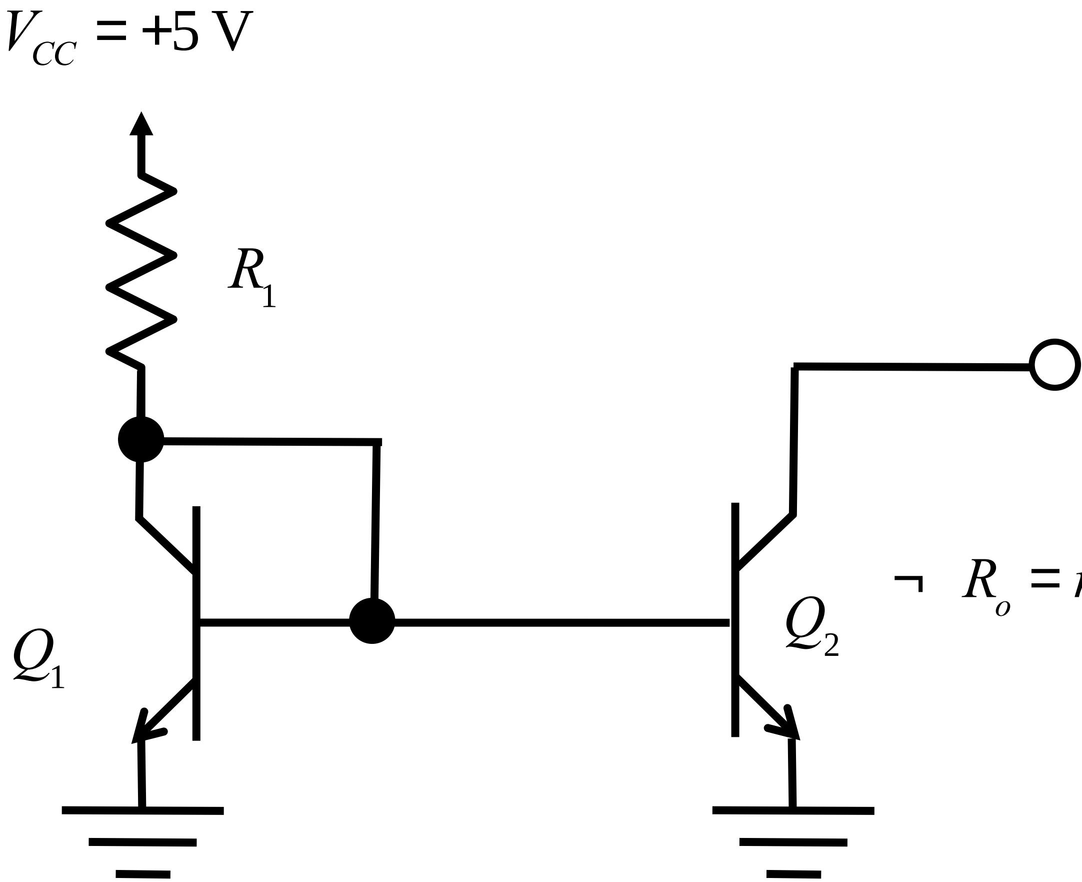
$$\frac{I_{C2}}{I_{R_1}} = \frac{m}{1 + (m+1)/b}\left(1 + \frac{V_{CE} - V_{BE}}{V_{A2}}\right)$$

$$I_{C2} = 0.5\text{mA}\ \frac{9}{1 + (10/75)}$$

= 4.0 mA

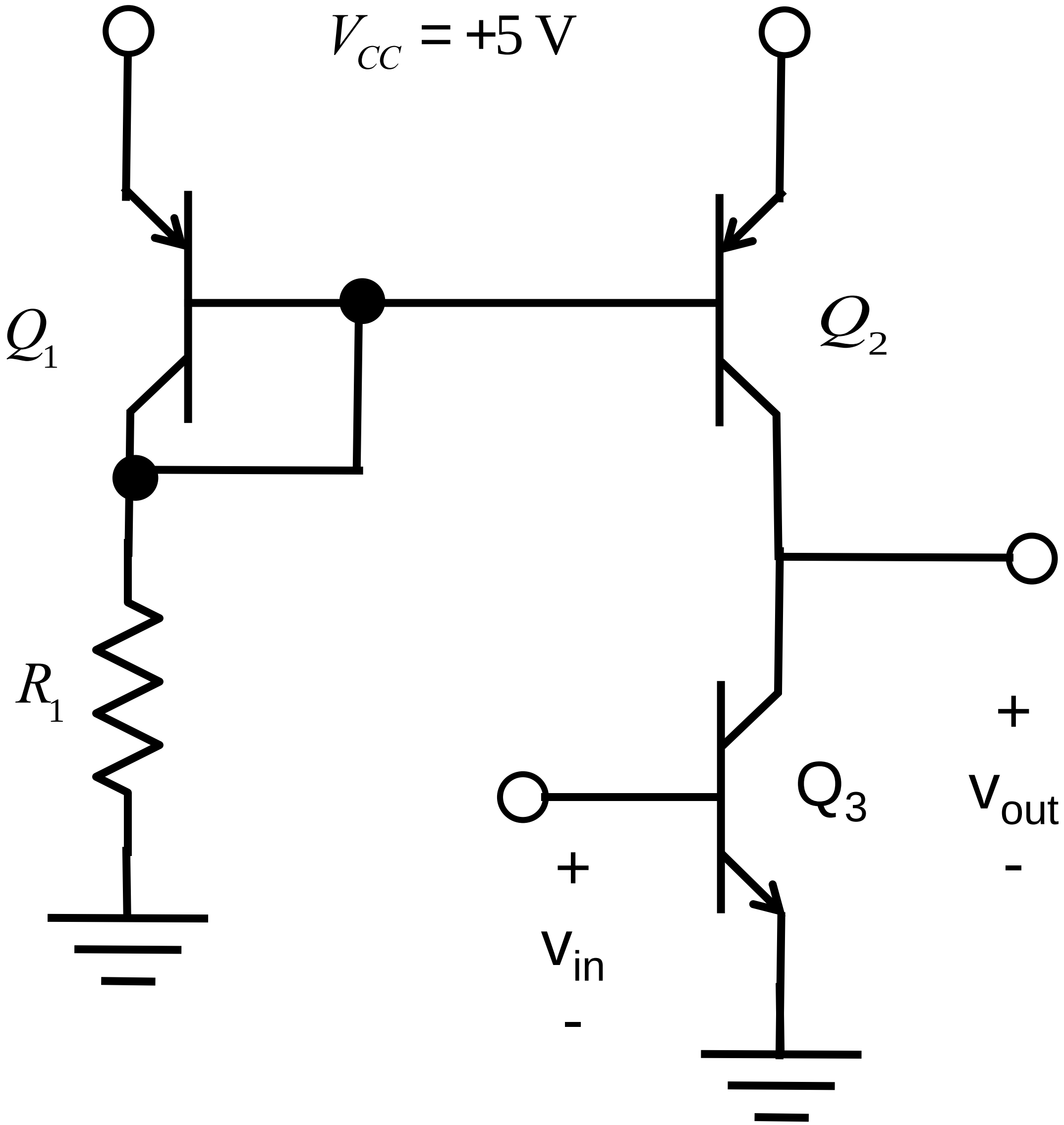
8x I_{R1}, versus 9x area ratio

Current Mirror (output resistance)

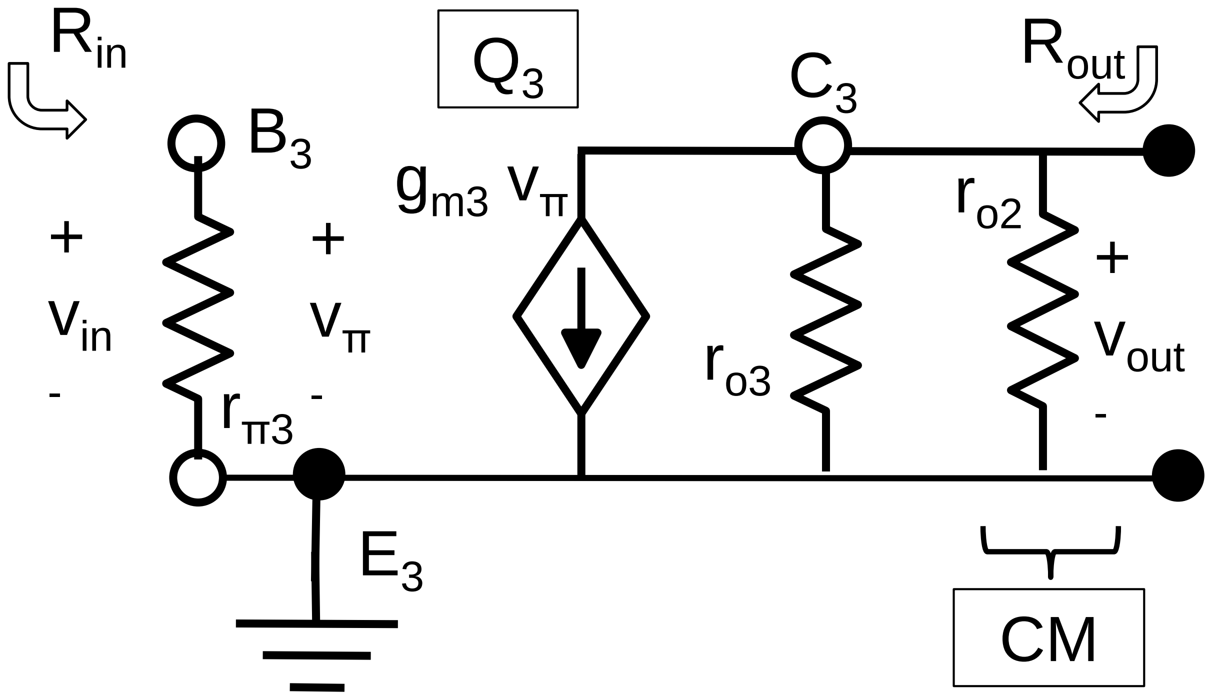


$$\neg \quad R_o = r_{o2} = \frac{V_{A2}}{I_{C2}}$$

Current Mirror as active load



CE with Active Load – Small Signal



$A_{v0} = v_{out}/v_{in} = -g_{m3}(\ r_{o3} \ || \ r_{o2})$

$R_{in} = r_{\pi 3}$ $\qquad$ $R_{out} = r_{o3} \ || \ r_{o2}$

Compared to resistive load:
A_{v0} larger, R_{out} larger

PNP and NPN current mirrors

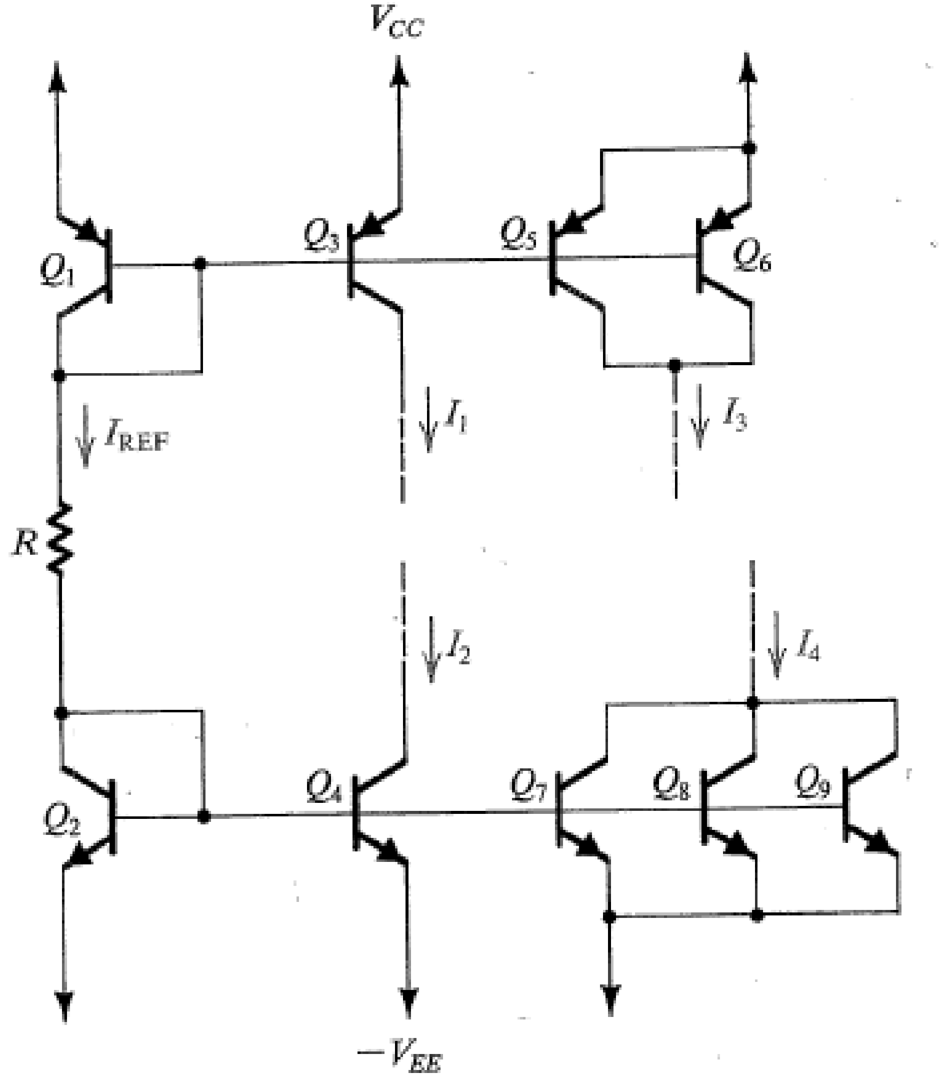


Fig. 7.31 6th Ed. Sedra and Smith

Current Mirror Comments

Many sophisticated current mirror / current source circuits exist (to minimize beta mismatch, maximize output resistance.

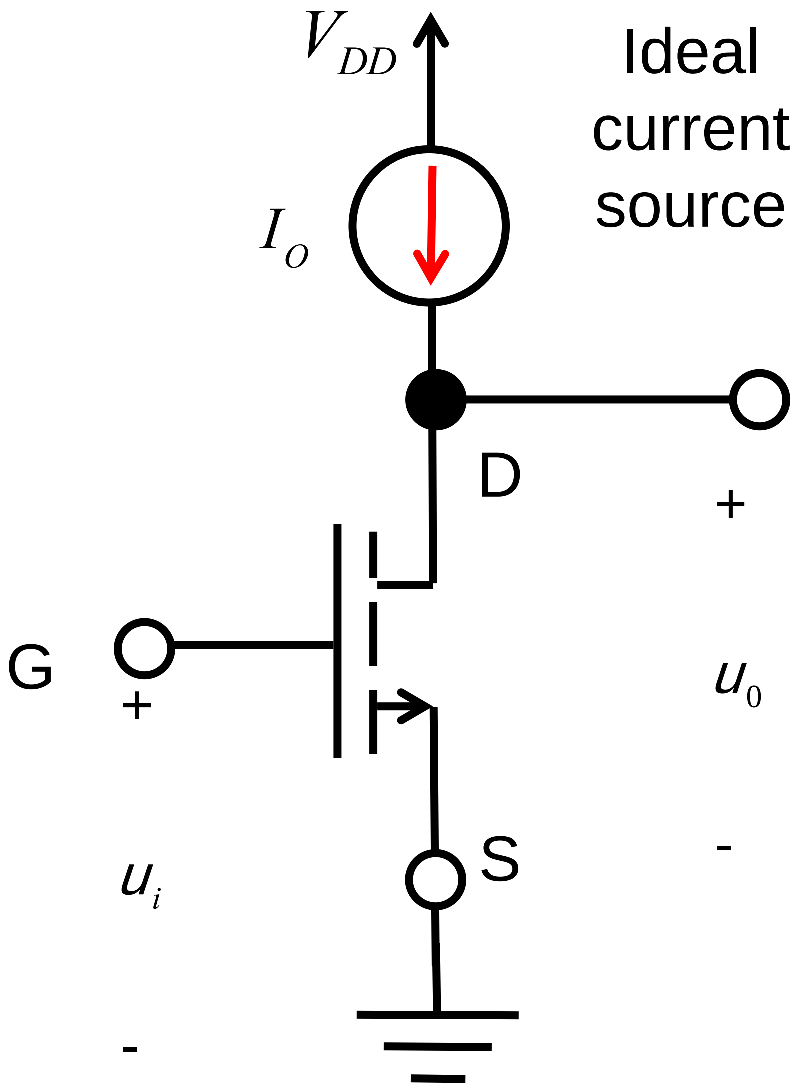
See: Sedra – Smith 6th Ed. Sec. 7.5
Sedra – Smith 7th Ed. Sec. 8.6

Outline

1) Current Mirrors

2) Common Source with “active load”

Basic IC gain cell



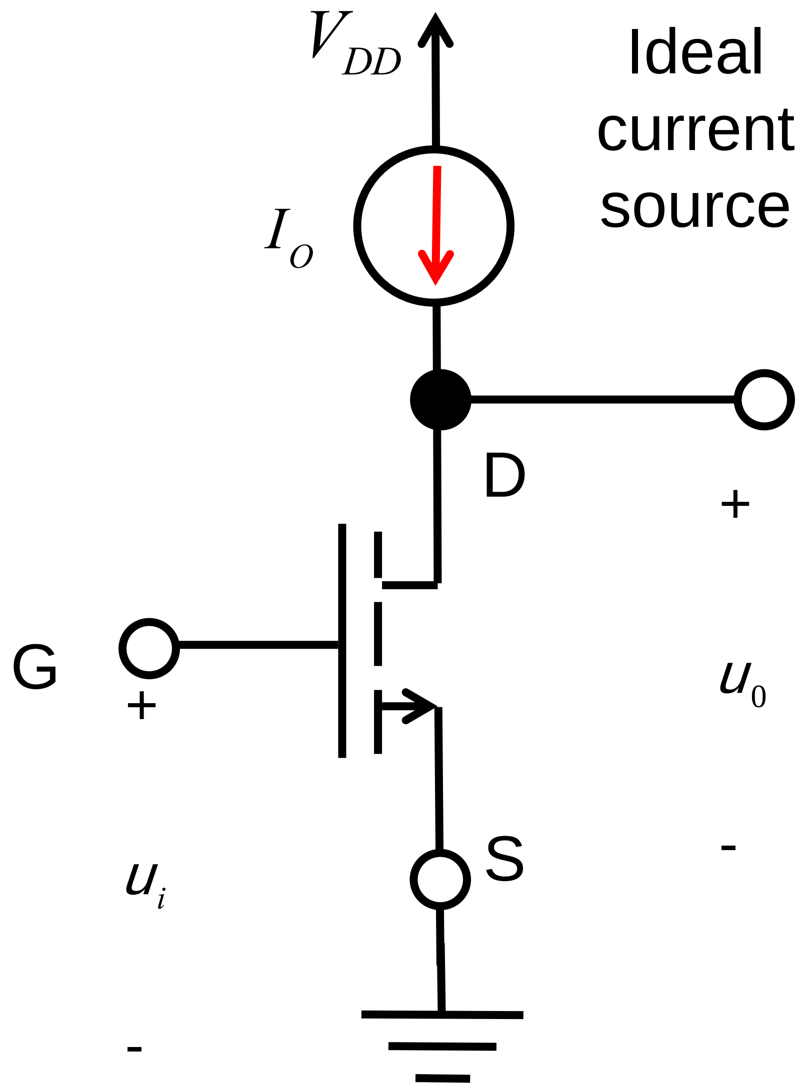
$R_O = \infty$

$$A_{u_o} = \frac{u_o}{u_i} = -g_m r_o$$

$$R_{in} = \infty$$

$$R_o = r_o$$

Maximum gain



Ideal current source

$R_O =$ ¥

$$A_{u_o} = -g_m r_o$$

$$A_0 = \left|A_{u_o}\right| = g_m r_o$$

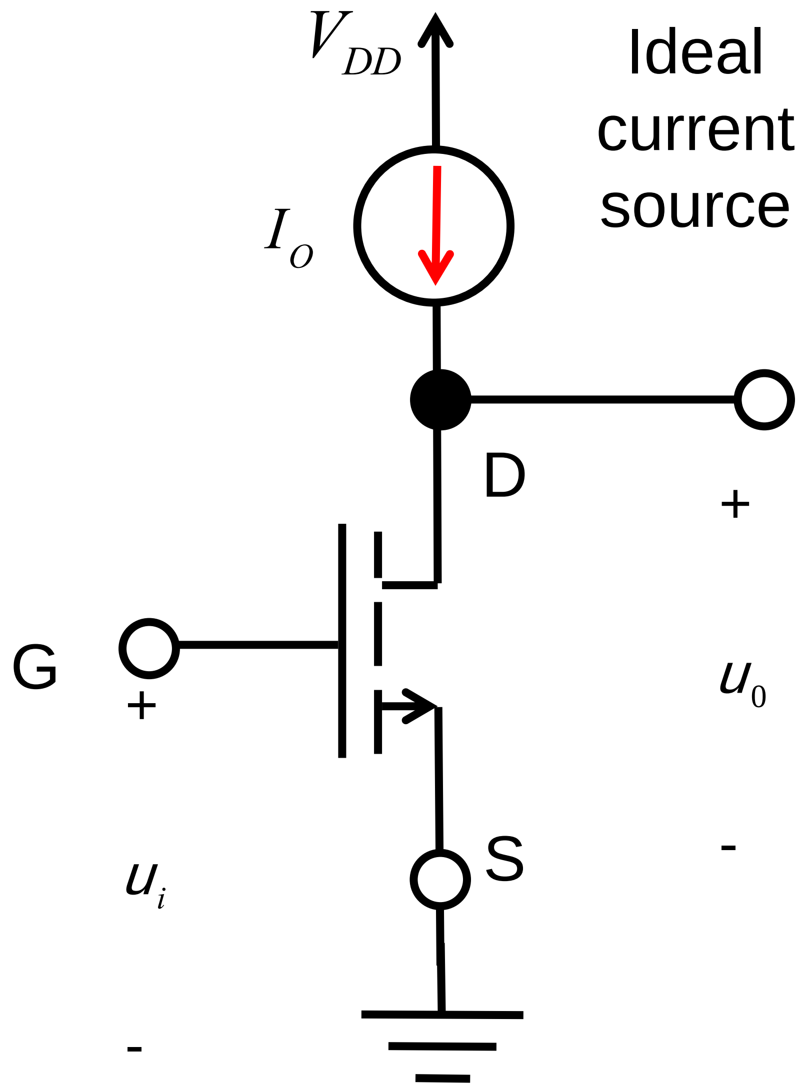
“self-gain”

“intrinsic-gain”

$$g_m = \frac{I_D}{\left(V_{GS} - V_{tn}\right)/2}$$

$$r_o = \frac{V_A}{I_D}$$

Maximum (intrinsic/self) gain



$R_O =$ ¥

$$A_0 = \frac{V_A}{\left(V_{GS} - V_{tn}\right)/2}$$

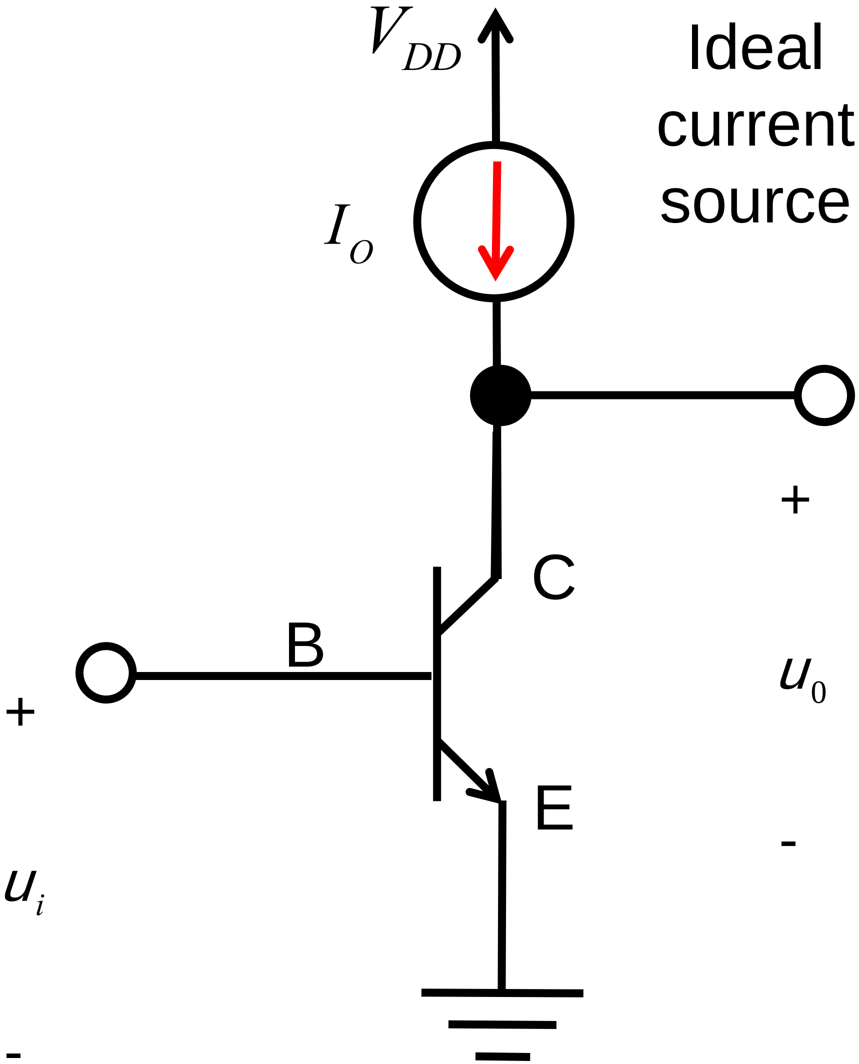
Modern CMOS:

$\left(V_{GS} - V_{tn}\right)$ » 0.2 V

V_A » 3 - 4 V

A_0 » 30 - 40

Basic IC gain cell (BJT)



Ideal current source

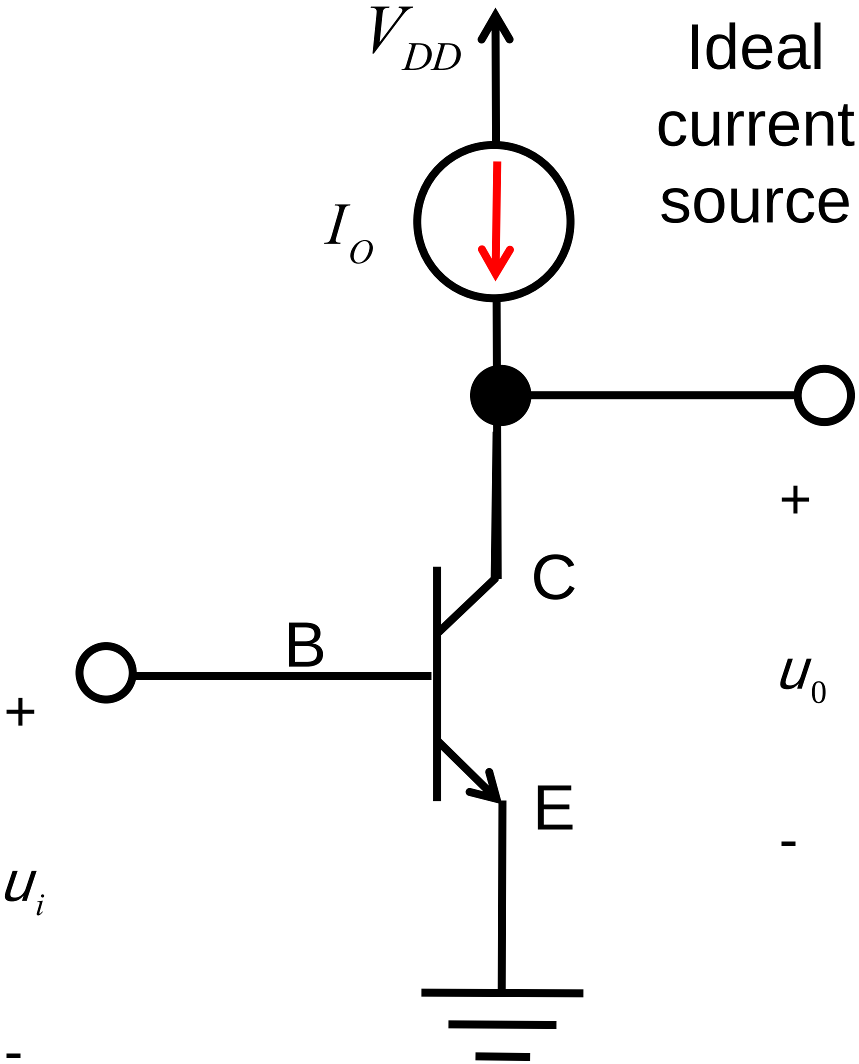
$R_O = ¥$

$$A_{u_o} = \frac{u_o}{u_i} = - g_m r_o$$

$$R_{in} = r_p$$

$$R_o = r_o$$

Intrinsic gain (BJT)



$R_O = ¥$

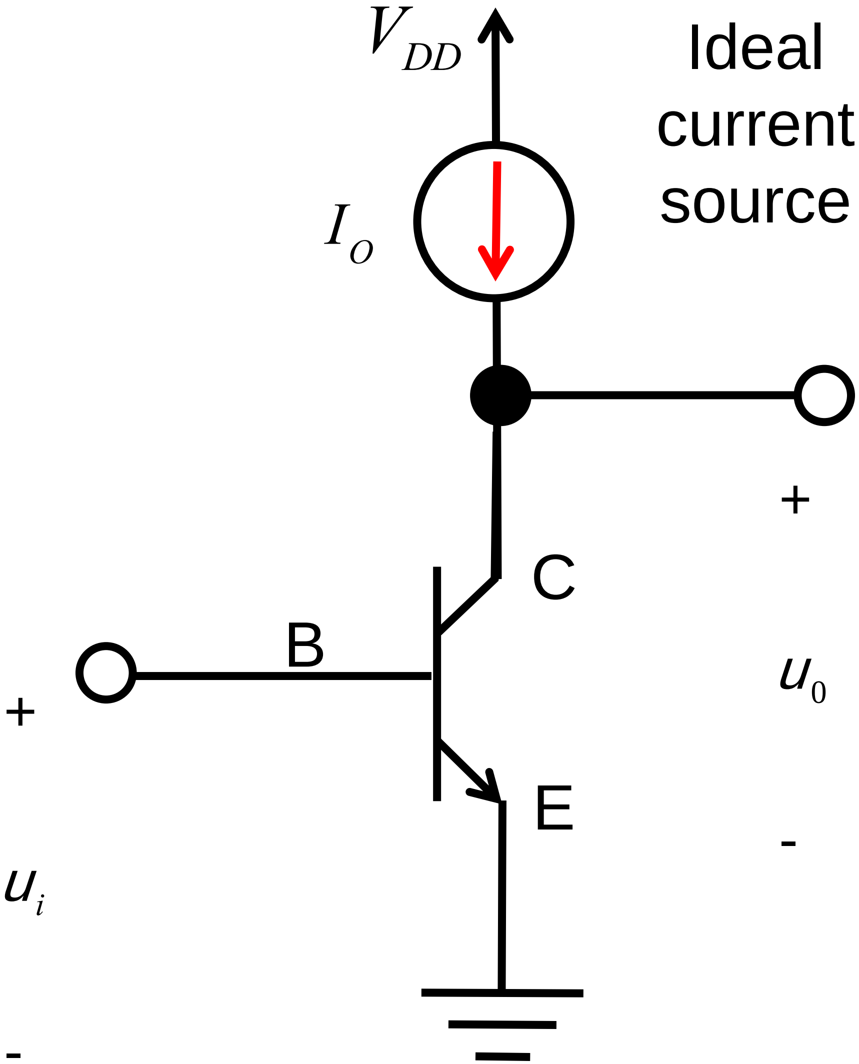
$$A_0 = g_m r_o$$

$$g_m = \frac{I_C}{V_T}$$

$$r_o = \frac{V_A}{I_C}$$

$$A_0 = \frac{V_A}{V_T}$$

Intrinsic gain (BJT)



$$R_O = \infty$$

$$A_0 = \frac{V_A}{V_T}$$

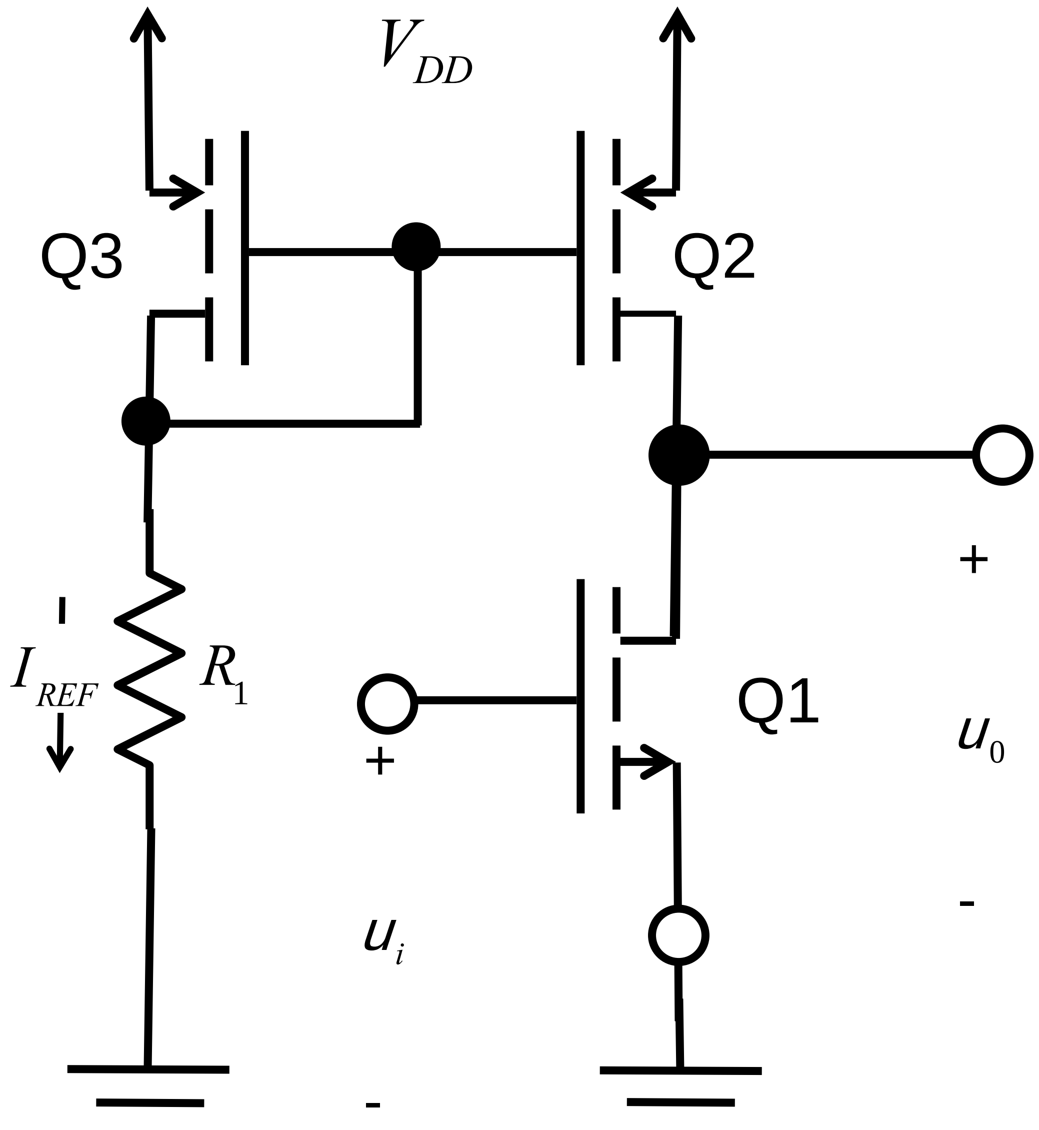
Modern BJTs:

$$V_A \approx 5 - 35\ \mathrm{V}$$

$$V_T = 0.026\ \mathrm{V}$$

$$A_0 \approx 200 - 1500$$

Implementation



$$A_{u_o} = -g_m \left(r_{oN} \parallel r_{oP} \right)$$

$$A_0 \approx \left(30 - 40\right)/2$$

Question:
How can we increase the gain of the basic cell?

Answer: Cascode

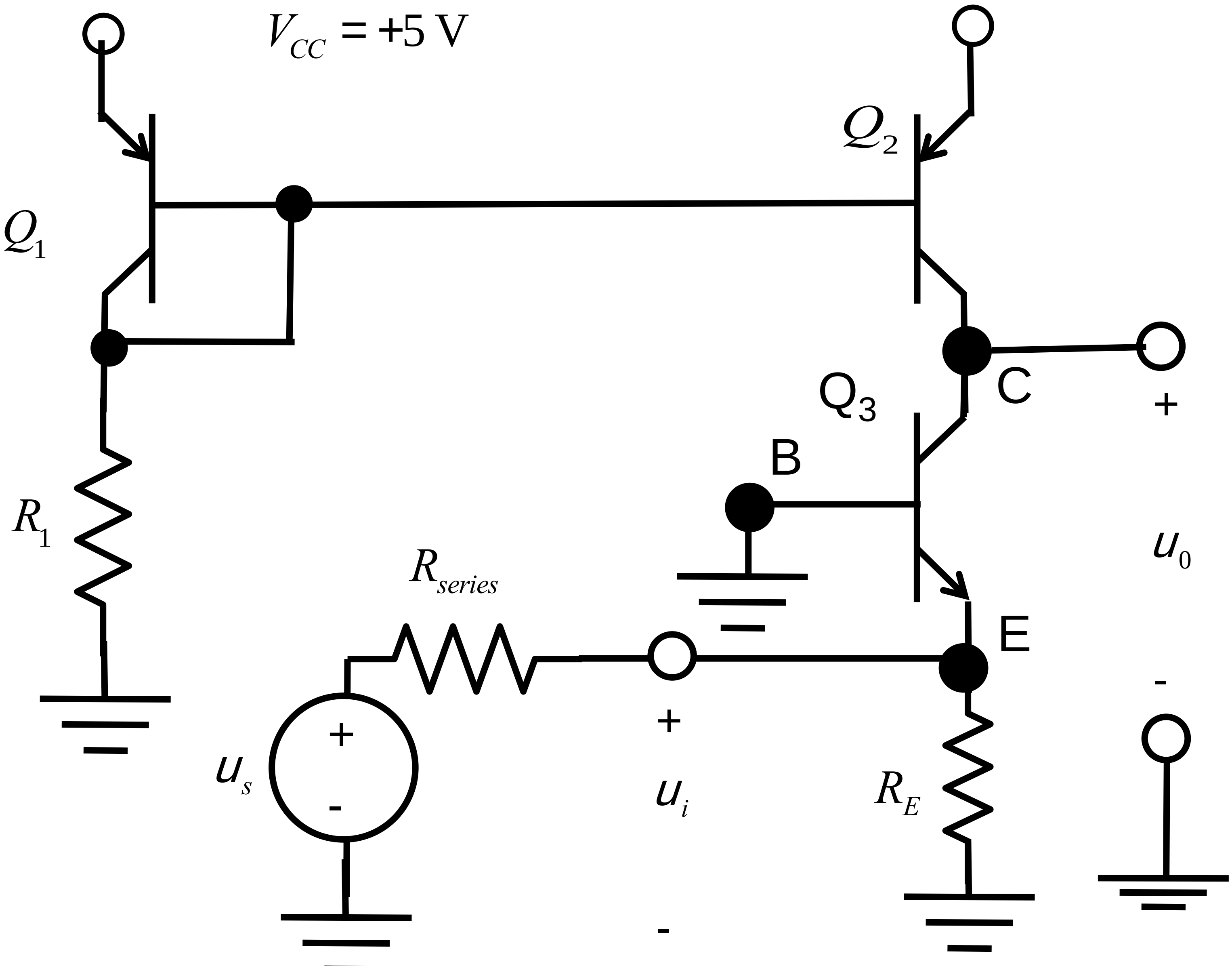
Outline

1) Finish MOSFET Current Mirrors

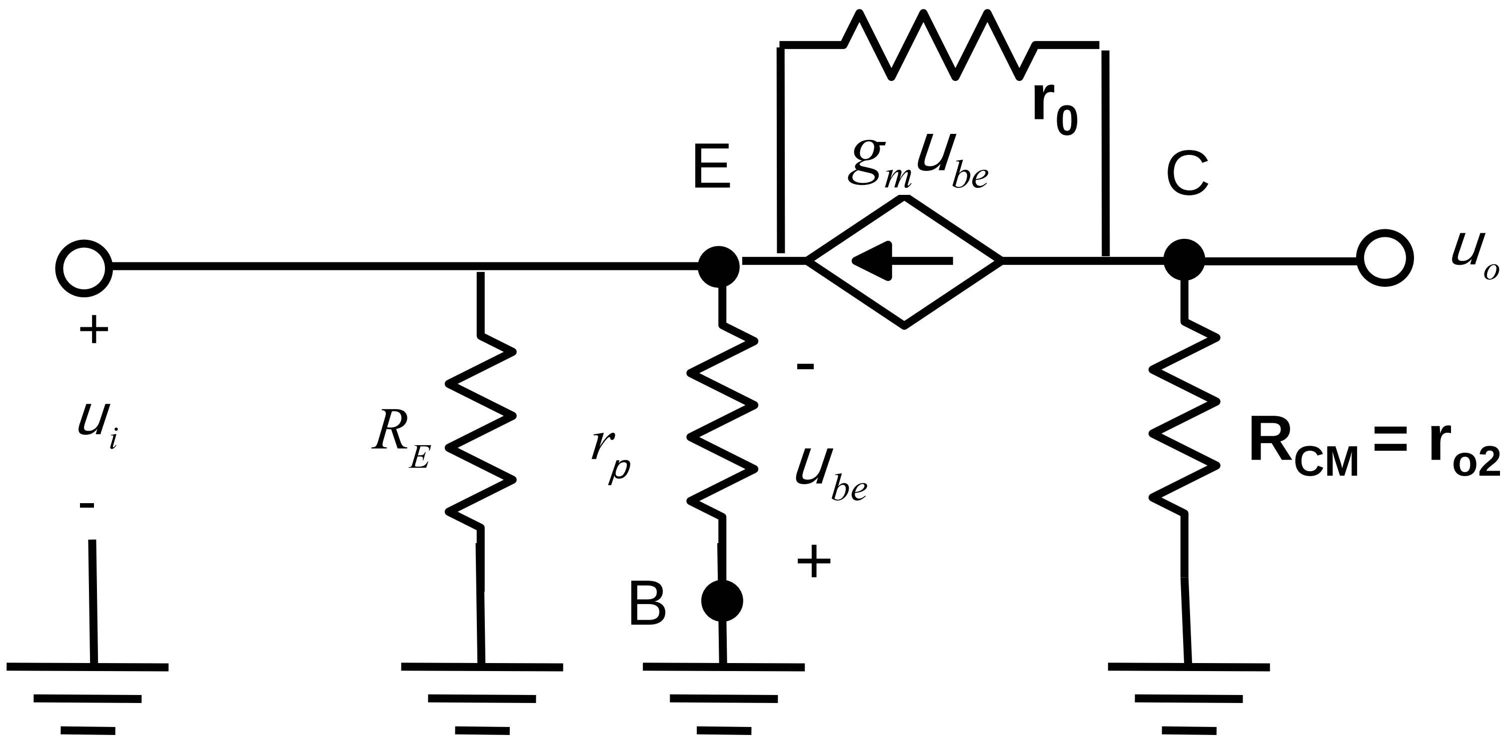
2) BJT Current Mirrors

3) **CB/GG with Active Load**

Common base

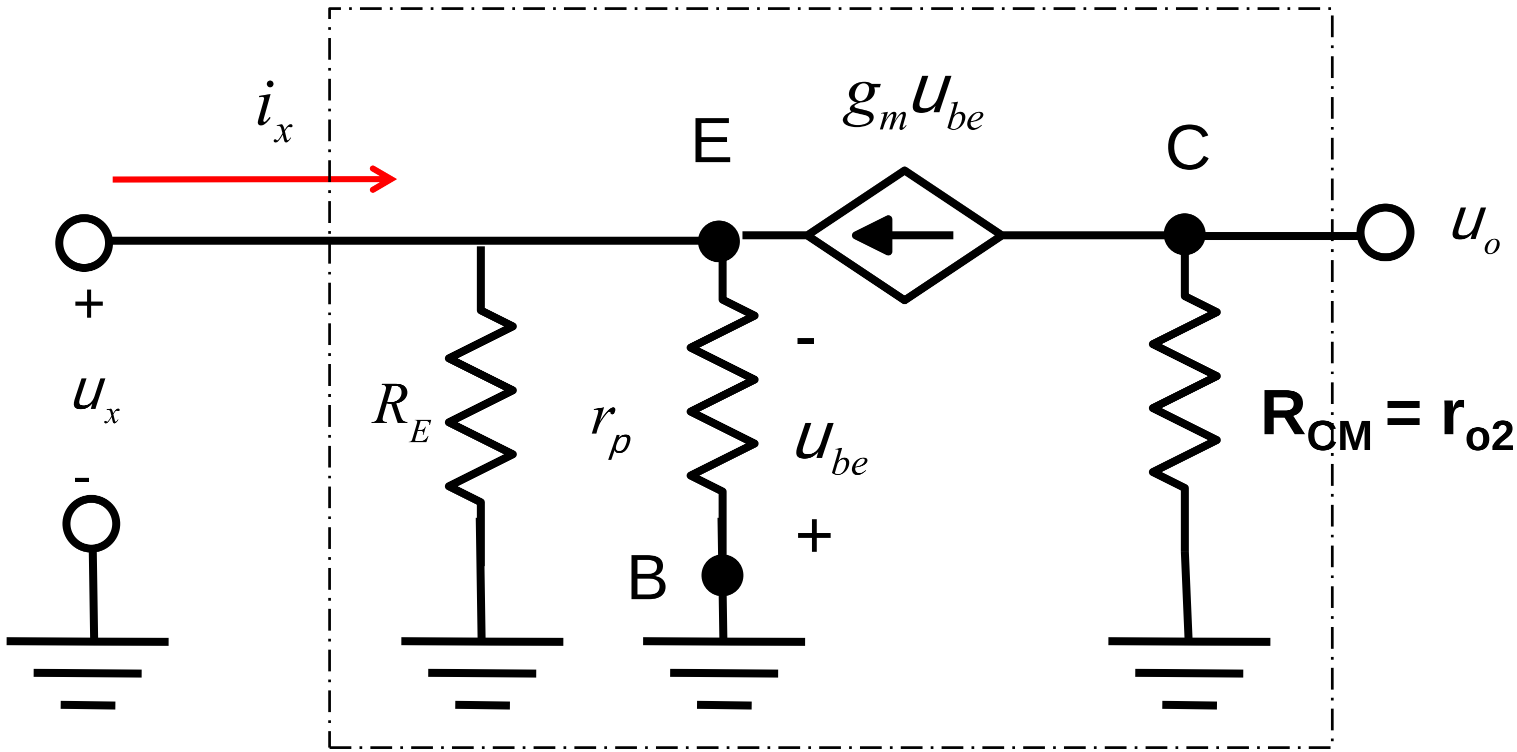


Common base amplifier



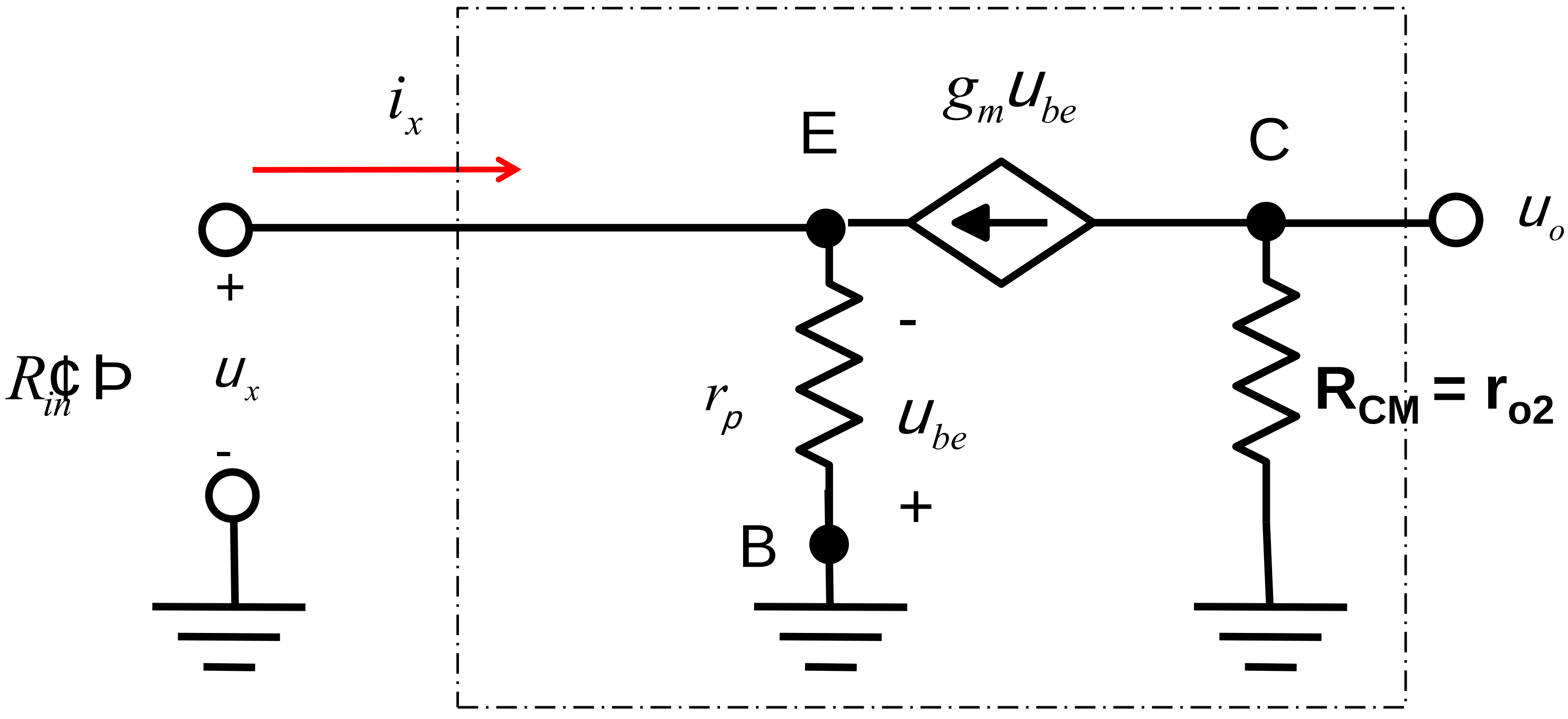
CB input resistance

R_{in} Þ



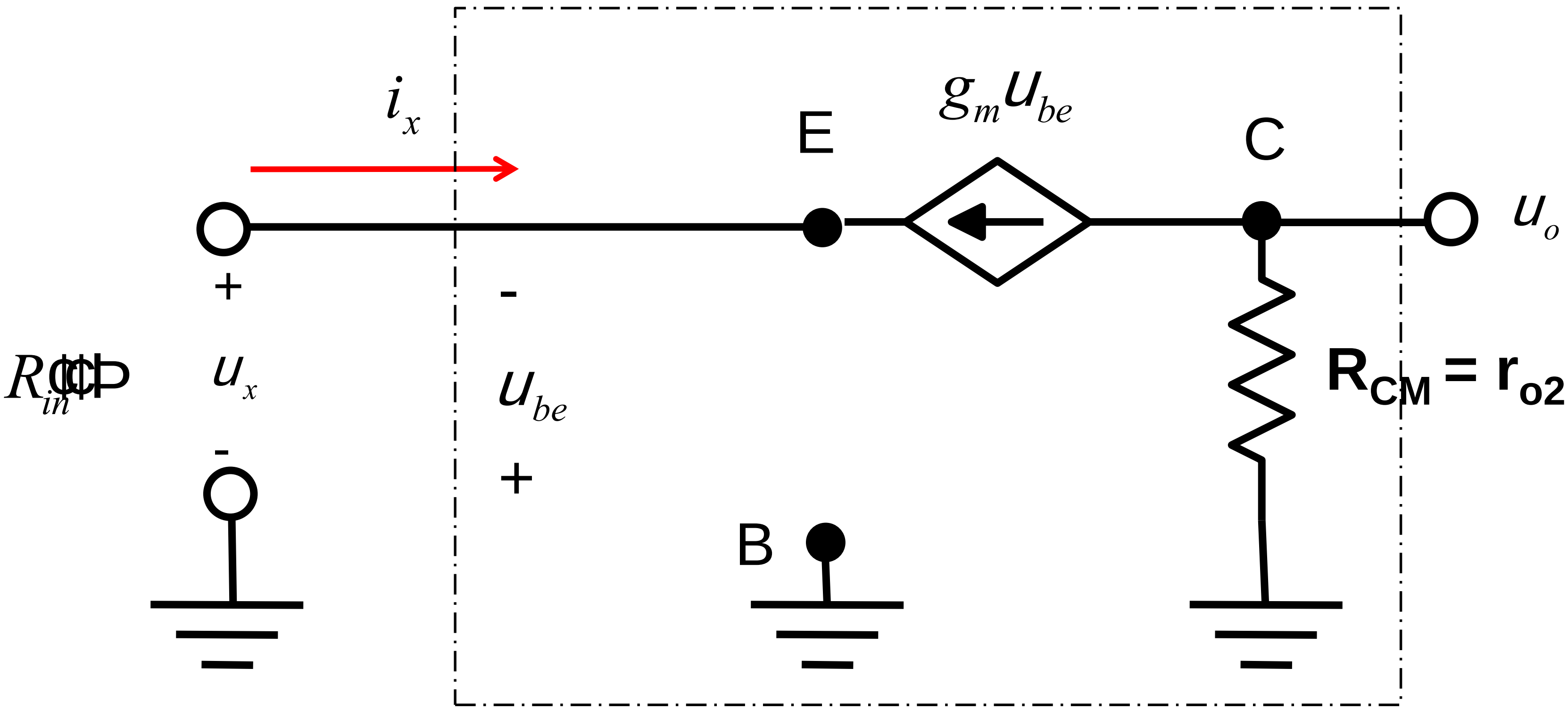
$$R_{in} = R_E \parallel ?$$

CB input resistance (ii)



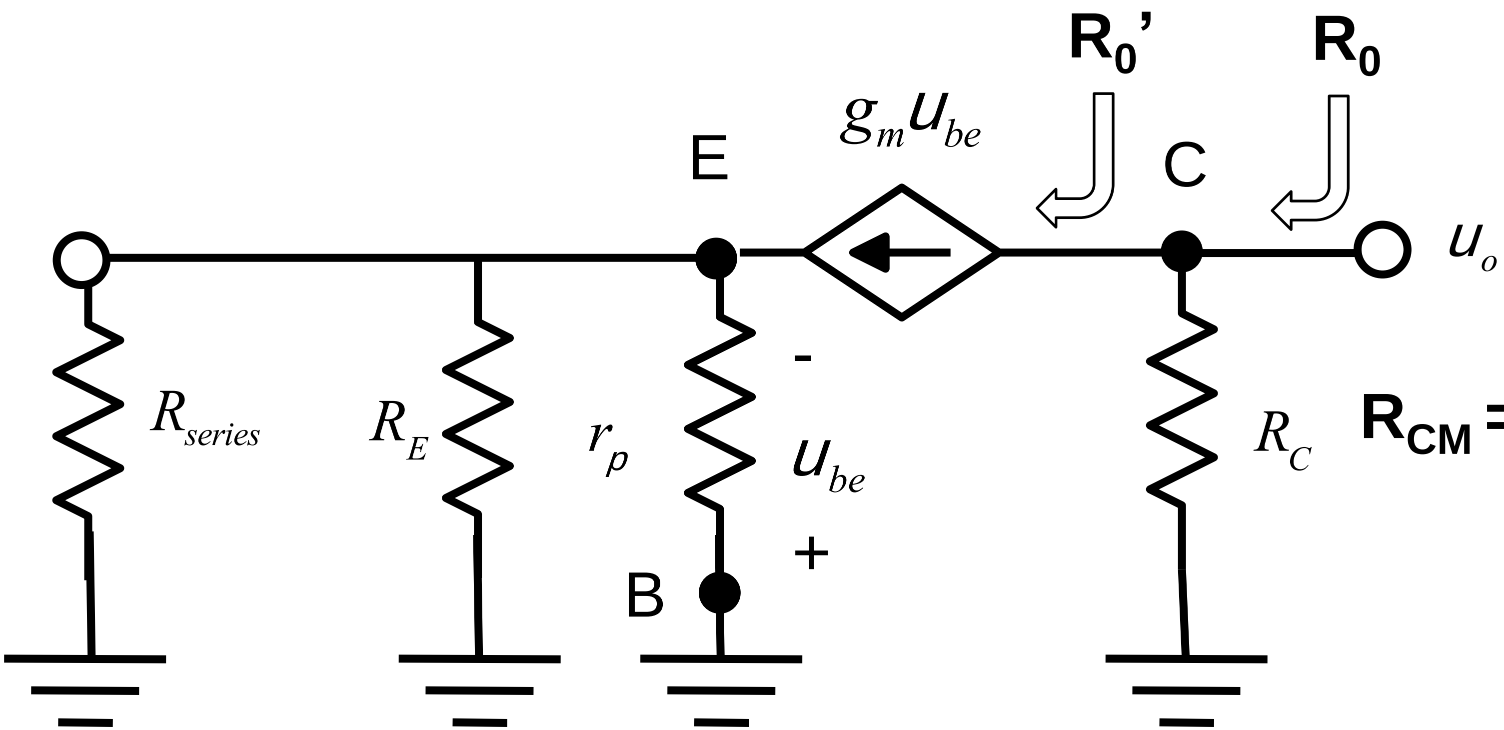
$$R_{in} = R_E \| r_\pi \| ?$$

CB input resistance (iii)



$$R_{in} = R_E \| r_\pi \| ? \qquad R_{in}' = \frac{u_x}{i_x} = \frac{u_x}{g_m u_x} = \frac{1}{g_m}$$

CB Output Resistance



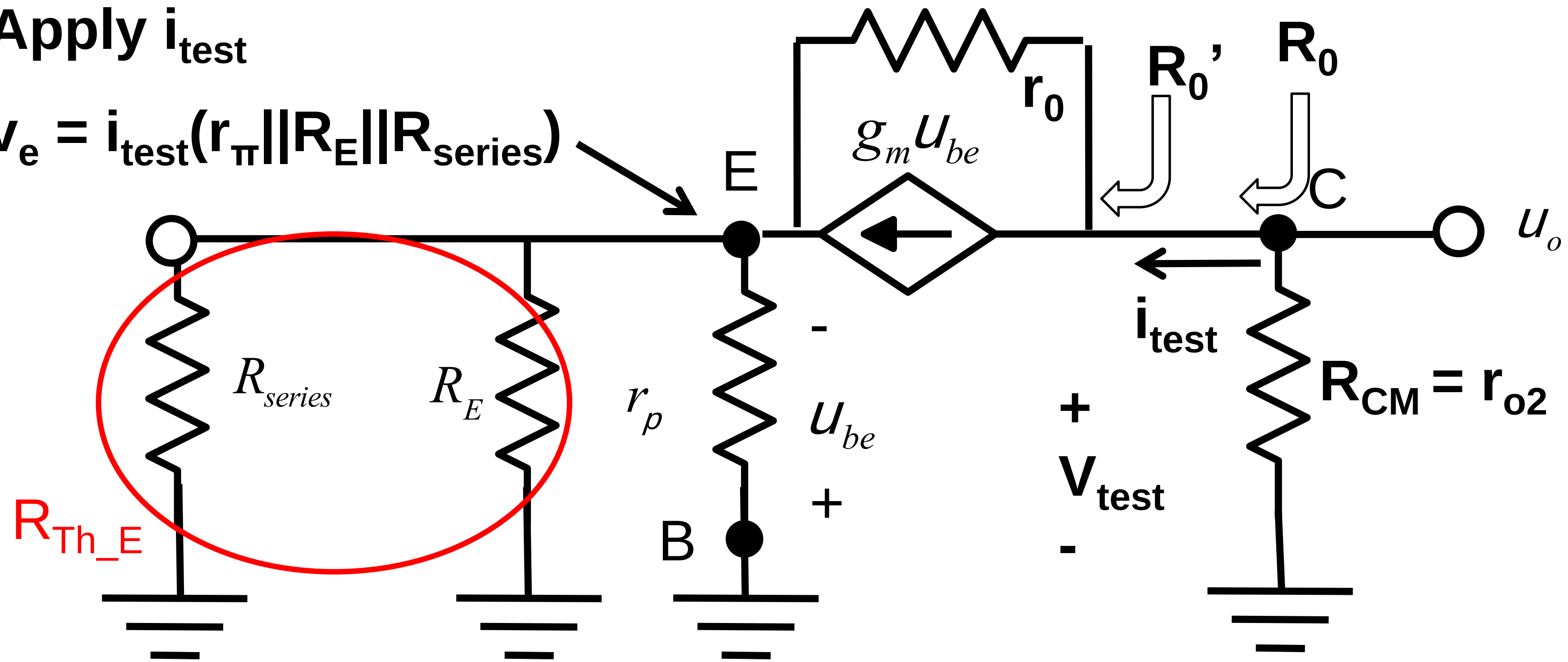
$R_{CM} = r_{o2}$

$R_0 = R_0' \| r_{02}$

CB Output Resistance

Apply i_{test}

$v_e = i_{test}(r_\pi || R_E || R_{series})$

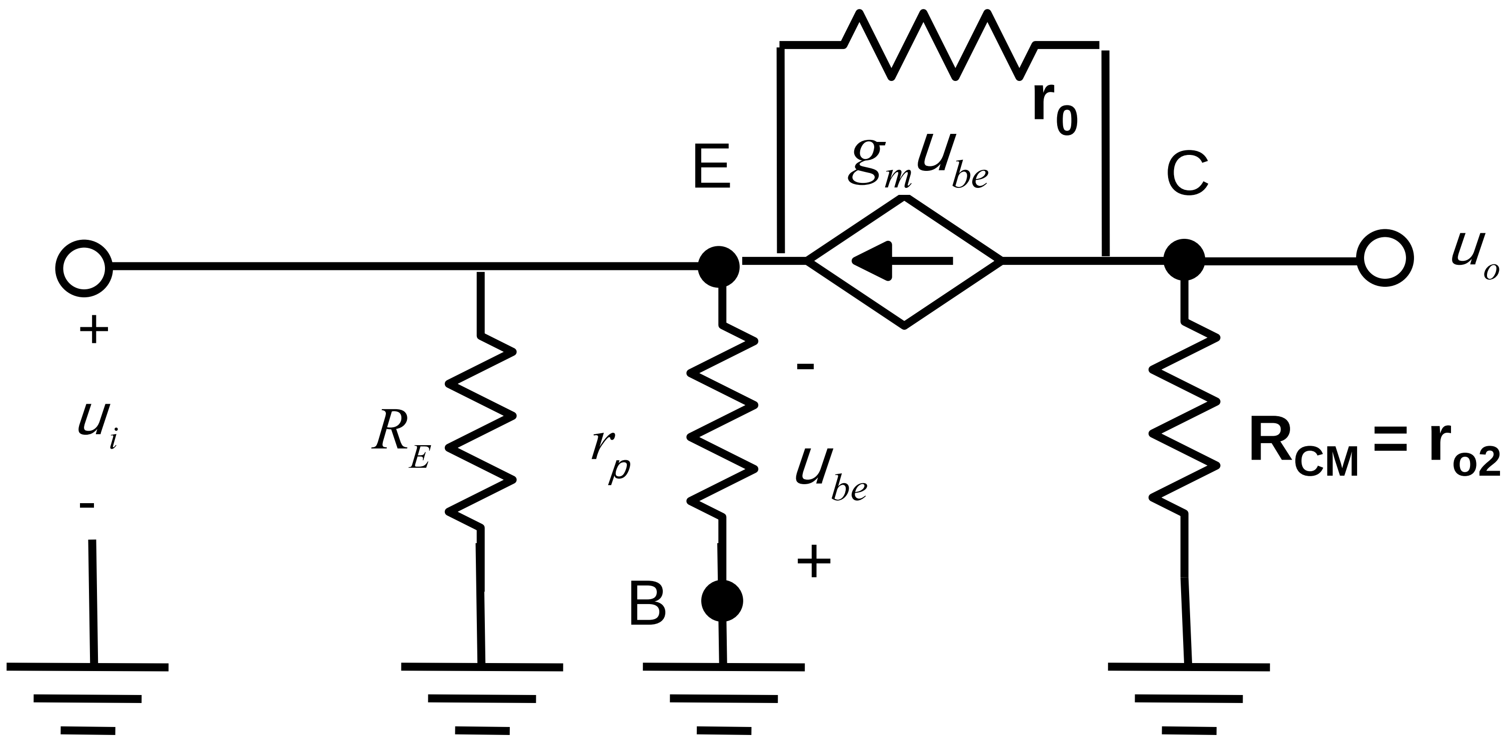


KCL at E: $0 = i_{test} - g_m v_{be} - (v_{test} - v_e)/r_o$

$0 = i_{test} + g_m v_e - (v_{test} - v_e)/r_o$

Solve for v_{test}/i_{test}: $R_0' = r_o [1 + \underbrace{g_m (r_\pi || R_E || R_{series})}_{>>1}]$

Common base amplifier



$A_V = v_o/v_i = +g_m R_{out}$

$u_{be} = - u_i$

Common base with Active Load

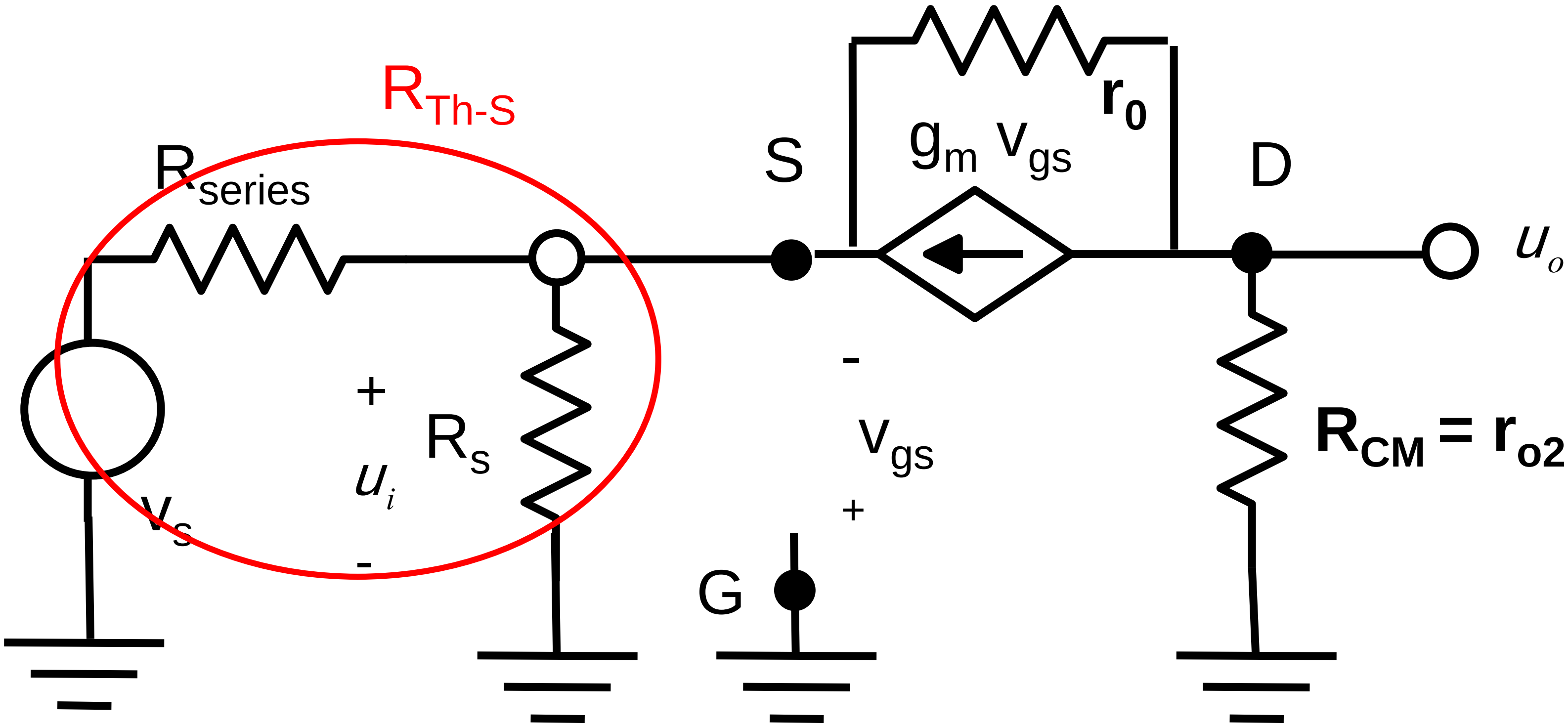
$$R_{in} = R_E \,||\, r_p \,||\, \frac{1}{g_m}$$

$$\mathbf{R_0 = R_0' \,||\, R_{CM} = R_0' \,||\, r_{o2}}$$

$$\mathbf{R_0' = r_o\,[1 + g_m\,(r_\pi||R_E||R_{series})] = r_o\,[1 + g_m\,(r_\pi||R_{Th\text{-}E})]}$$

$$A_V = v_o/v_i = +g_m\, R_{out}$$

Common gate amplifier



Common gate with Active Load

$$\mathbf{R_{in} = R_S \,||\, 1/g_m}$$

$$\mathbf{R_0 = R_0' \,||\, R_{CM} = R_0' \,||\, r_{o2}}$$

$$\mathbf{R_0' = r_o\,[1 + g_m\,(R_S||R_{series})] = r_o\,[1 + g_m\,(R_{Th\text{-}S})}$$

$$A_V = v_o/v_i = +g_m\,R_{out}$$