Spring 2019 Purdue University

ECE 255: L31

CMOS Op Amps

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Announcements

HW9 Due 5:00 PM Friday, April 12 in EE-209 dropbox

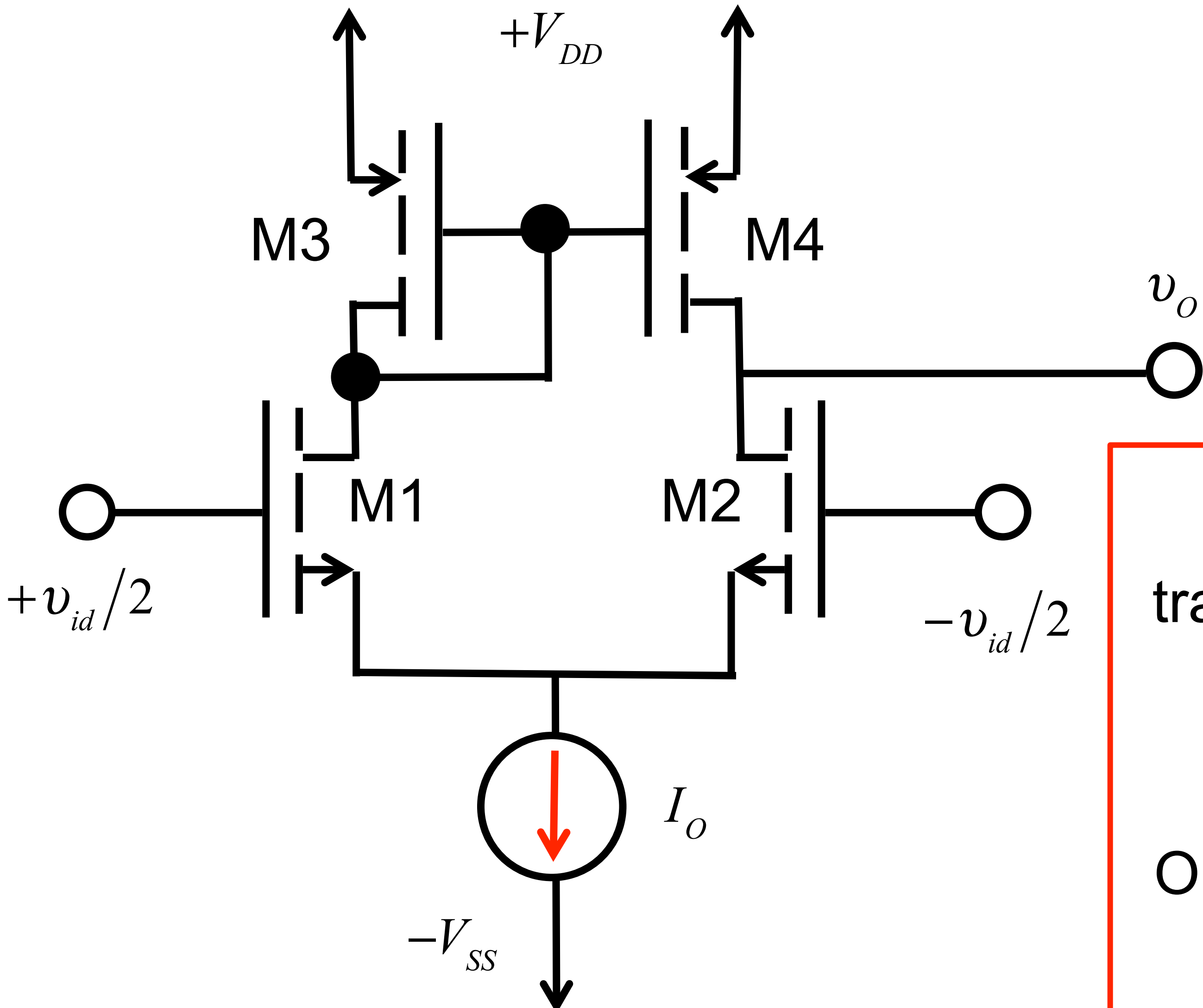
Outline

1) Review

2) PMOS input version

3) Two-Stage Op Amps (PMOS input)

CM loaded differential pair



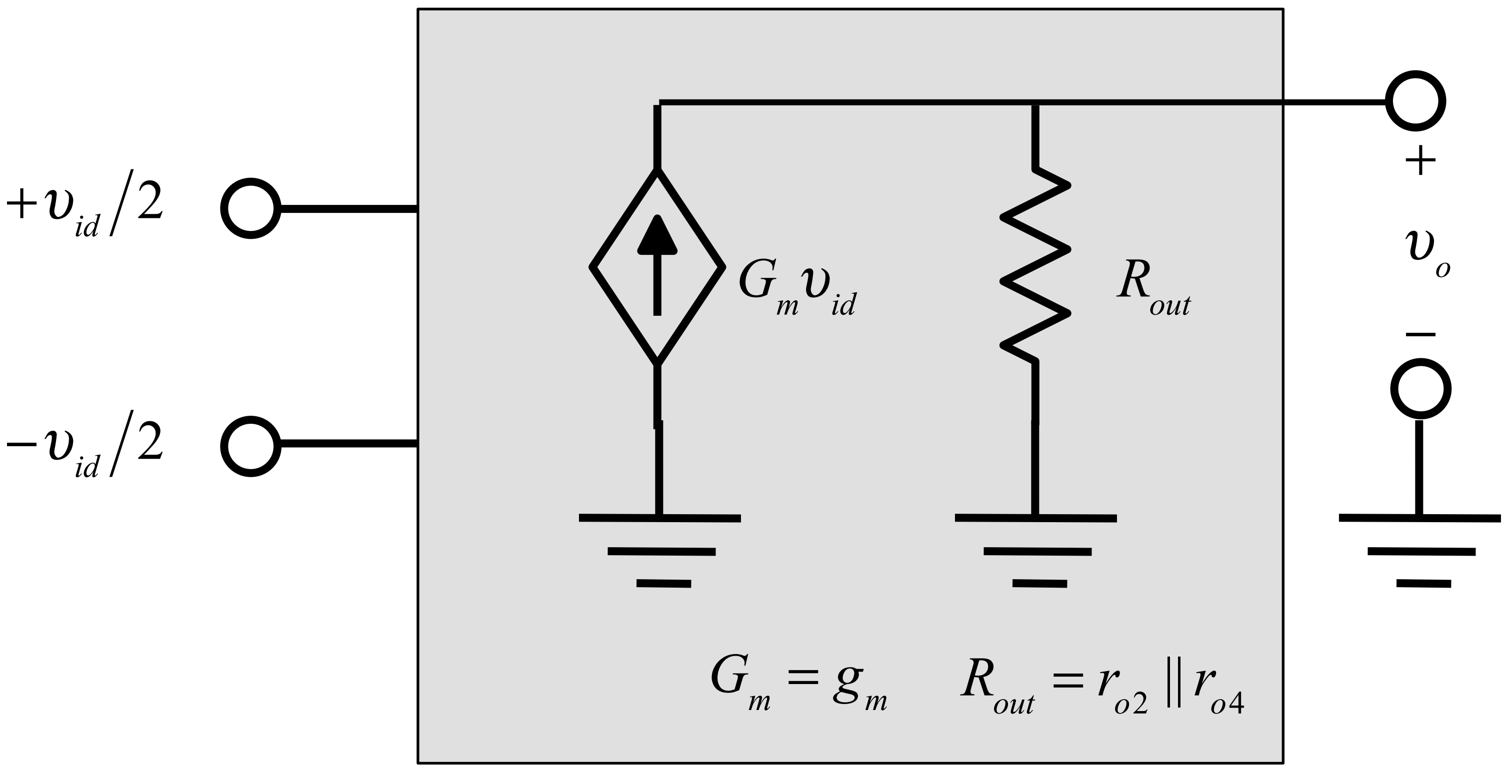
Short-circuit transconductance

$$G_m \equiv \frac{i_o}{v_{id}} = g_m$$

Output resistance

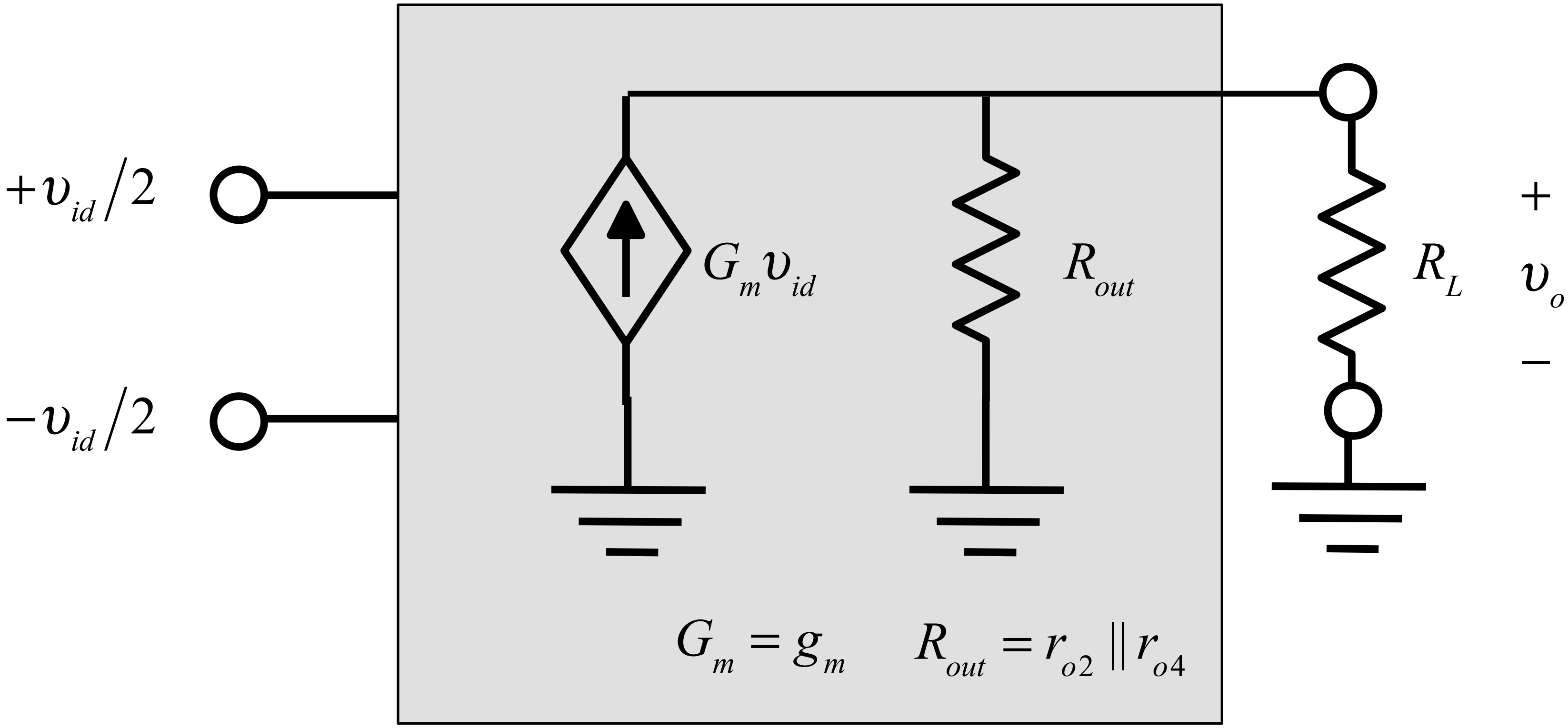
$$R_{out} = r_{o2} \parallel r_{o4}$$4

CM loaded differential pair: equivalent circuit



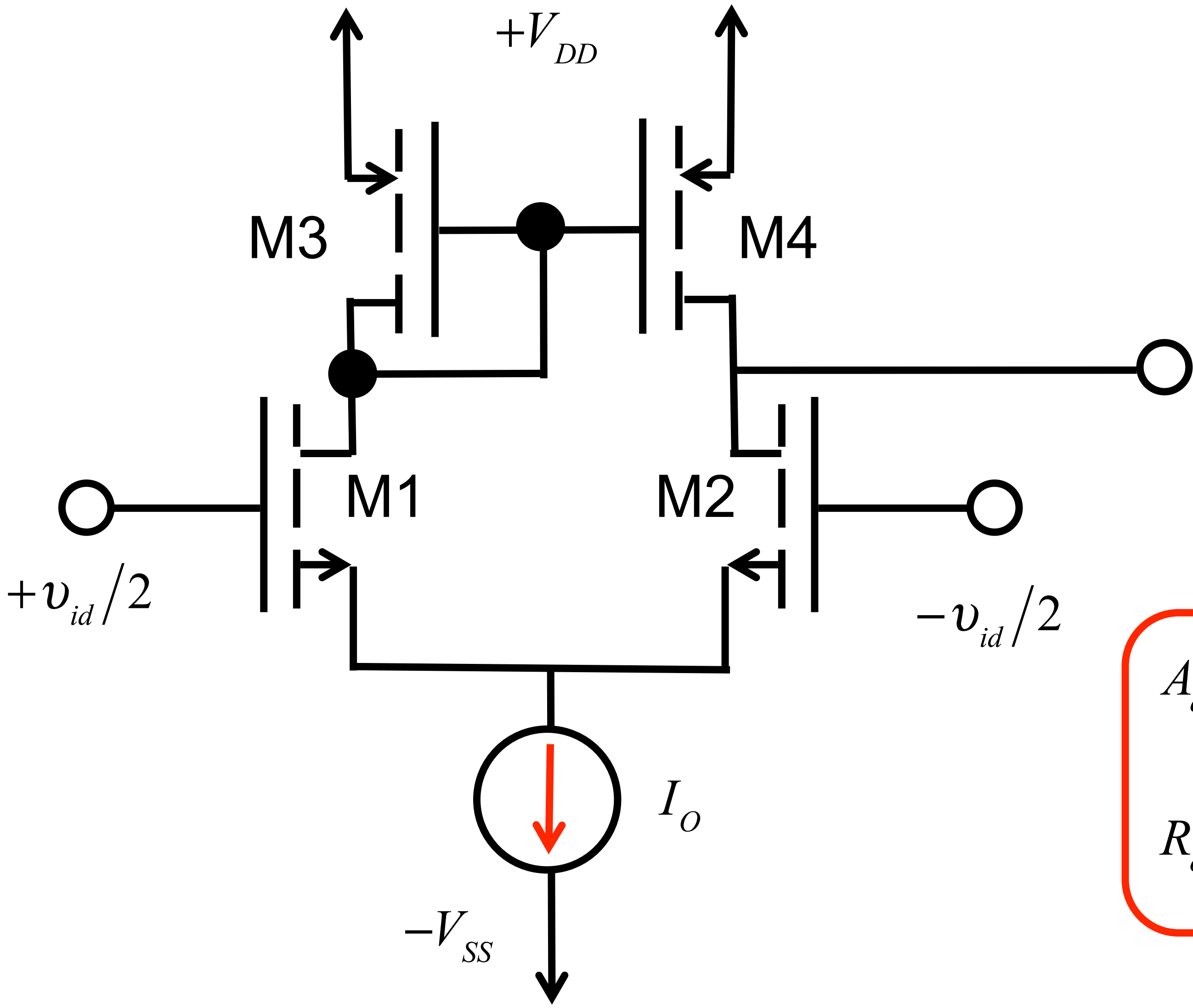
$$v_o = G_m v_{id} R_{out} = g_m v_{id} \left(r_{o2} \parallel r_{o4} \right)$$

CM loaded differential pair: With load



$$\upsilon_o = G_m \upsilon_{id} R_{out} \| R_L = g_m \upsilon_{id} \left(r_{o2} \| r_{o4} \right) \| R_L$$

CM loaded differential pair

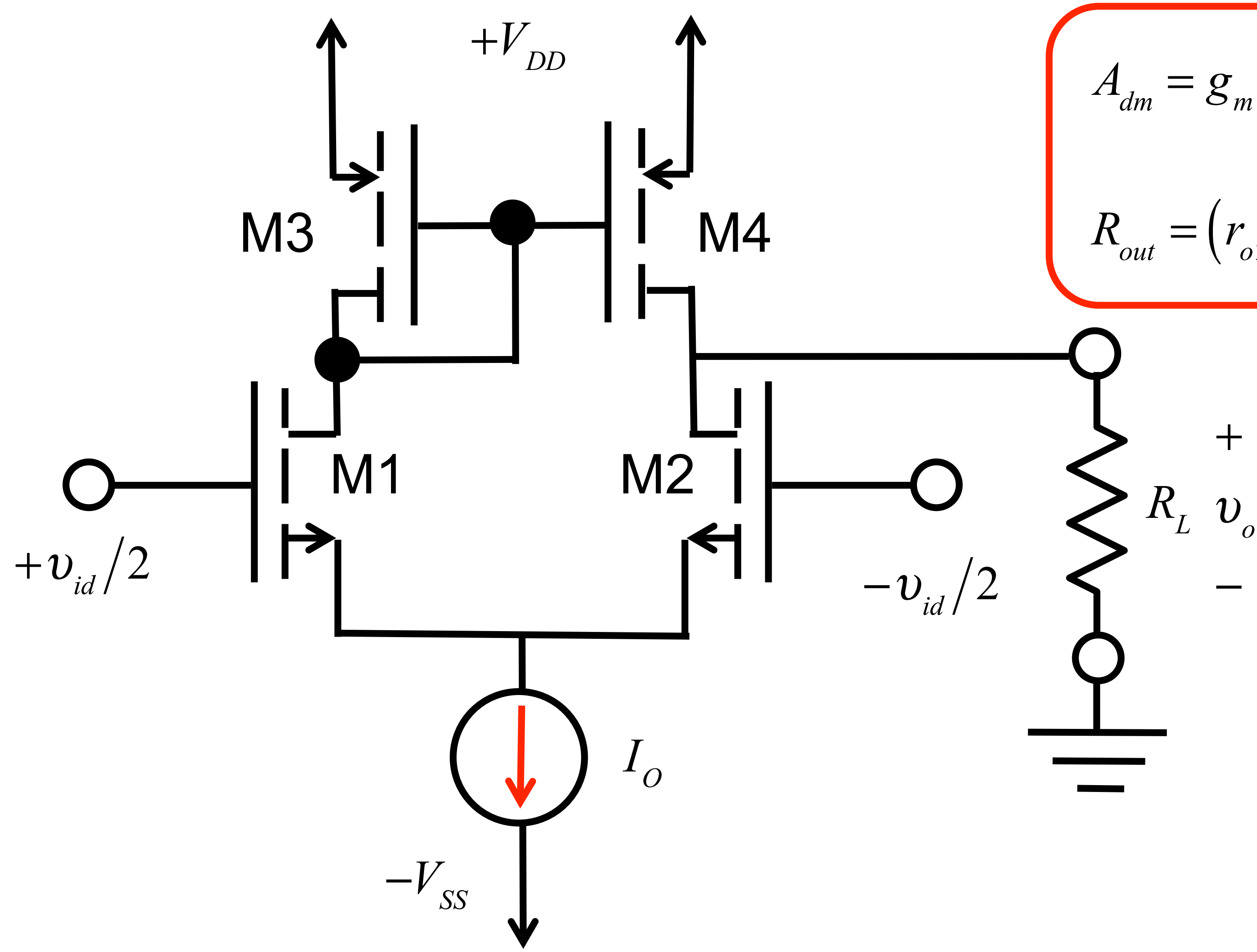


$$\upsilon_o = G_m \upsilon_{id} R_{out}$$

$$A_{dm} = g_m \left(r_{o2} \parallel r_{o4} \right)$$

$$R_{out} = \left(r_{o2} \parallel r_{o4} \right)$$

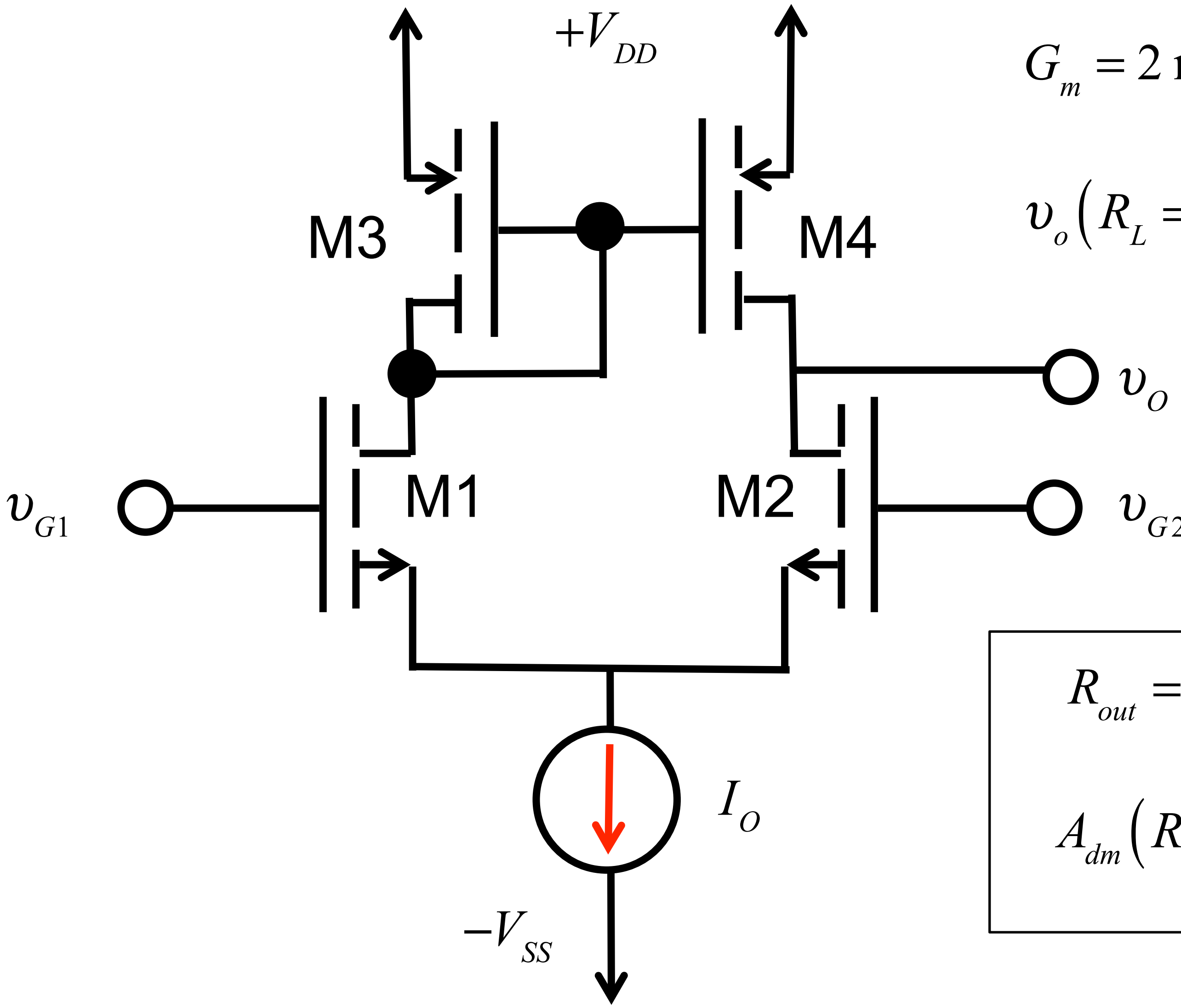
CM loaded differential pair: With load



$$A_{dm} = g_m\left(r_{o2} \parallel r_{o4}\right) \parallel R_L$$

$$R_{out} = \left(r_{o2} \parallel r_{o4}\right)$$

Problem 9.85



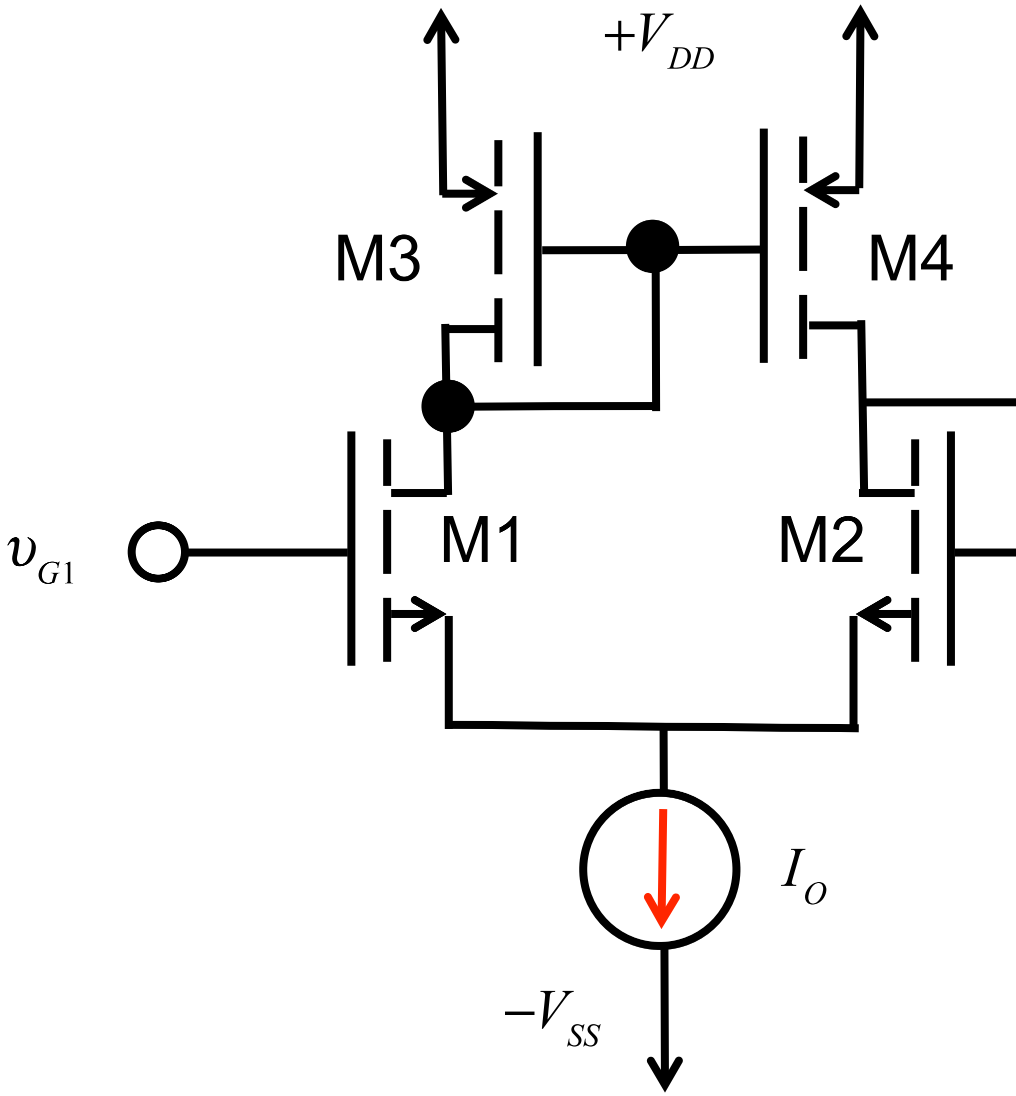
$$G_m = 2\ \text{mA/V}$$

$$\upsilon_o\left(R_L = 20\ \text{k}\right) = \frac{\upsilon_o\left(R_L = \infty\right)}{2}$$

$$R_{out} = ?$$

$$A_{dm}\left(R_L = \infty\right) = ?$$

Problem 9.86

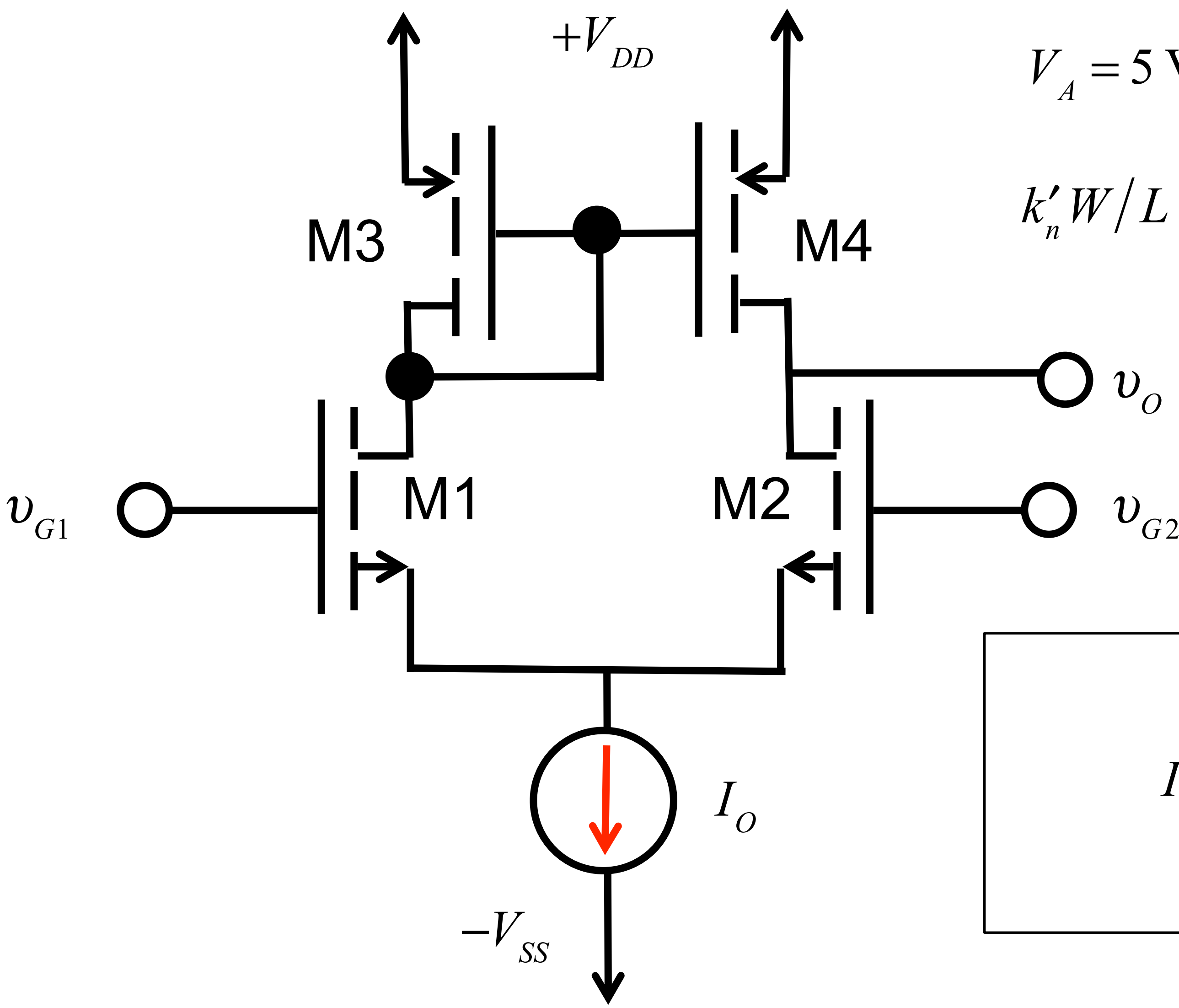


$V_A' = 5\ \text{V}/\mu\text{m}$ $\quad L = 0.5\ \mu\text{m}$

$V_{GS} - V_{tn} = 0.25\ \text{V}$

$A_{dm}\left(R_L = \infty\right) = ?$

Problem 9.88



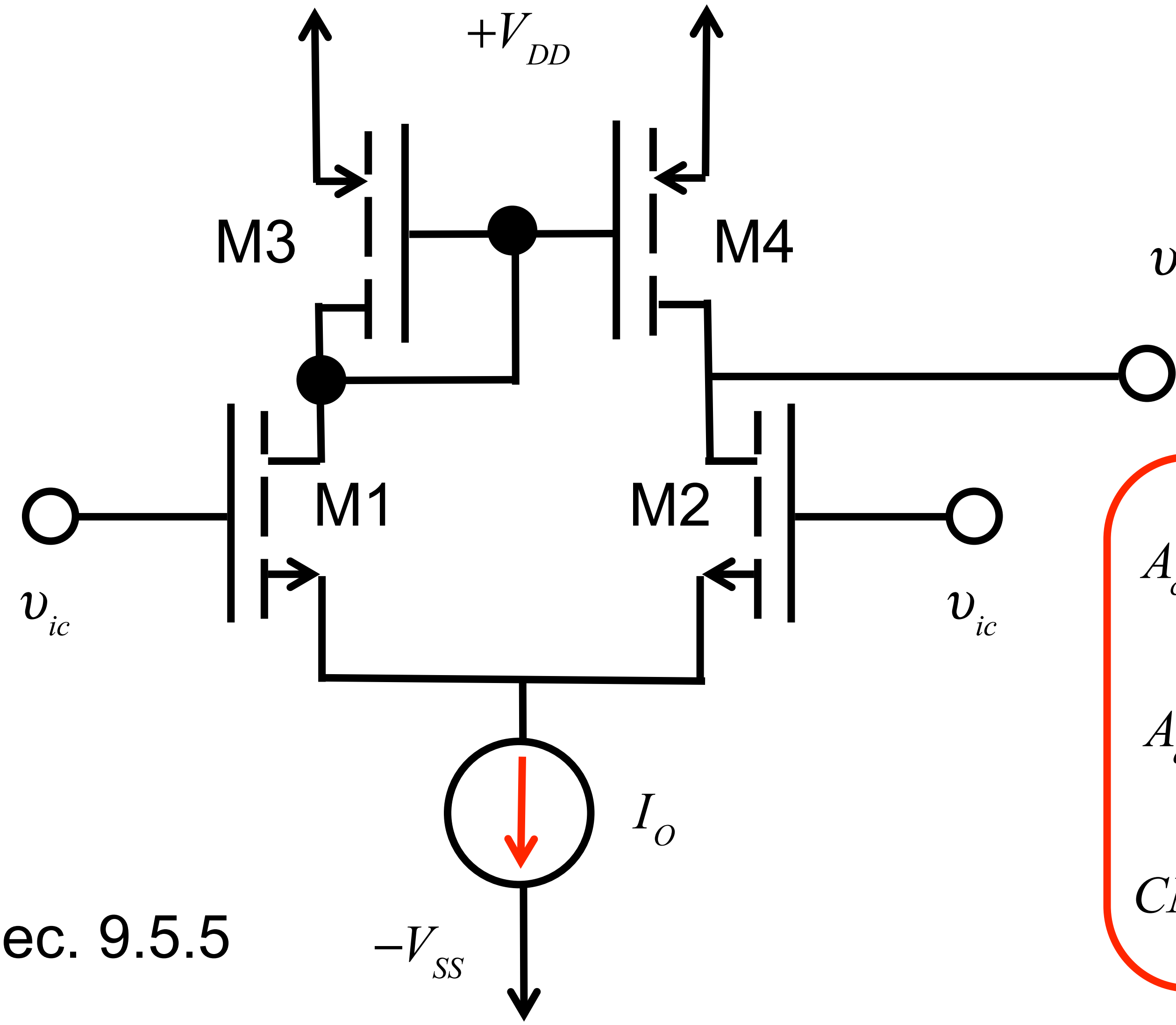
$V_A = 5\text{ V}$

$A_{dm} = 20$

$k_n' W/L = k_n = 4\text{ mA/V}^2$

$I_0 = ?$

Common mode gain and CMRR



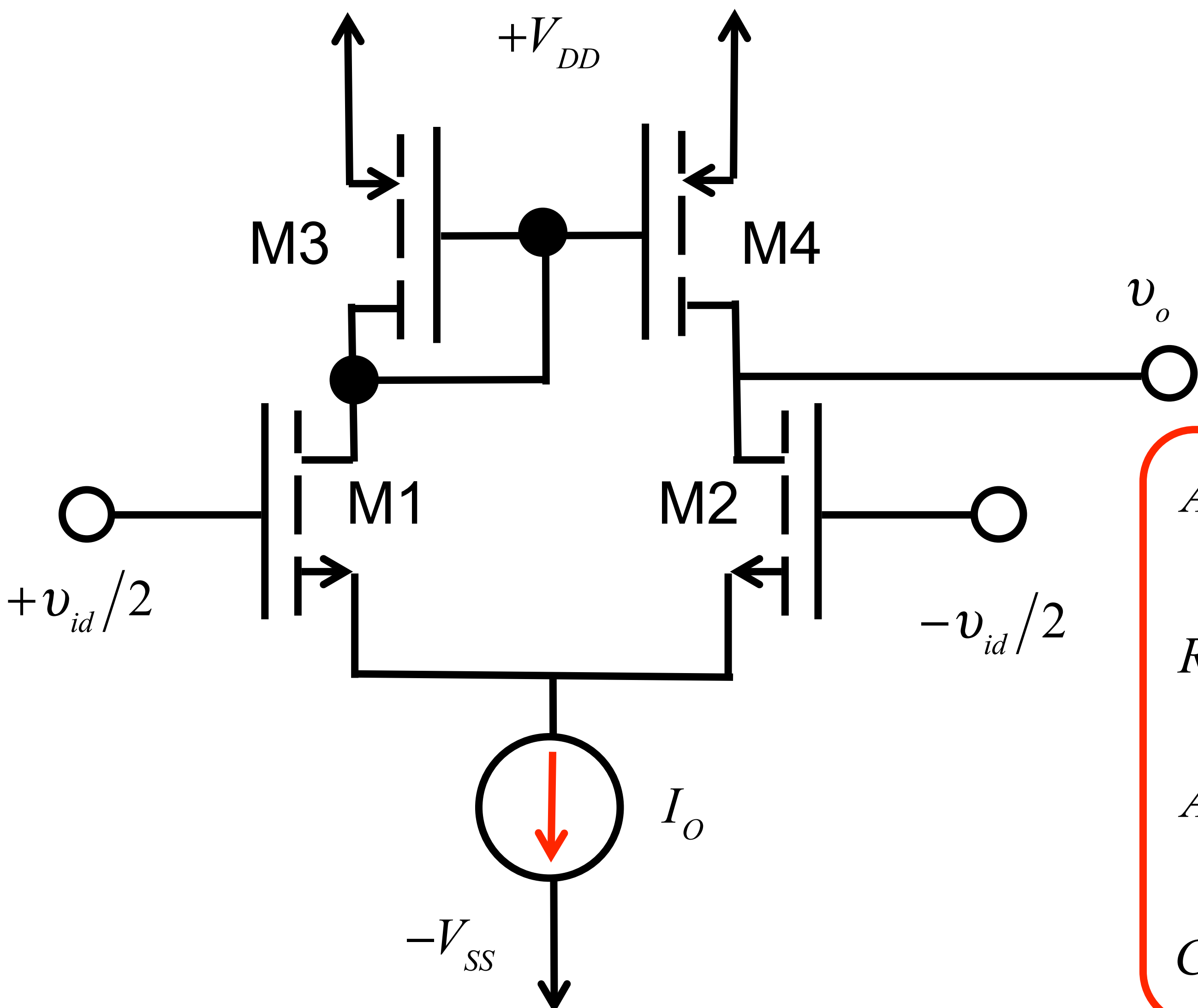
$$A_{cm} \approx -\frac{1}{2g_{m3}R_{SS}}$$

$$A_{dm} = g_m\left(r_{o2} \parallel r_{o4}\right)$$

$$CMRR = \left|A_{dm}\right| / \left|A_{cm}\right|$$

Sec. 9.5.5

CM loaded differential pair



$$A_{dm} = g_m \left(r_{o2} \parallel r_{o4} \right)$$

$$R_{out} = \left(r_{o2} \parallel r_{o4} \right)$$

$$A_{cm} \approx -\frac{1}{2 g_{m3} R_{SS}}$$

$$CMRR = \left| A_{dm} \right| / \left| A_{cm} \right|$$

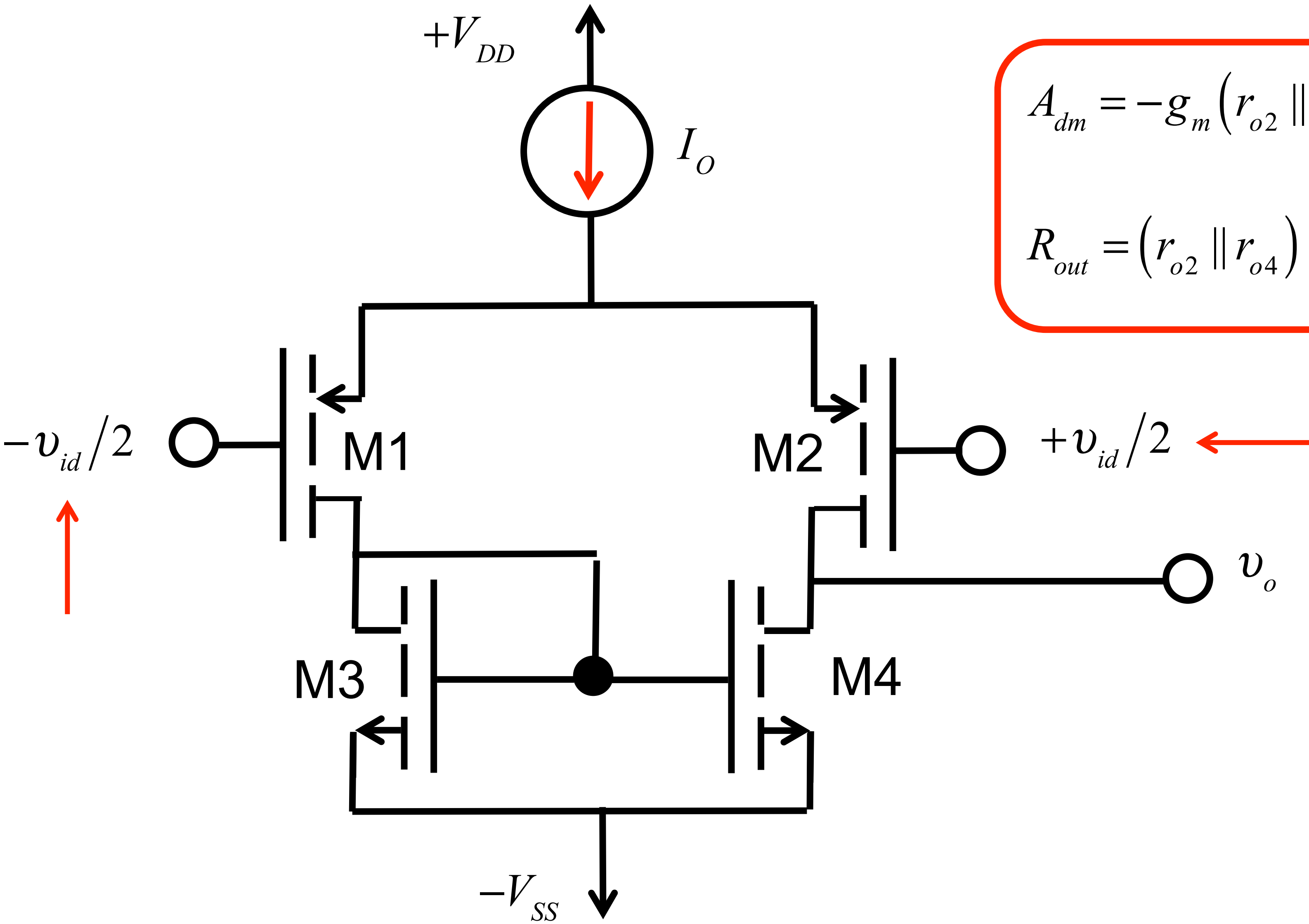
Outline

1) Review

2) **PMOS input version**

3) Two-Stage Op Amps (PMOS input)

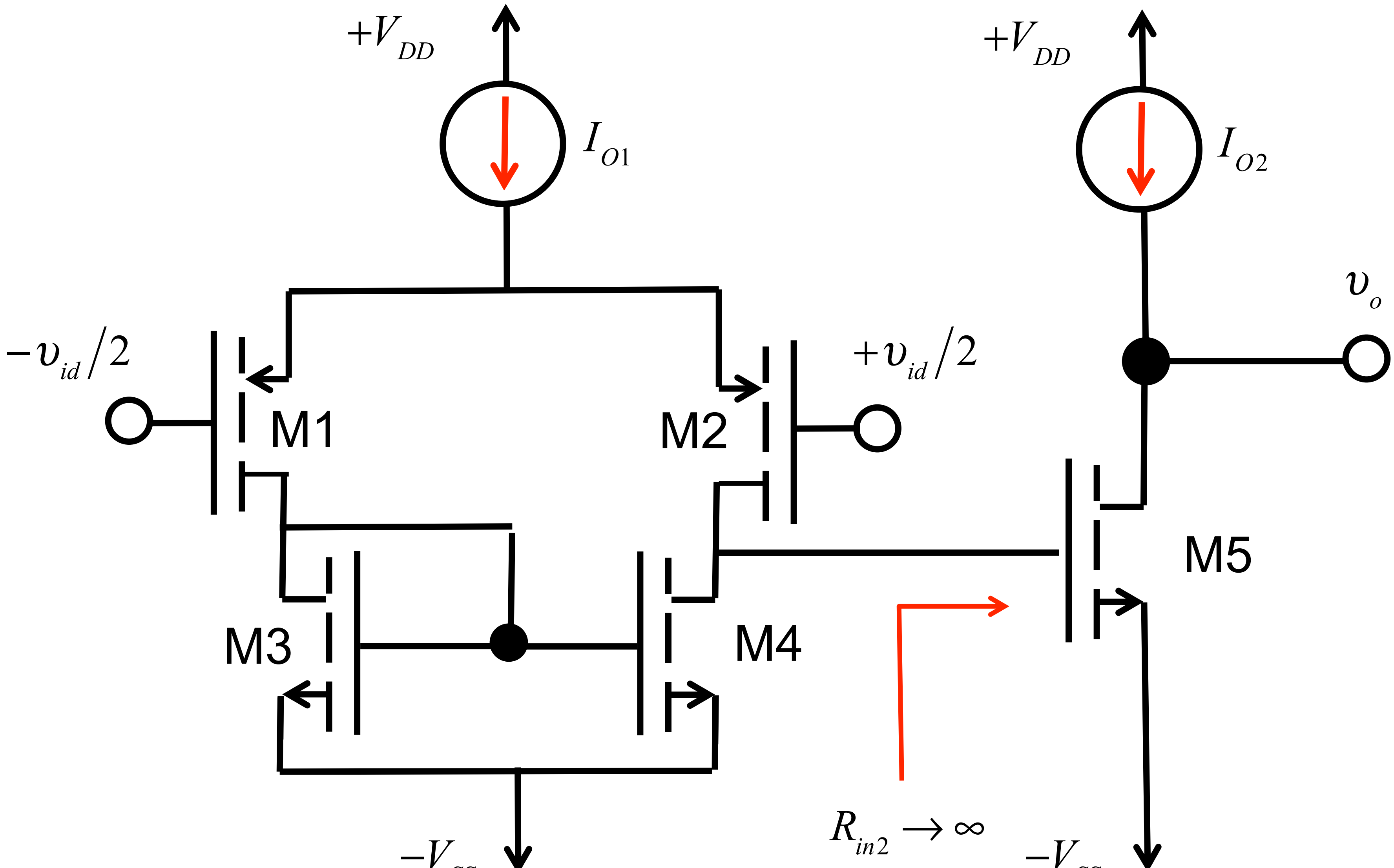
PMOS input differential pair



$$A_{dm} = -g_m\left(r_{o2} \parallel r_{o4}\right)$$

$$R_{out} = \left(r_{o2} \parallel r_{o4}\right)$$

2-stage CMOS Op Amp



CMOS Op Amp

$$A_{dm} = A_{dm1} \times A_{CS}$$

$$A_{dm} = -g_m \left(r_{o2} \parallel r_{o4} \right) \times \left[-g_{m5} \left(r_{o5} \parallel R_{ocs} \right) \right]$$

$$A_{cm} = A_{cm1} \times A_{CS}$$

$$A_{cm} \approx -\frac{1}{2 g_{m3} R_{SS}} \times \left[-g_{m5} \left(r_{o5} \parallel R_{ocs} \right) \right]$$

$$CMRR = \frac{\left| A_{dm} \right|}{\left| A_{cm} \right|}$$

Two-stage CMOS Op Amp

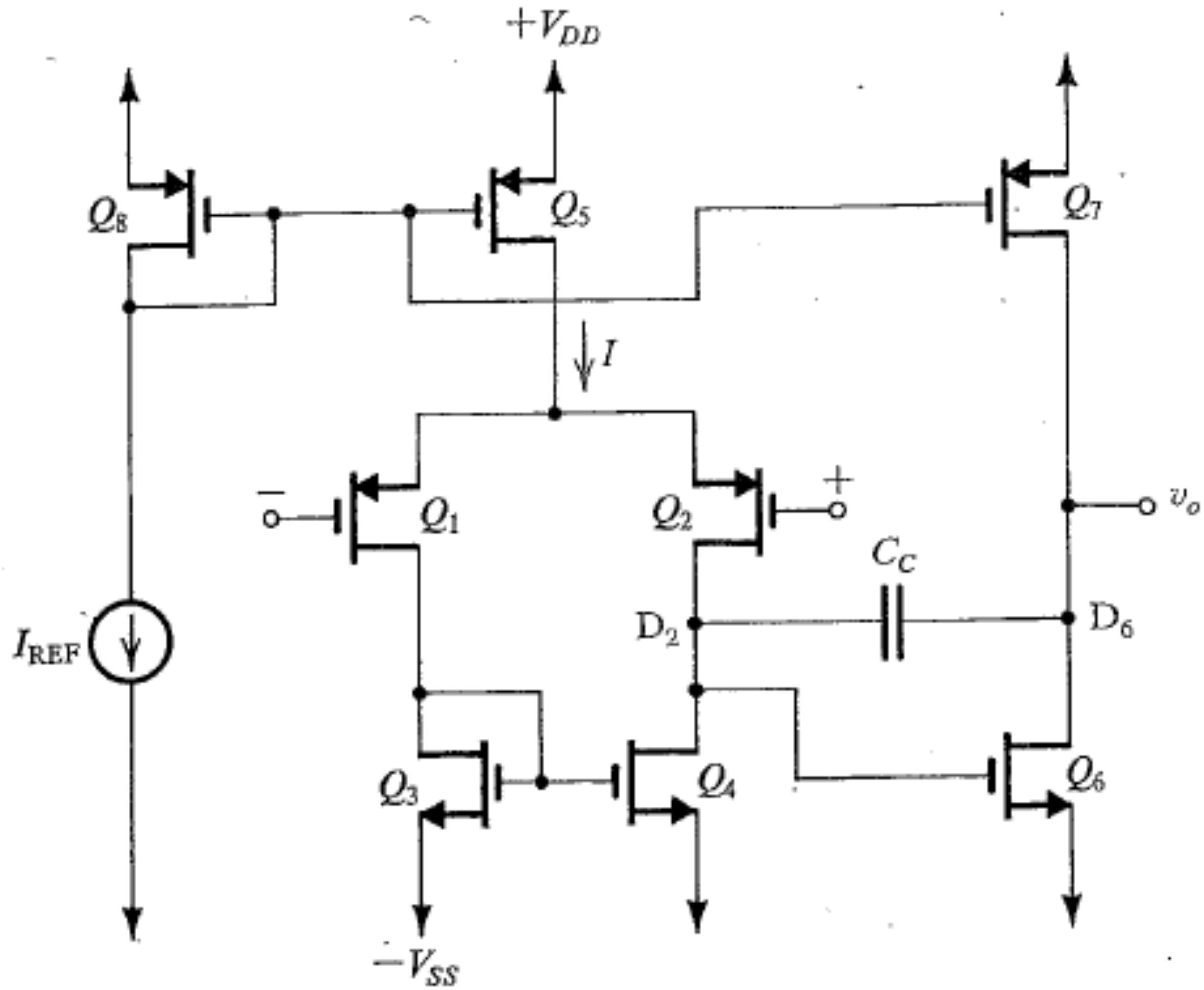
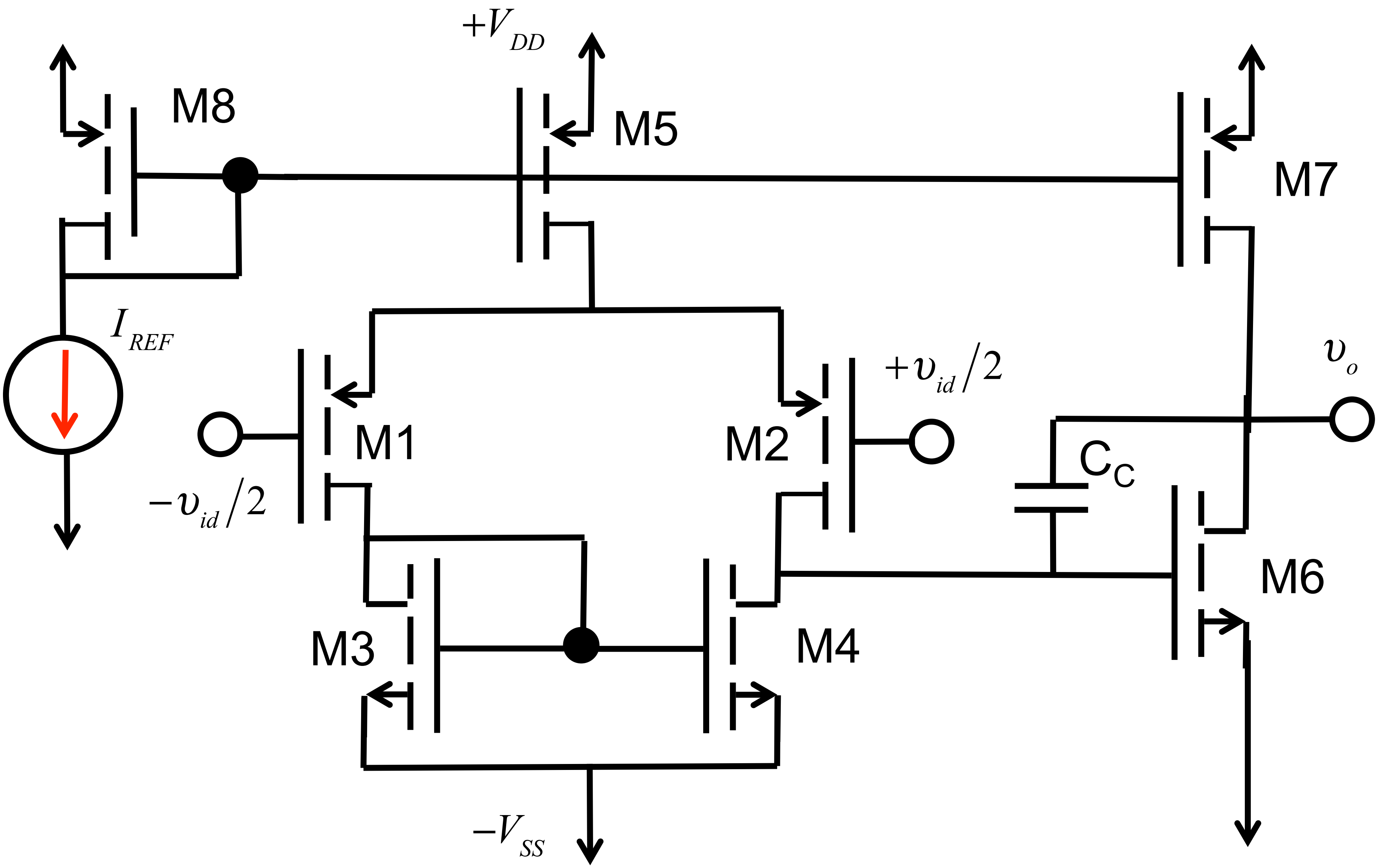


Fig. 9.40 Sedra and Smith 7th Ed.

Two-stage CMOS Op Amp



Two-stage CMOS Op Amp

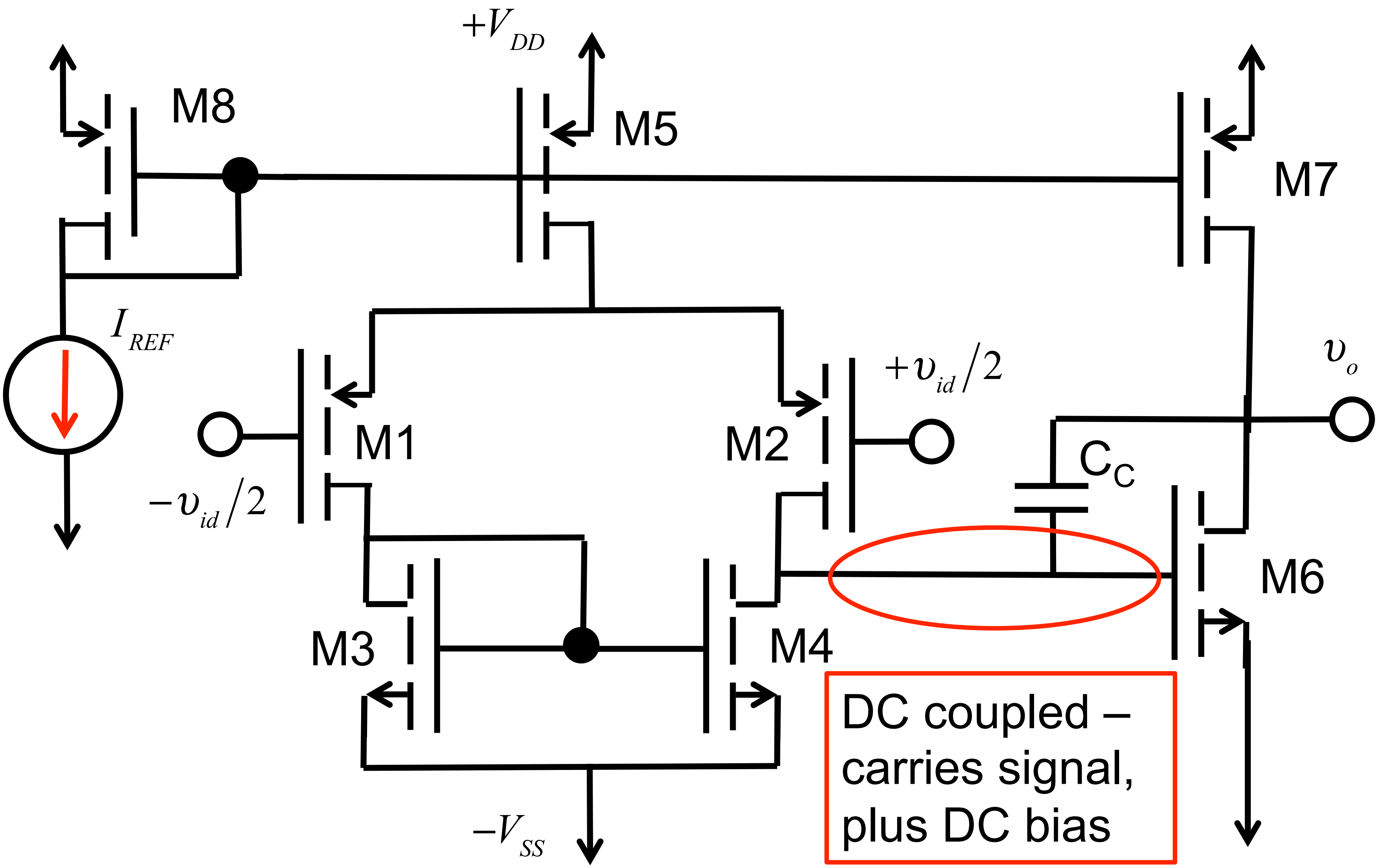
$$A_{dm} = A_{dm1} \times A_{CS}$$

$$A_{dm} = -g_m\left(r_{o2} \parallel r_{o4}\right) \times \left[-g_{m6}\left(r_{o6} \parallel r_{07}\right)\right] = \left(\frac{g_m r_o}{2}\right)^2$$

$$A_{dm} = \left(\frac{g_m r_o}{2}\right)^2$$

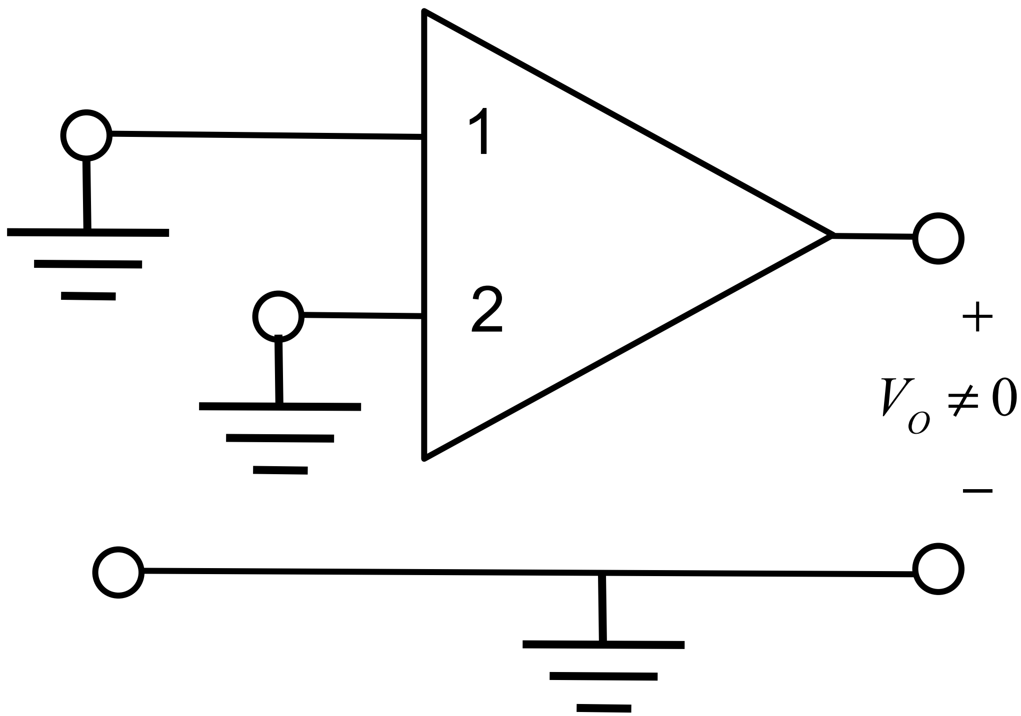
$$R_{out} = \left(\frac{r_o}{2}\right)$$

Two-stage CMOS Op Amp: DC coupling

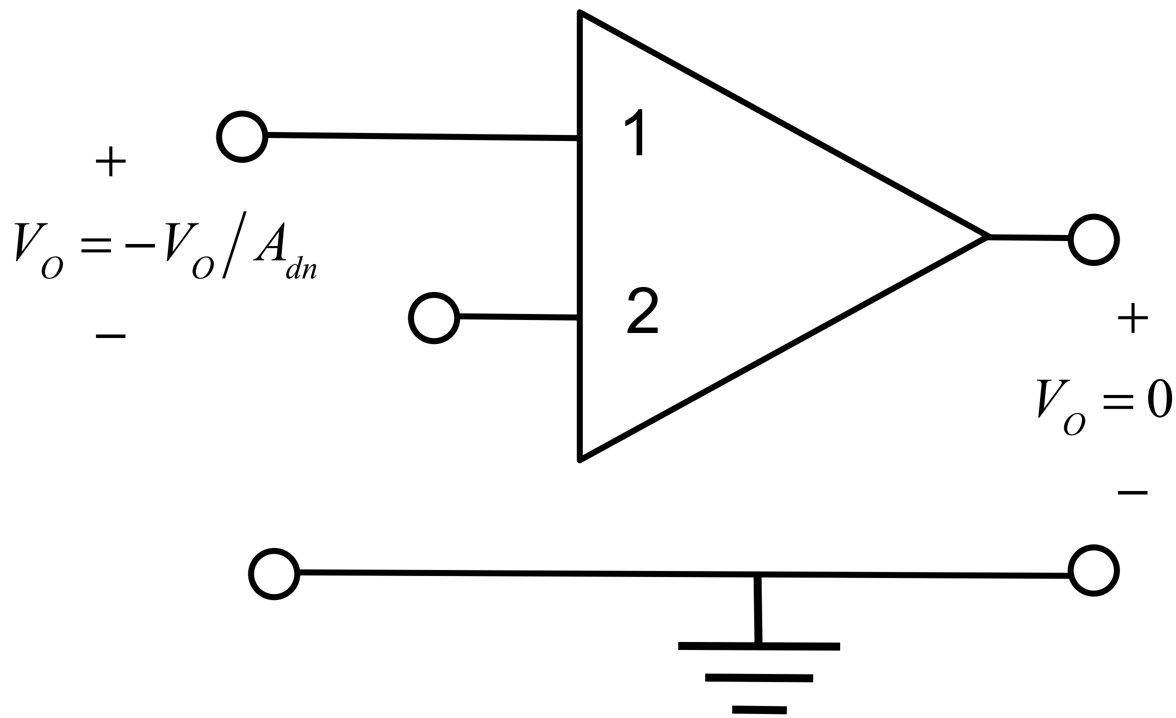


DC coupled – carries signal, plus DC bias

Input offset voltage



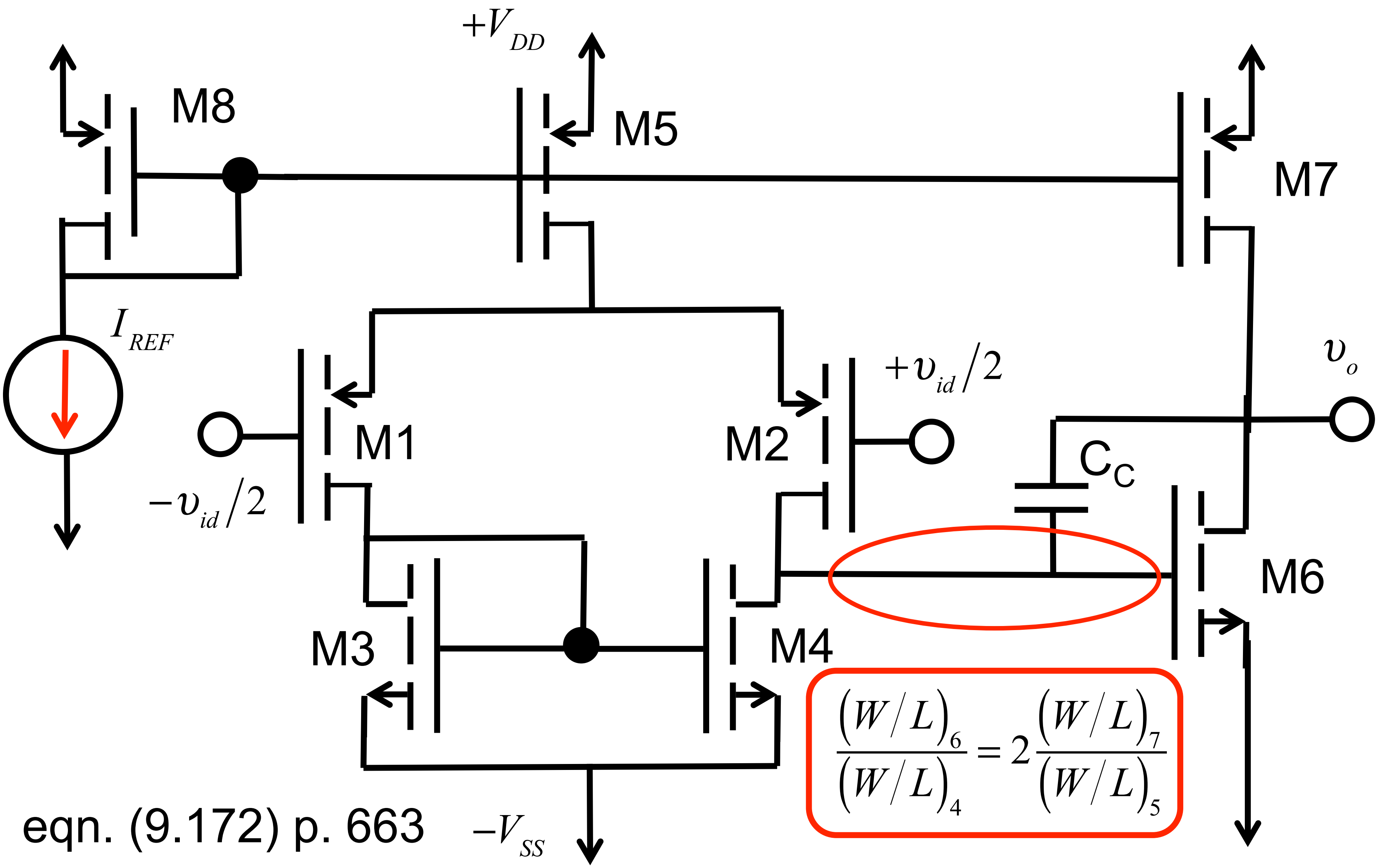
Input offset voltage



"random offset" and "systematic offset"

See Sec. 9.6.1 eqn. (9.172)

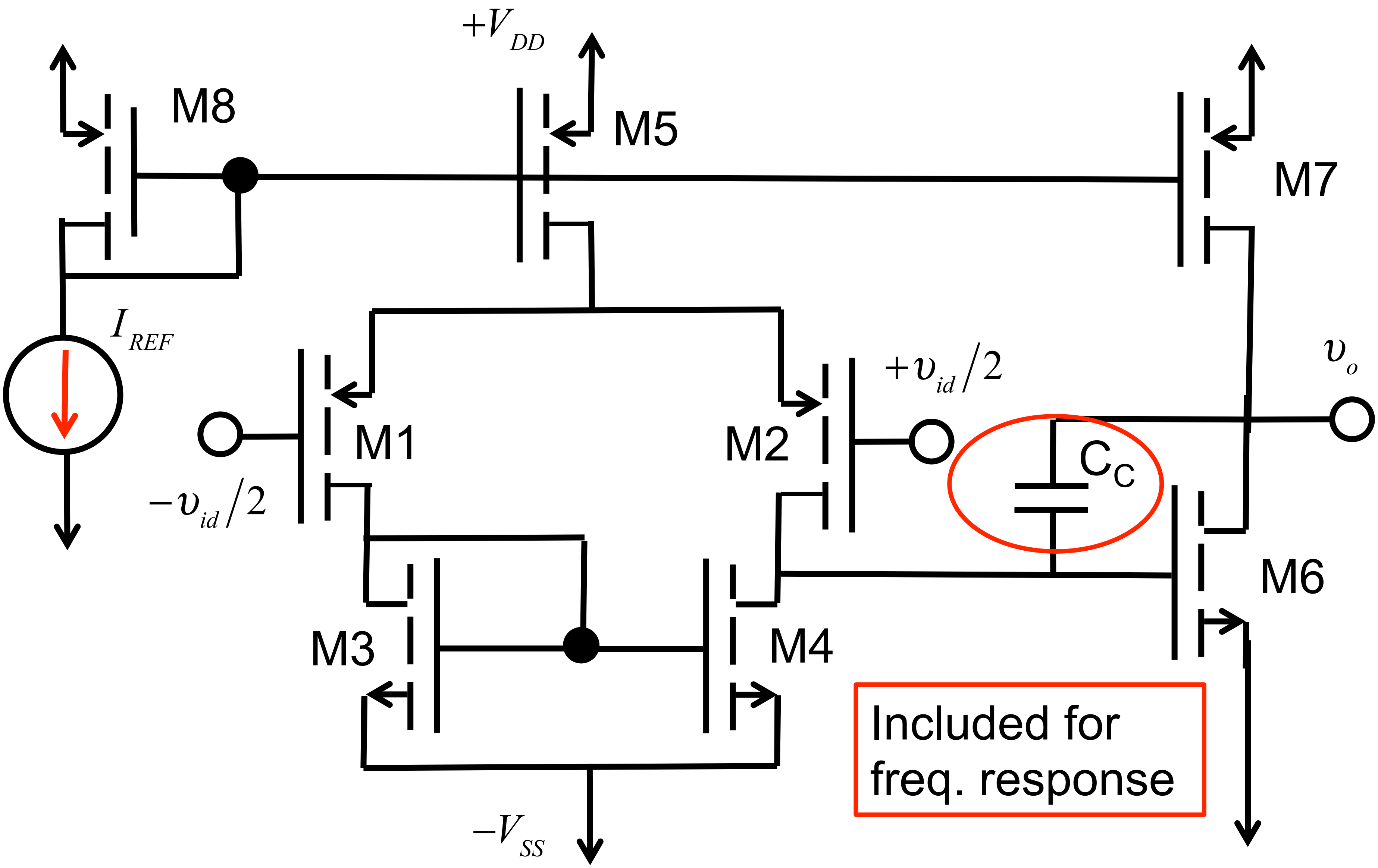
Two-stage CMOS Op Amp: DC coupling



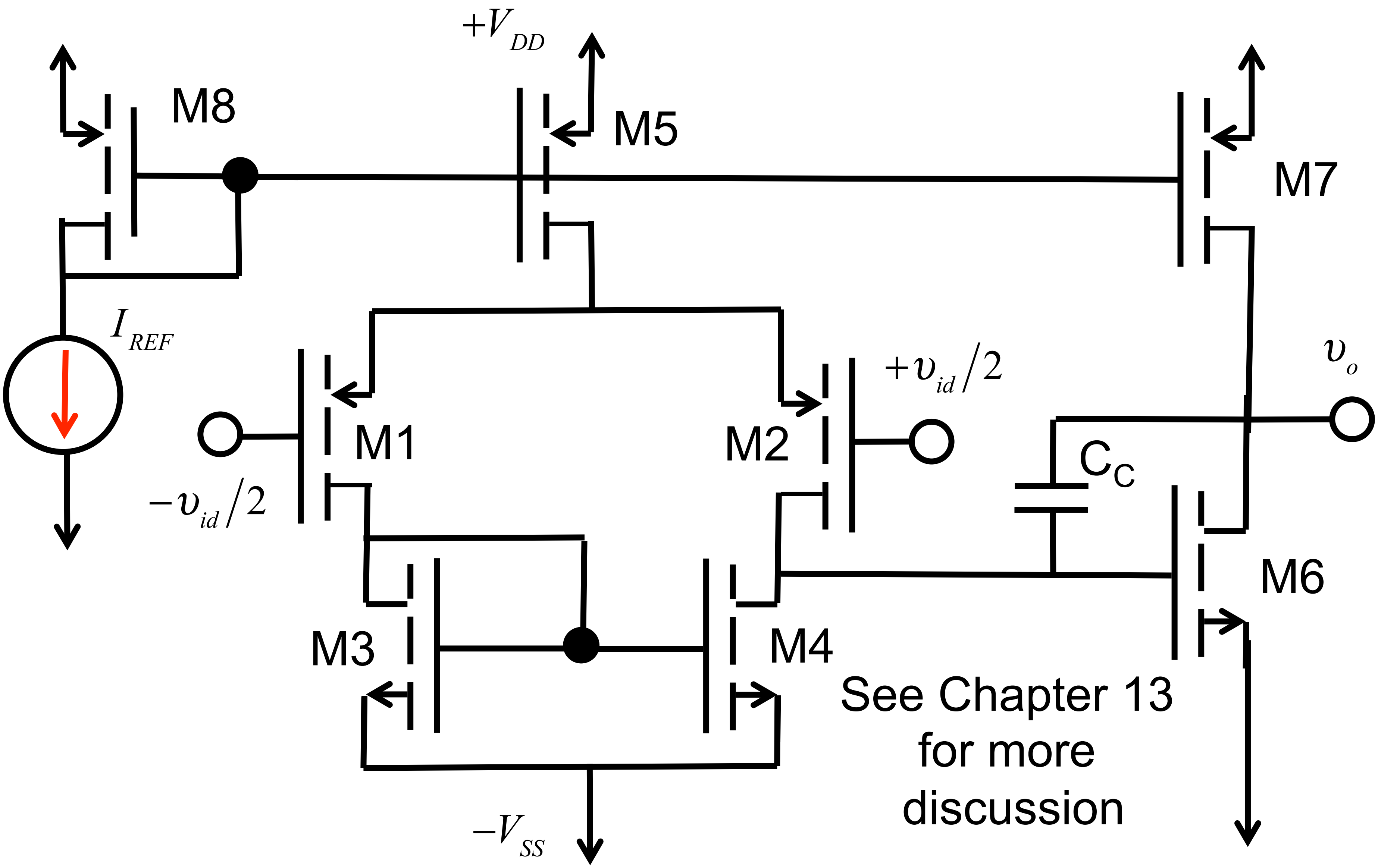
$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$

eqn. (9.172) p. 663

Two-stage CMOS Op Amp: Capacitor



Two-stage CMOS Op Amp: Summary



See Chapter 13 for more discussion

Two-stage CMOS Op Amp

You are encouraged to read through Example 9.6, pp. 661, 662

Two-stage CMOS Op Amp: Summary

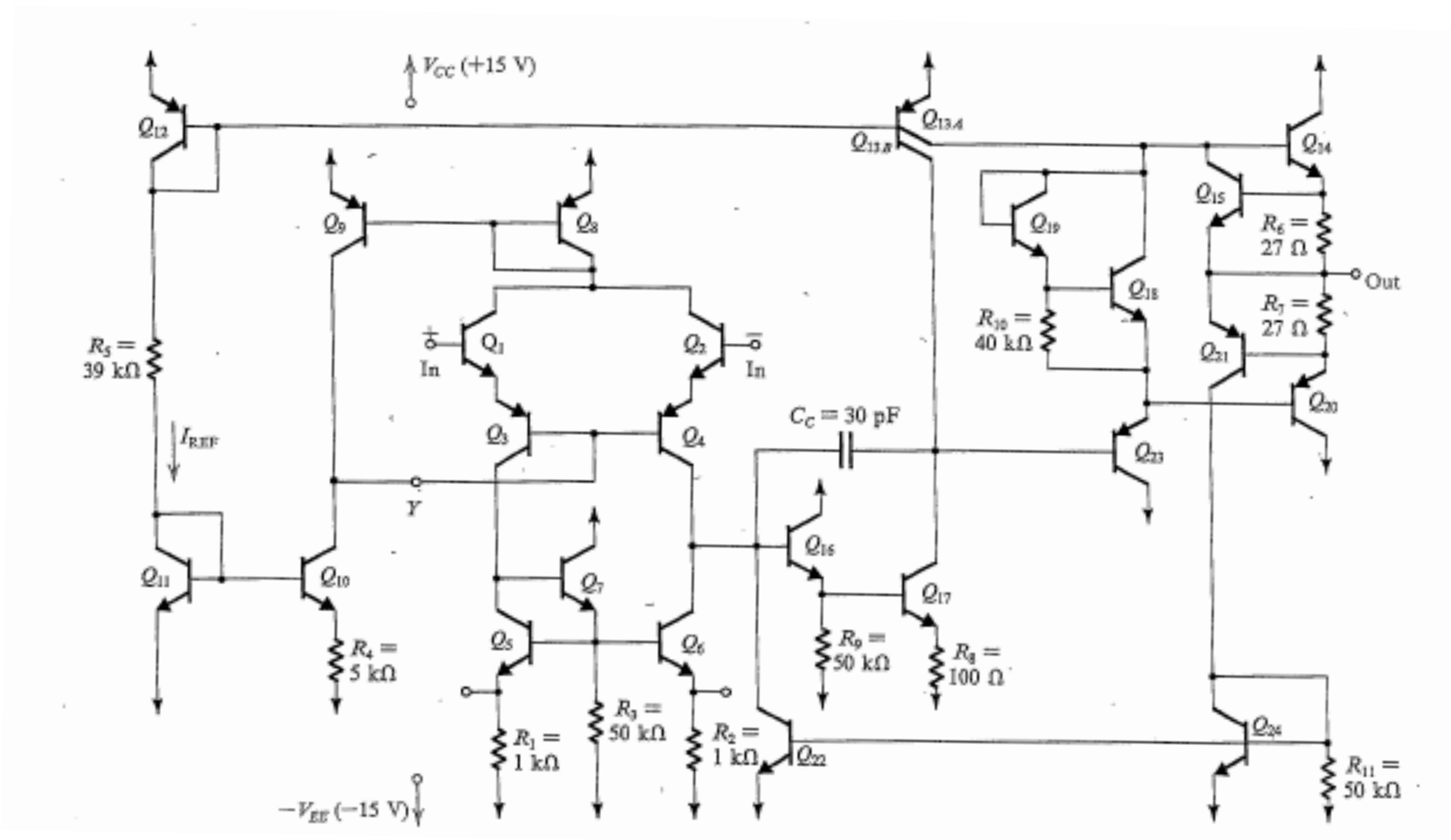
$$A_{dm} = \left(\frac{g_m r_o}{2} \right)^2$$ 1000's but not millions

$$R_{out} = \left(\frac{r_o}{2} \right)$$ relatively large, suitable for driving MOS ckts.

DC coupled − works all the way to DC

General purpose op amp requires more gain and a low output resistance.

741 Op Amp



Sedra and Smith, Section 13.3, 7th Ed.

LTSpice Project 3

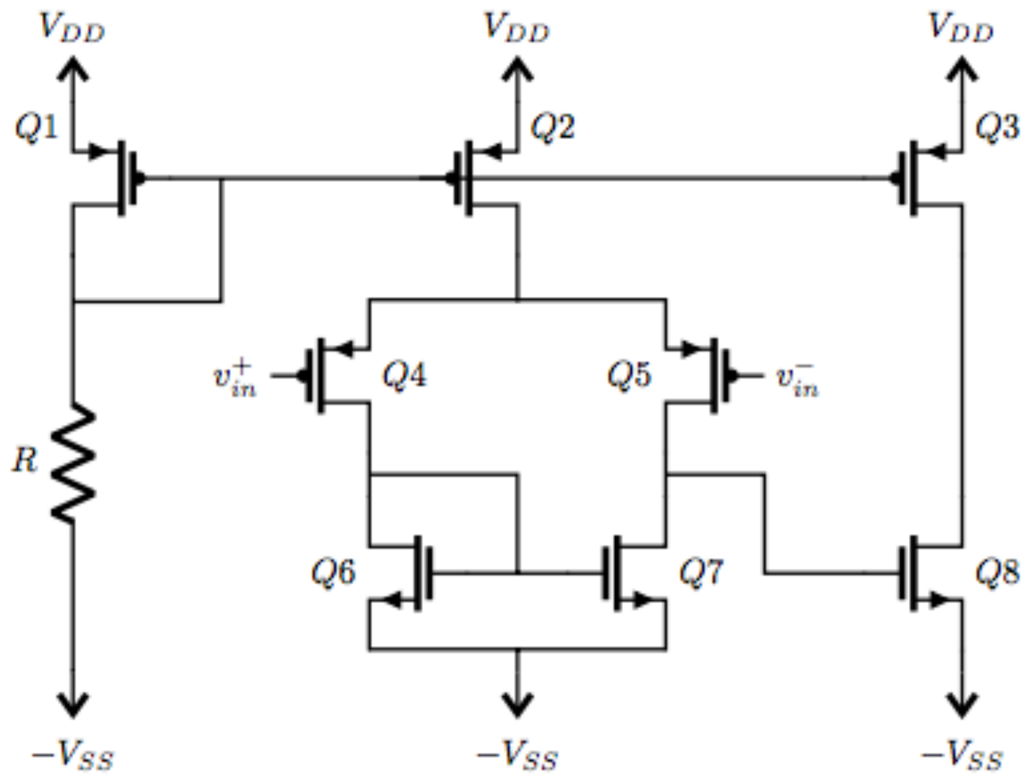


Fig.2 - Two-stage CMOS Amplifier