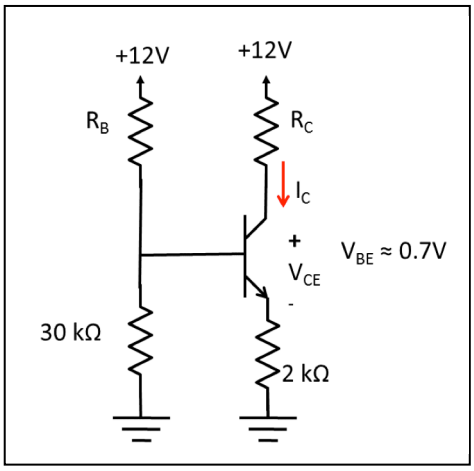
ECE 255 Spring 2019

Homework 5

Due 5:00 PM **Monday**, Feb. 17 in EE-209 Dropbox

1) Consider the BJT bias circuit shown in the figure. Our design goal is $I_C = 1.5$ mA and $V_{CE} = 4$ V.



a) For $\beta = 100$, what values of R_C and R_B do we need in order to achieve the design goal?

b) What are the values of I_B and I_E for the circuit you designed?

c) Suppose the value of β increases to 200. Using the values for R_C and R_B that you found in part a), find I_C, I_B, I_E and V_{CE} for this circuit.

2) Consider a modern MOSFET with a gate length of 10 nm and a gate width of 20 nm. Assume a gate insulator with an equivalent gate oxide thickness of 0.5 nm. (This means some insulator with a relative dielectric constant and thickness equivalent to 0.5 nm of SiO2, which has $\kappa_{ox} = 4$. If the gate voltage is 1.0 V and $V_{tn} = 0.2$ V, how many electrons are there in the channel (i.e. how many electrons on one plate of the capacitor)?

3) Use dimensional analysis to show that the expression for drain current,

$$I_D = \frac{W}{L}\frac{\mu_n C_{ox}}{2}\left(V_{GS} - V_{tn}\right)^2$$

gives the correct units for current.

HW 5 (continued)

4) The table below is for a square law NMOS transistor with $V_{tn} = 1.0$ V. The terminal voltages relative to ground are specified. Identify the region of operation for each case (Cut-off, triode, or saturation). If you encounter a case for which $V_{DS} < 0$, then interchange the source and drain terminals before answering the question. You can do this because MOSFETs are symmetric.

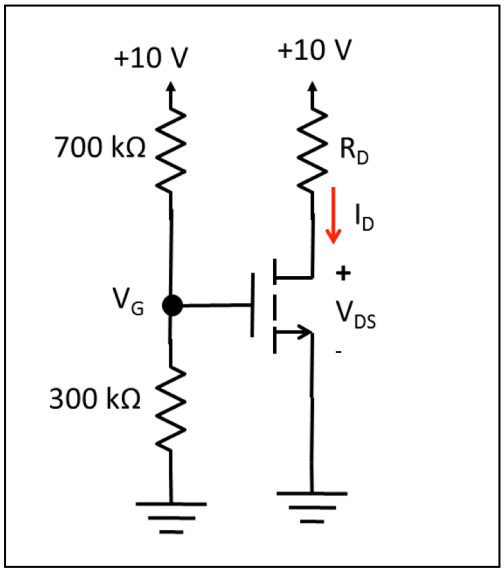
Case	**Source**	**Gate**	**Drain**	**Region?**
1	+1.0	+1.0	+2.0	
2	+1.0	+2.5	+2.0	
3	+1.0	+2.5	+1.25	
4	+1.0	+1.5	0	
5	0	+2.5	+1.0	

5) The table below is for a square law PMOS transistor with $V_{tp} = -1.0$ V. The terminal voltages relative to ground are specified. Identify the region of operation for each case (Cut-off, triode, or saturation). If you encounter a case for which $V_{DS} > 0$, then interchange the source and drain terminals before answering the question. You can do this because MOSFETs are symmetric.

Case	**Source**	**Gate**	**Drain**	**Region?**
1	+2.0	+2.0	0	
2	+2.5	+1.0	0	
3	+2.0	0	0	
4	+2.0	0	+1.0	
5	+2.0	0	+1.5	

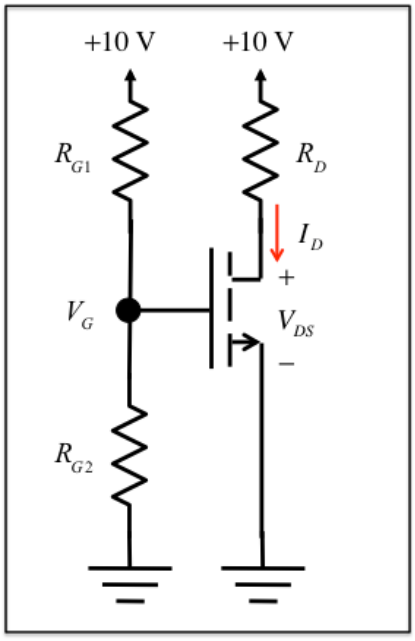
6) An NMOS transistor has a drain current of 0.4 mA at $V_{GS} = V_{DS} = 1$ V and a drain current of 0.1 mA at $V_{GS} = V_{DS} = 0.8$ V. Assuming a square law device, what are the values of k_n and V_{tn} for this transistor?

7) Consider the NMOS circuit shown in the figure to the left. The symbol denotes an enhancement-mode device. Let $V_{tn} = 0.5$ V, $k_n' = 0.1$ mA/V^2, $W_n = 4\ \mu$m, $L_n = 1\ \mu$m and $\lambda = 0$.



a) For $R_D = 4$ kΩ, calculate I_D and V_{DS}.
b) Calculate the value of R_D for which V_{DS} is at the boundary between the triode and saturation regions.
c) Suppose that we increase R_D to 40 kΩ. Find I_D and V_{DS}. Note that you should be able to infer the operating regime by considering your answer to part b).

8) Consider the NMOS circuit shown in the figure to the left. Let $V_{tn} = 0.5$ V, $k_n' = 0.1$ mA/V^2, $W_n = 4\ \mu$m, $L_n = 1\ \mu$m and $\lambda = 0$. Specify the value of the three resistors so that $I_D = 0.2$ mA and $V_{DS} = 2.5$ V.



HW 5 (continued)

9) Consider the enhancement-model PMOS circuit shown in the figure to the left. Let $|V_{tp}| = 1.0$ V, $k_p' = 0.05$ mA/V^2, $W_p = 6\ \mu$m, $L_p = 1\ \mu$m and $\lambda = 0$. Calculate I_D and V_{SD} for $R_D = 5$ kΩ.