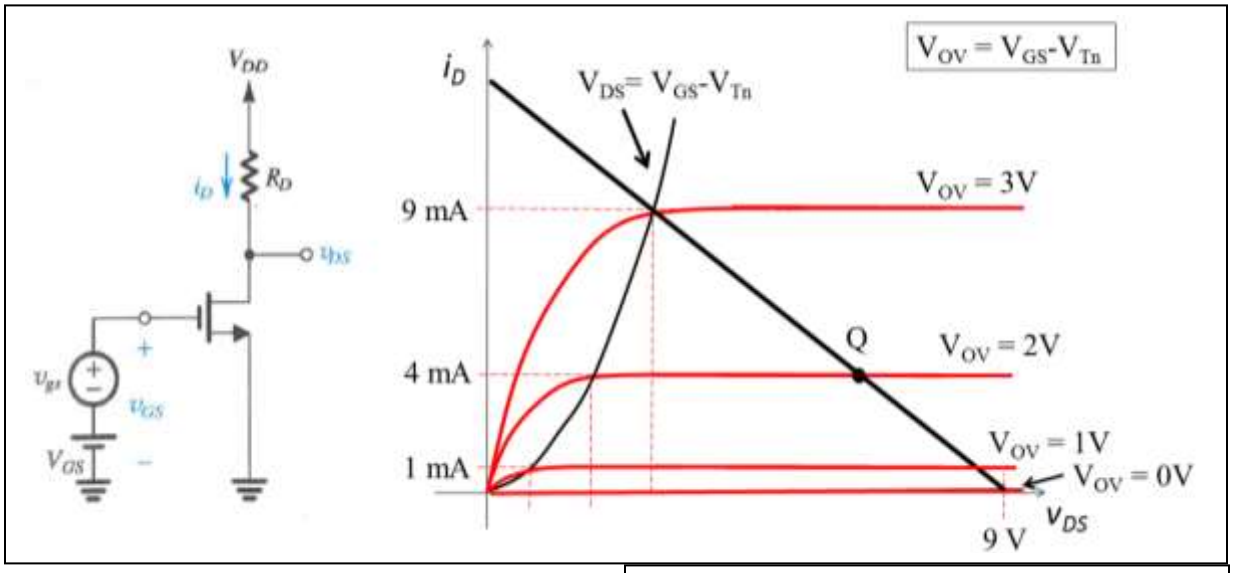
ECE 255 Spring 2019

Homework 6

Due 5:00 PM **Monday**, Feb. 24 in EE-209 Dropbox

Note: Throughout this assignment, the use of upper and lower case characters in symbols for voltages and currents is consistent with the text and lecture convention.

1) Consider the MOSFET circuit shown below. The MOSFET has k_n = 2 mA/V^2, V_{Tn} = 1V, and λ= 0. The I-V characteristics and load line corresponding to R_D = 0.667 kΩ and V_{DD} = 9V are shown. The point marked "Q" corresponds to v_{gs} =0 (the "signal" component).

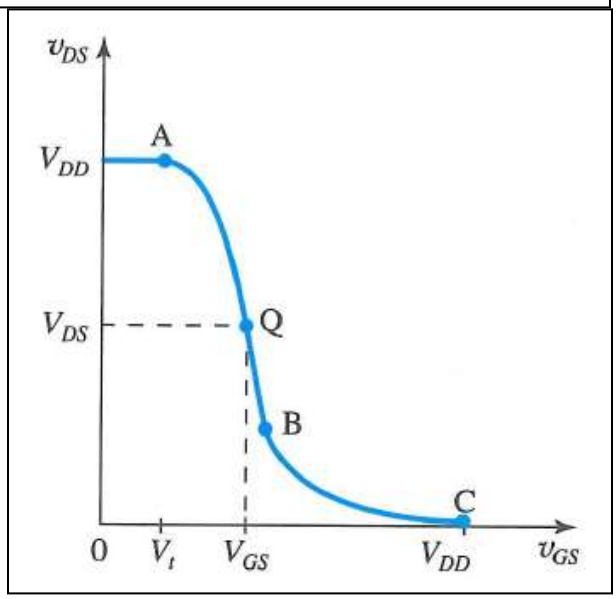


a) Find the gate and drain voltages (V_{GS} and V_{DS}) at the "Q" point.

b) Calculate the change in value of v_{DS} for v_{gs} = +0.1V.

c) What is the voltage gain ($\Delta v_{DS}/\Delta v_{GS}$) for this circuit?

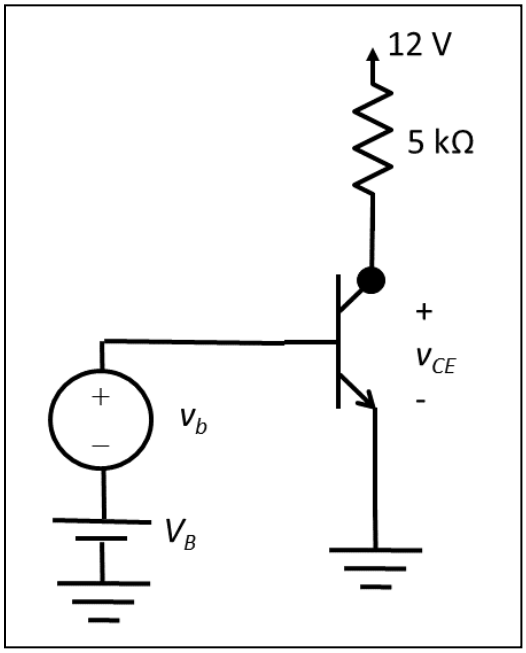
d) Consider the transfer curve shown to the right. What are the values of v_{GS} corresponding to points A and B?



e) Suppose that we apply appropriate V_{GS} to bias the circuit at the Q point from part a), then apply $v_{gs} = v_{sig} \cos(\omega t)$. What is the maximum value of v_{sig} for which the circuit will remain in the "high gain" region (i.e. between points A and B on transfer curve?

2) Consider a NPN BJT with $\beta = 80$ and $V_A = 40V$. The transistor is biased at $I_C = 1$ mA and operates at room temperature in the (forward) active region at $V_{CE} = 2.5V$. For parts a)-d), you should consider the hybrid π model.
   a) Find the value of r_π.
   b) Find the value of g_m.
   c) Find the value of r_o.
   d) Find the value of r_e (for the T-model)

3) Consider the BJT circuit shown in the figure below. The transistor has $\beta = 100$. The value of V_B is adjusted such that $I_B = 0.02$ mA and $V_{BE} \sim 0.7V$. For parts a)-d), $V_A = 0$.

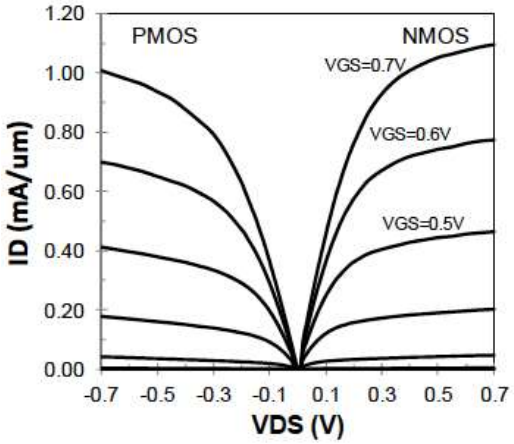


   a) Find I_C and V_{CE}.
   b) What are the values of r_π and g_m?
   c) Draw a small-signal equivalent circuit for the amplifier, showing v_b and v_{ce}.
   d) Find the voltage gain, v_{ce}/v_b.
   e) For this part, assume that $V_A = 30$ V. Find the value of r_o and the voltage gain. You should assume that I_C and V_{CE} are unchanged.

4) The *IV* characteristics of an N- and P-MOSFET for the 14 nm technology node are shown on the next page. Note that the NMOS characteristics are shown in the $V_{DS} > 0$ region and PMOS characteristics in the $V_{DS} < 0$ region (with same magnitudes, but negative values, for V_{GS}). The current is normalized by device width, so your result will be expressed in "per micron." Reading from the graphs as carefully as you can, estimate the average transconductance, g_m, for the two cases below:

   a) For the N-MOSFET at $V_{DS} = 0.7$ V and for V_{GS} between 0.6 and 0.7 V.
   b) The corresponding transconductance for the P-MOSFET.

   HINT: Note that this is not a square law MOSFET.



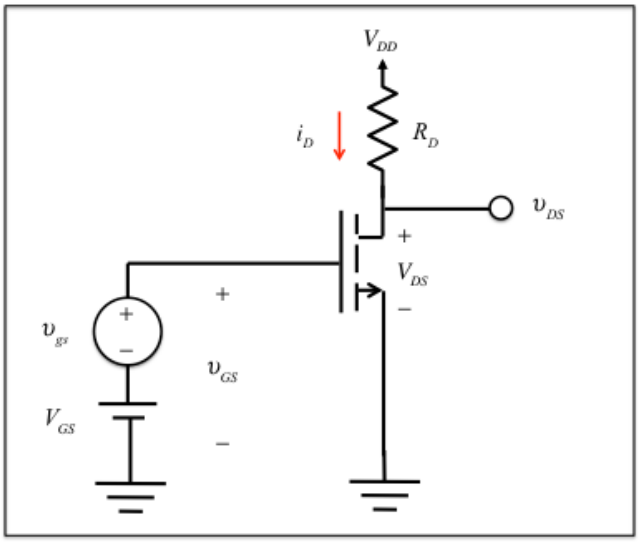
From: S. Natarajan, et al., "A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 um2 SRAM cell size," pp. 70-72. Tech. Digest, Intern. Electron Dev. Mtg, Dec. 2014.

5) An enhancement-mode PMOS transistor operating in saturation has $\mu_p C_{ox} = 250\ \mu\text{A/V}^2$ and $V_{tp} = -0.5\ \text{V}$. The channel length is $L = 0.5\ \mu\text{m}$

   a) Find the value of W that produces $g_m = 2\ \text{mA/V}^2$ at $I_D = 0.5\ \text{mA}$.

   b) Find the value of V_{SG} corresponding to this bias point.

6) Consider the MOSFET amplifier shown in the figure at the right. Assume a transistor with $k_n = 5\ \text{mA/V}^2$ and $V_{tn} = 0.4\ \text{V}$. Also assume that $V_{GS} = 0.6\ \text{V}$, $V_{DD} = 1.8\ \text{V}$, and $R_D = 10\ \text{k}\Omega$. Answer the following questions.



   a) Compute I_D and V_{DS}

   b) Calculate g_m

   c) Calculate the voltage gain (v_{ds}/v_{gs})

   d) If $\lambda = 0.1\ \text{V}^{-1}$, find r_o and the voltage gain.

7) Consider the amplifier shown below. All of the capacitors are large – you may assume that they are short circuits to the ac signals and open circuits for dc. The transistor has $k_n = 4$ mA/V^2, $V_{tn} = 1$ V and $V_A = 100$ V. Also assume that $V_{DD} = 1.8$ V, and $R_D = 10$ kW. Answer the following questions.

a) Show that $V_{GS} = 1.5$ V, $I_D = 0.5$ mA and that $V_D = 7.0$ V

b) Find g_m and r_o

c) Draw the complete small signal equivalent circuit assuming that all capacitors are short circuits at the signal frequency.

d) Find R_{in}. u_{gs}/u_{sig}, u_o/u_{gs}, and u_o/u_{sig}