ECE-305: Spring 2018
Semiconductor Fabrication

Pierret, *Semiconductor Device Fundamentals* (SDF)
Chapter 4 (pp. 139-194)

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current challenges in device fabrication

Smaller, Faster, Cheaper, Over: The Future of Computer Chips

By JOHN MARKOFF SEPT. 26, 2015

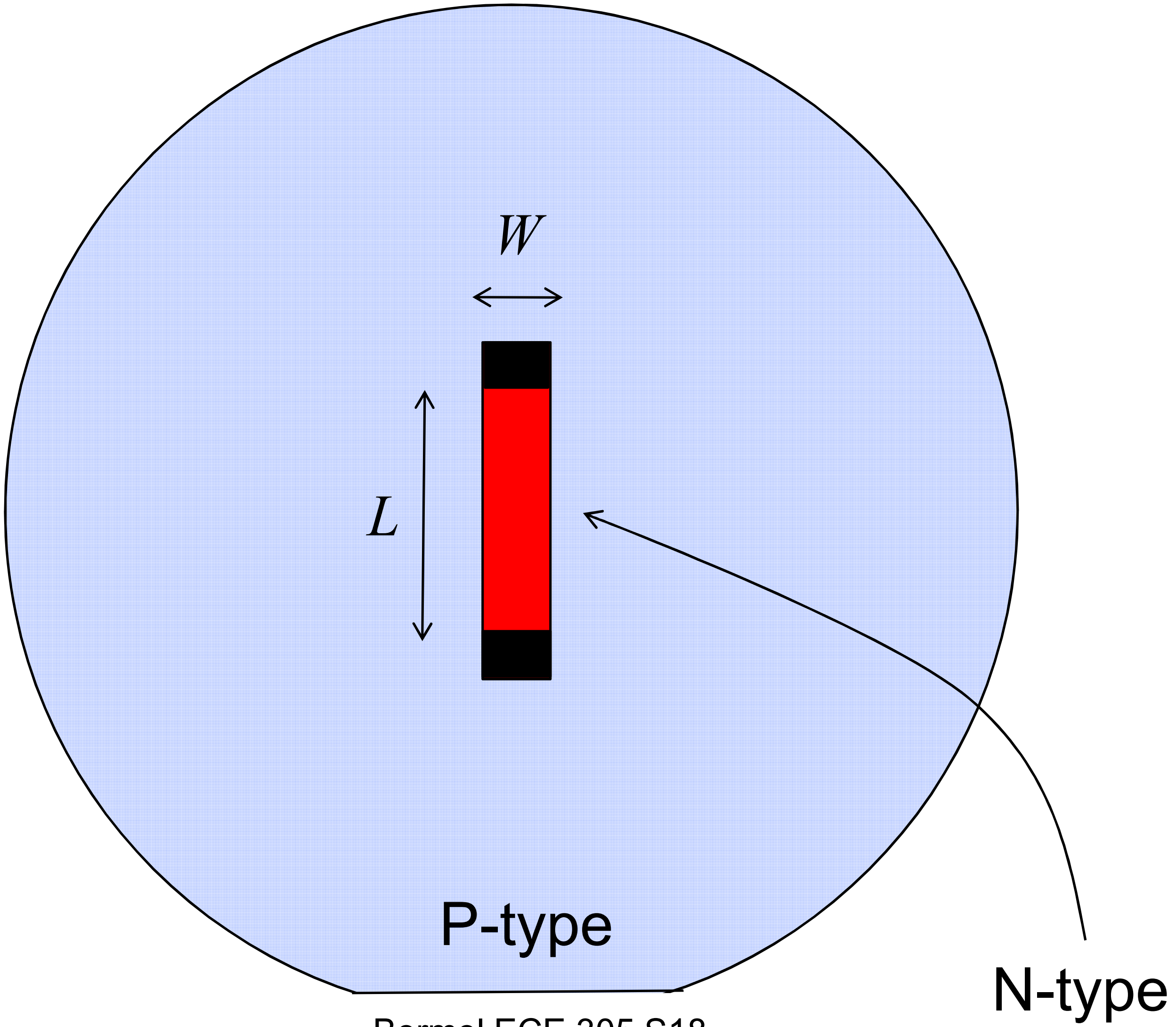
Max Shulaker, a graduate student at Stanford, working in 2011 on a new kind of semiconductor circuit. As chips continue to shrink, computer scientists are seeking new technological breakthroughs

http://www.nytimes.com/2015/09/27/technology/smaller-faster-cheaper-over-the-future-of-computer-chips.html?ref=technology&_r=0

integrated circuit resistors

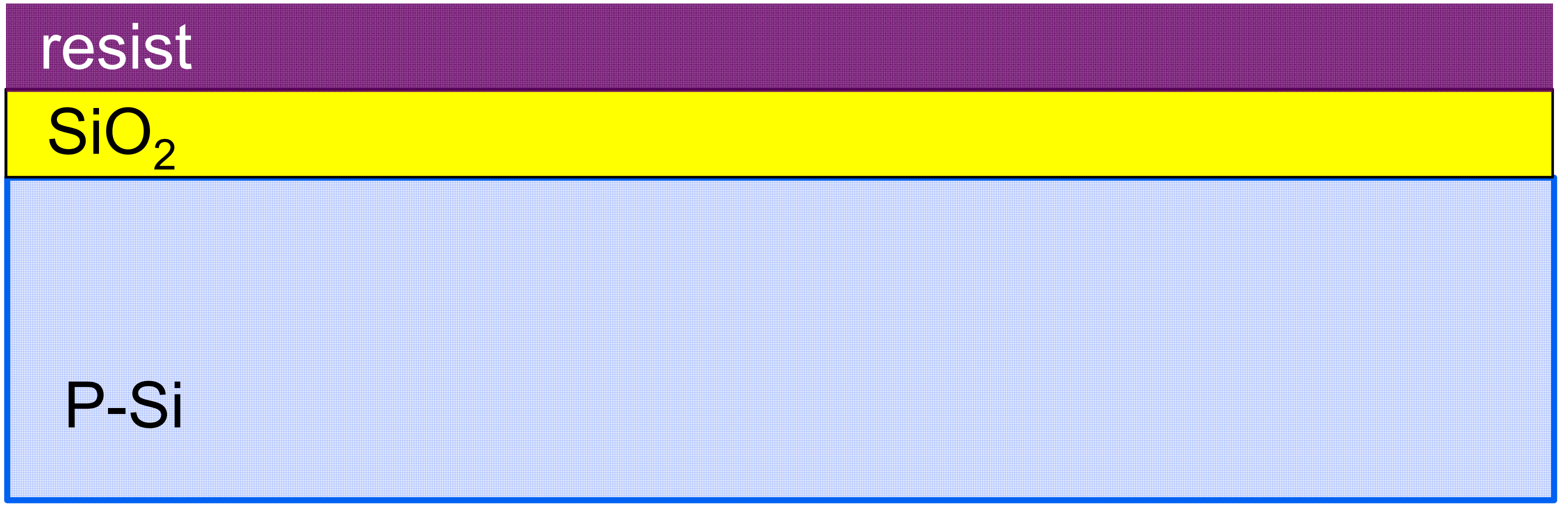
$$R = \rho_S \left(\frac{L}{W} \right)$$

$$\rho_S \; \left(\Omega / \square \right)$$



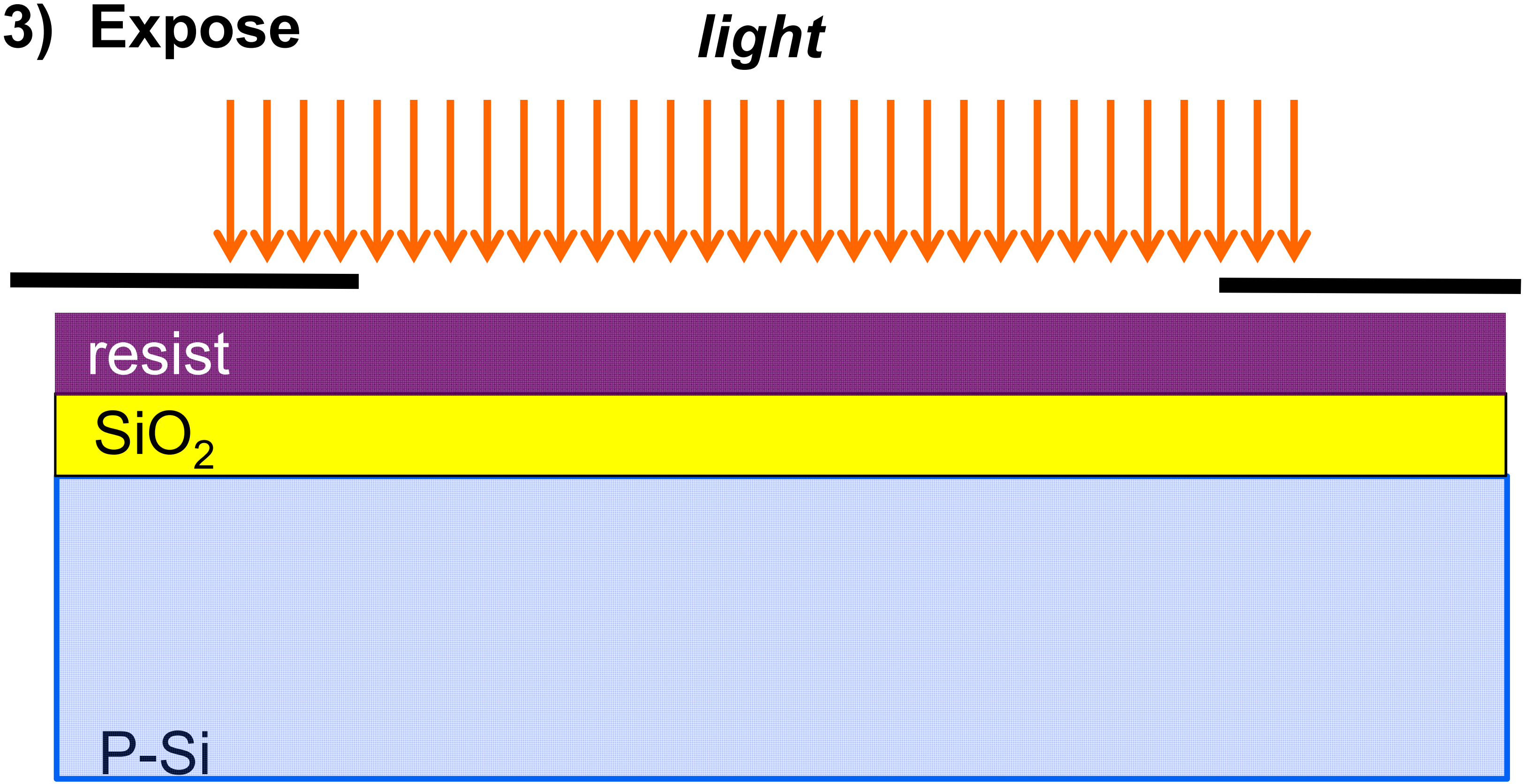
Integrated circuit resistors

1) Oxidize
2) Coat with resist



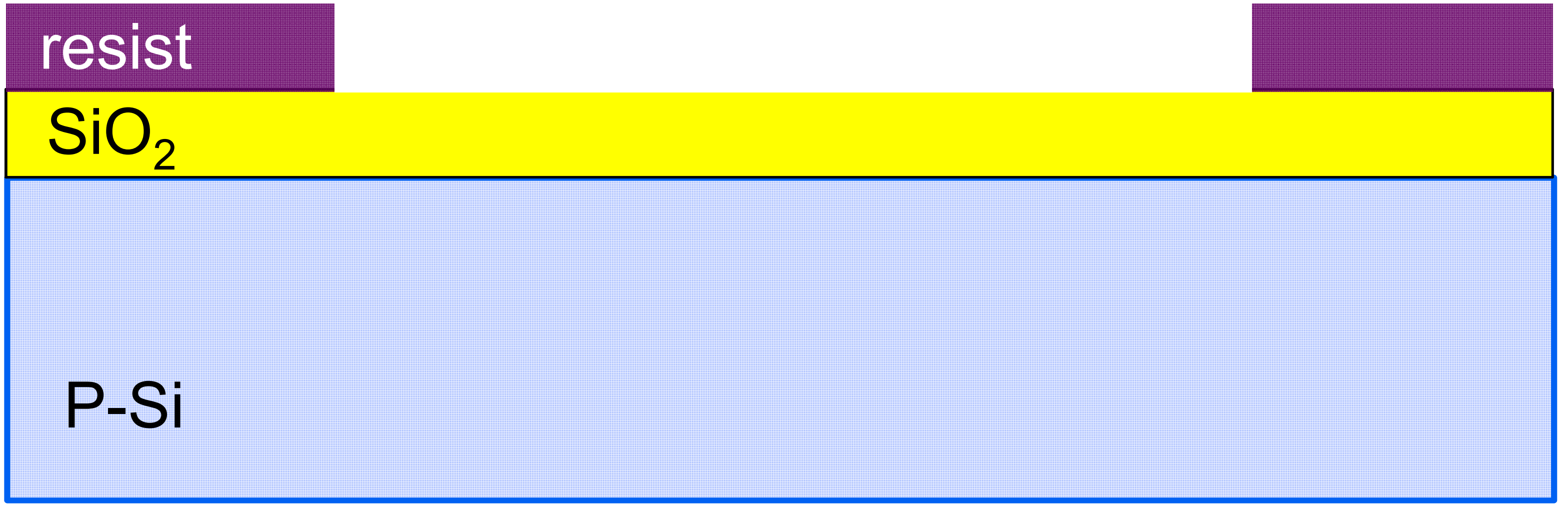
Integrated circuit resistors

1) Oxidize
2) Coat with resist
3) **Expose**



Integrated circuit resistors

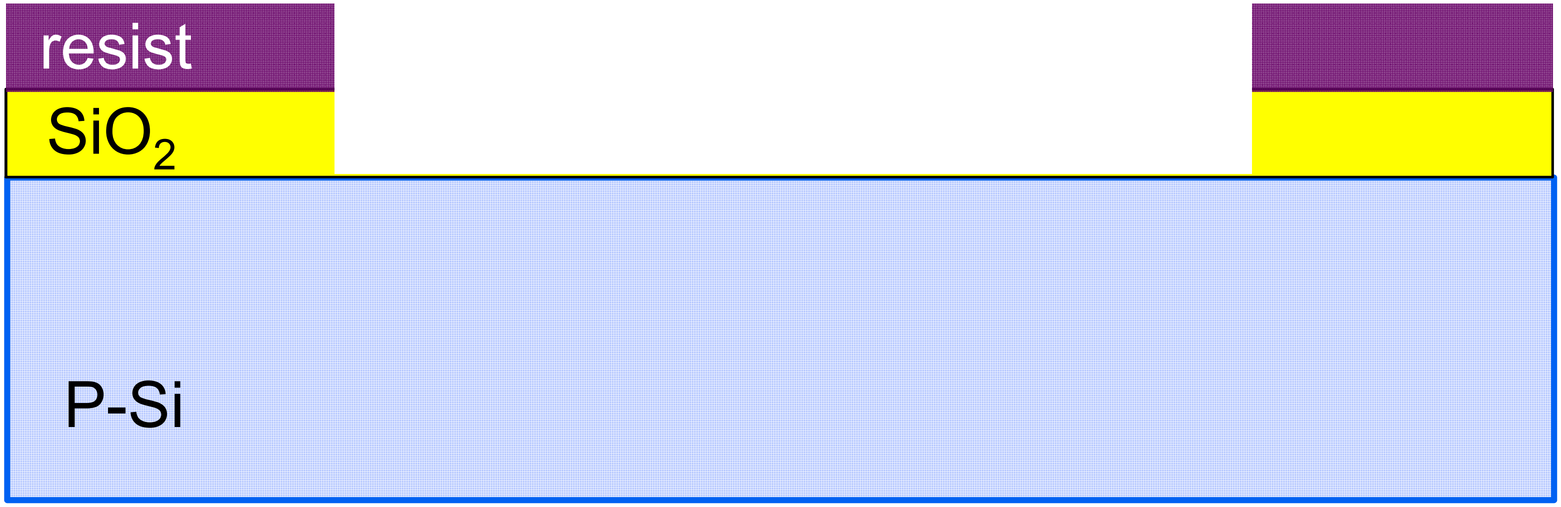
1) Oxidize
2) Coat with resist
3) Expose
4) **Develop**



Integrated circuit resistors

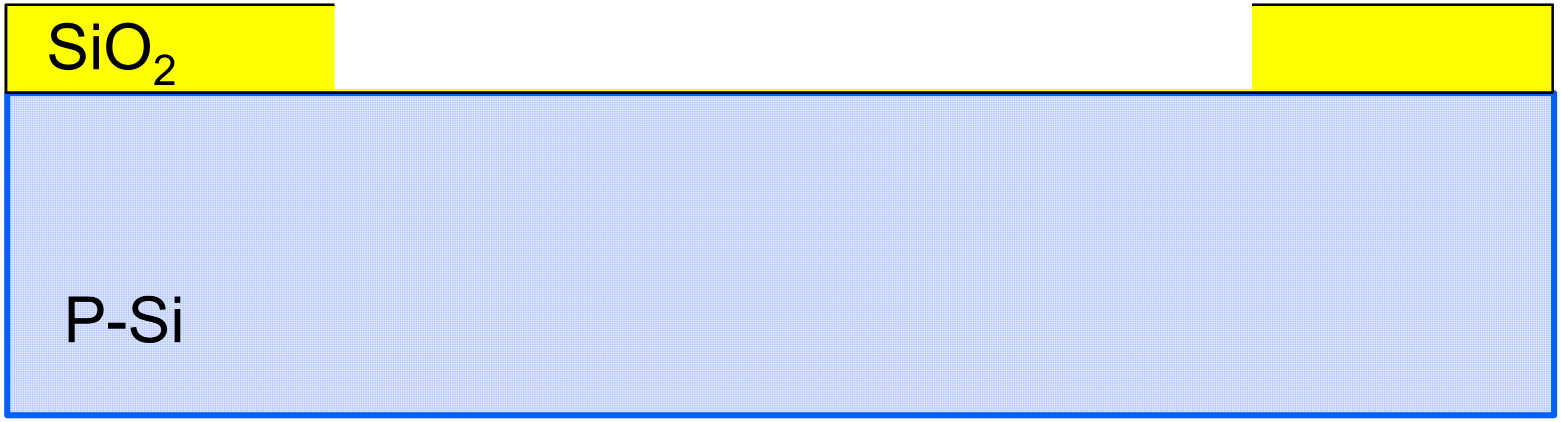
1) Oxidize
2) Coat with resist
3) Expose
4) Develop

5) Etch



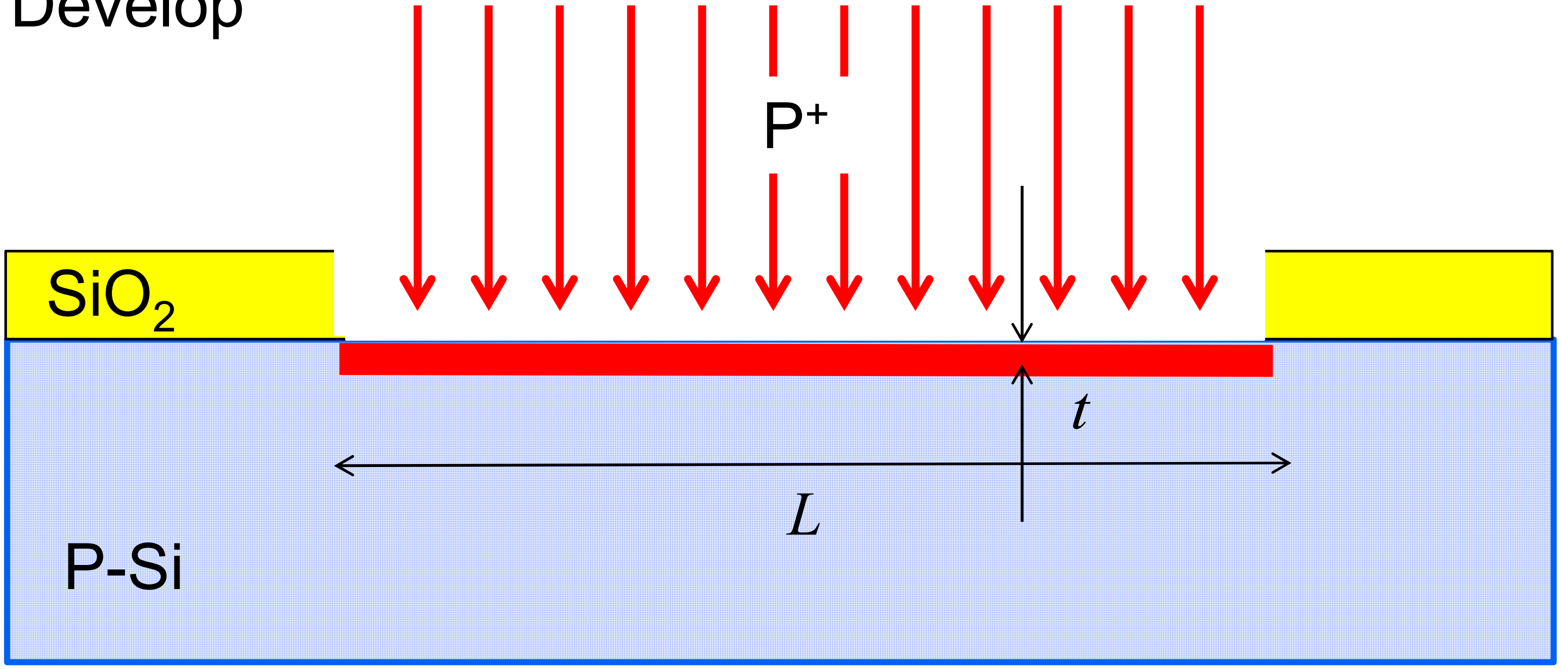
Integrated circuit resistors

1) Oxidize
2) Coat with resist
3) Expose
4) Develop
5) Etch
6) **Strip resist**



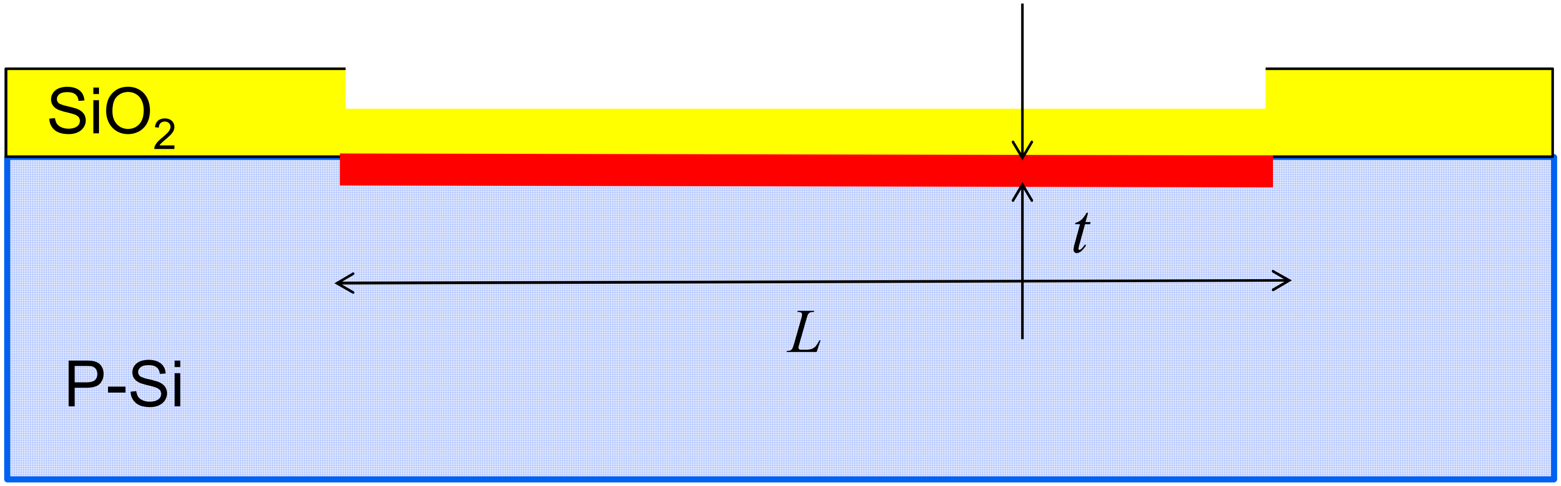
Integrated circuit resistors

1) Oxidize
2) Coat with resist
3) Expose
4) Develop
5) Etch
6) Strip resist
7) **Dope**



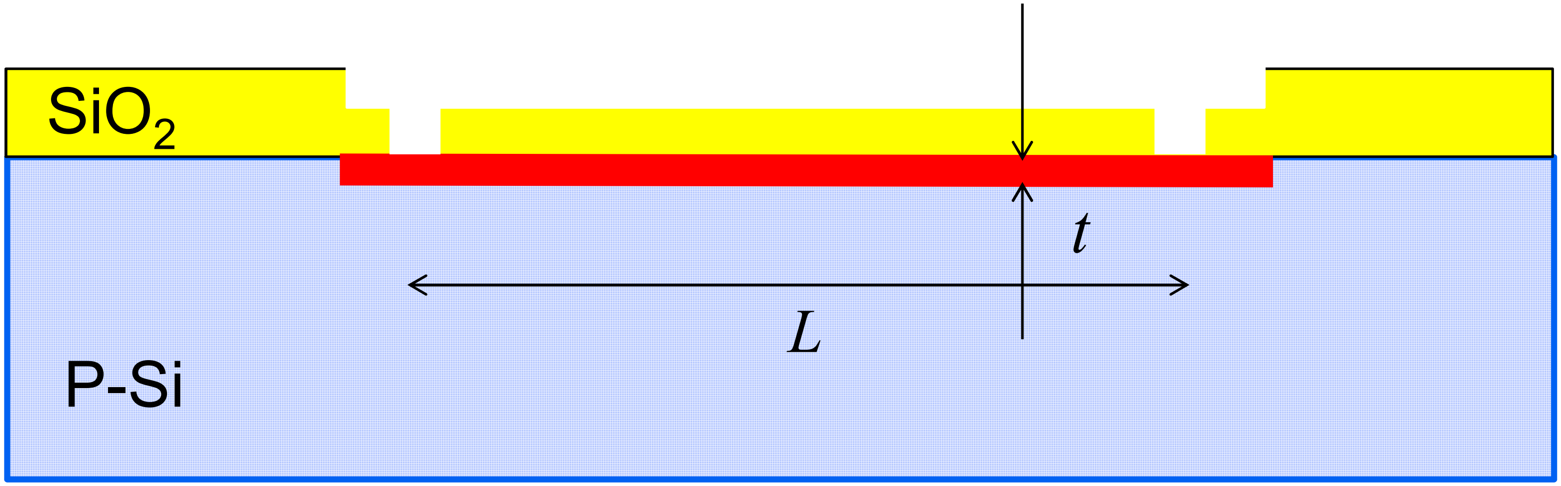
Integrated circuit resistors

1) Oxidize
2) Coat with resist
3) Expose
4) Develop
5) Etch
6) Strip resist
7) Dope
8) **Anneal and Oxidize**



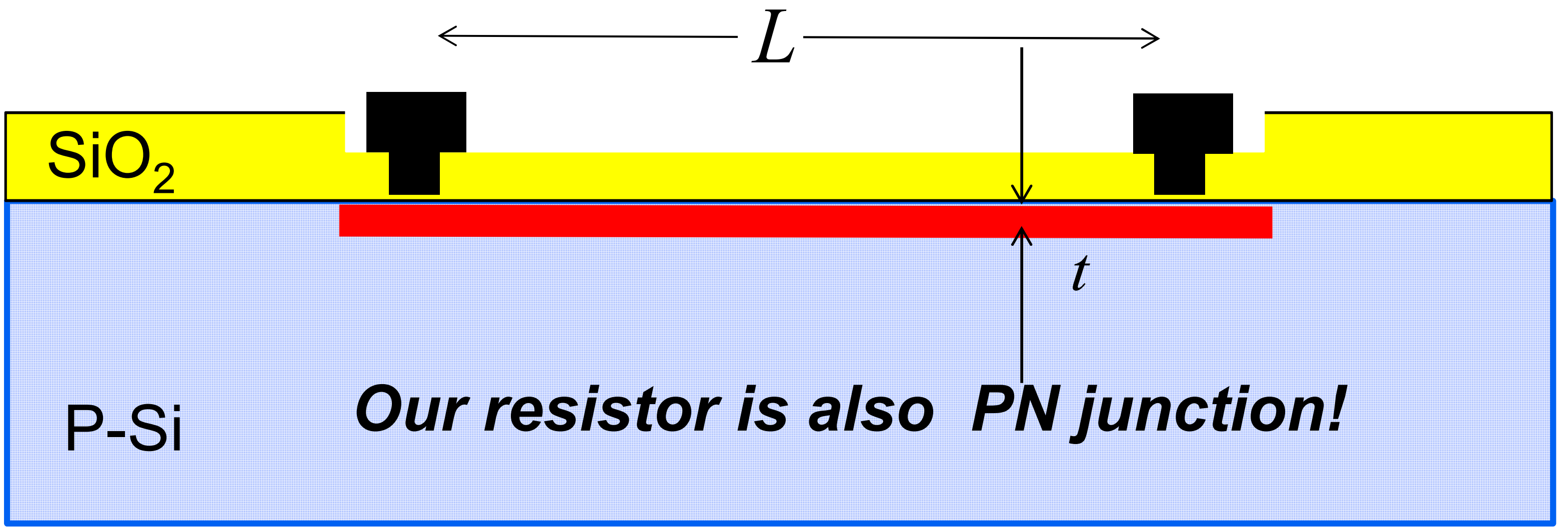
Integrated circuit resistors

1) Oxidize
2) Coat with resist
3) Expose
4) Develop
5) Etch
6) Strip resist
7) Dope
8) Anneal/Oxidize
9) Open contacts



Integrated circuit resistors

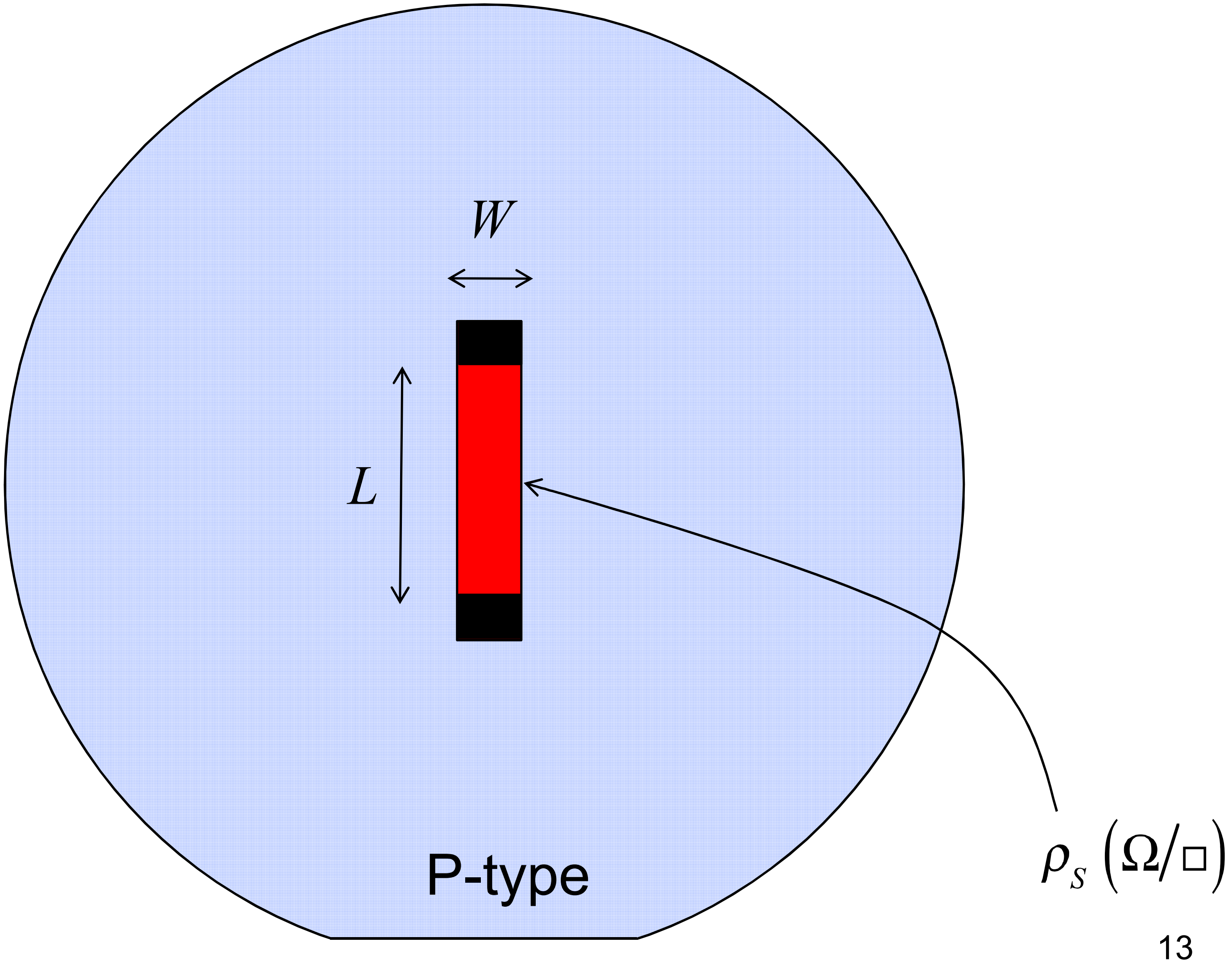
1) Oxidize
2) Coat with resist
3) Expose
4) Develop
5) Etch
6) Strip resist
7) Dope
8) Anneal/Oxidize
9) Open contacts
10) Deposit metal pattern, etch



Our resistor is also PN junction!

integrated circuit resistors

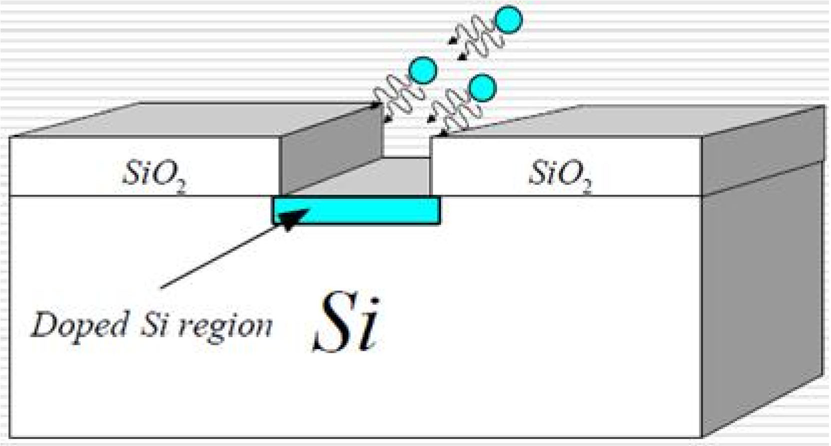
$$R = \rho_S\left(\frac{L}{W}\right)$$



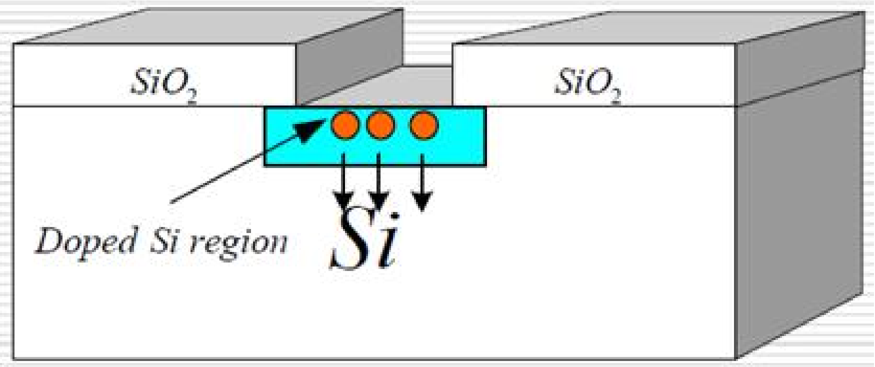
videos

- GLOBALFOUNDRIES Sand to Silicon
- Semiconductor Technology at TSMC, 2011
- Intel: The Making of a Chip with 22nm/3D Transistors

Diffusion from a gas, liquid or solid source



Pre-deposition (dose control)



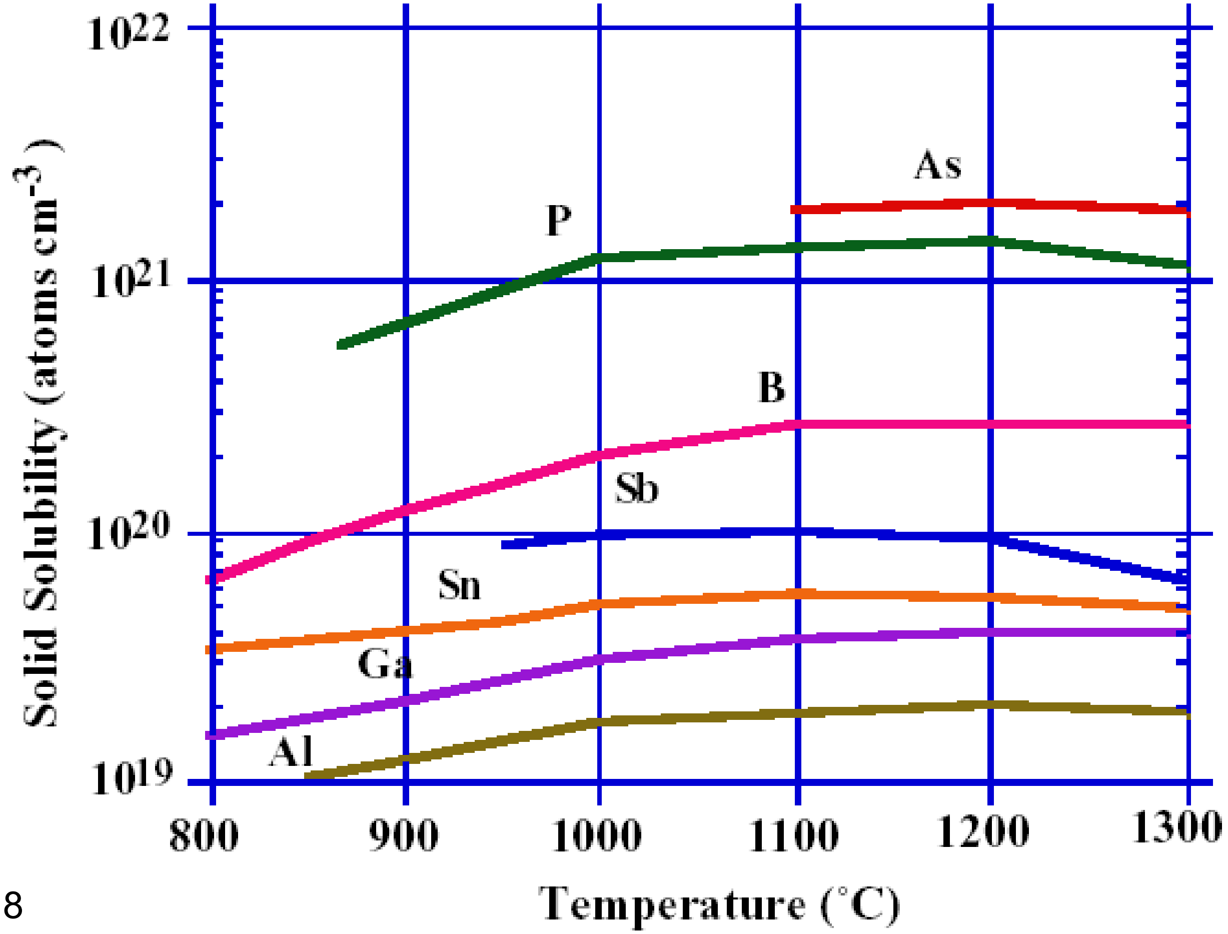
Drive-in (profile control)

- Silicon dioxide masks impurity diffusion in Si
- The mixture of dopant species, oxygen and inert gases pass over wafers at 900-1100^{o}C in a diffusion furnace
- The dopant concentration reaches the solid solubility limit
- The impurities can be introduced into the carrier gas from solid (evaporated), liquid (vapor) or gas source.

Adapted from Bo Cui, ECE, University of Waterloo; and *Silicon VLSI Technology* by Plummer, Deal and Griffin

Dopant solid solubility limits

Solid solubility limit: maximum concentration for an impurity before precipitation into a separate phase.



Adapted from Bo Cui, ECE, University of Waterloo; and *Silicon VLSI Technology* by Plummer, Deal and Griffin

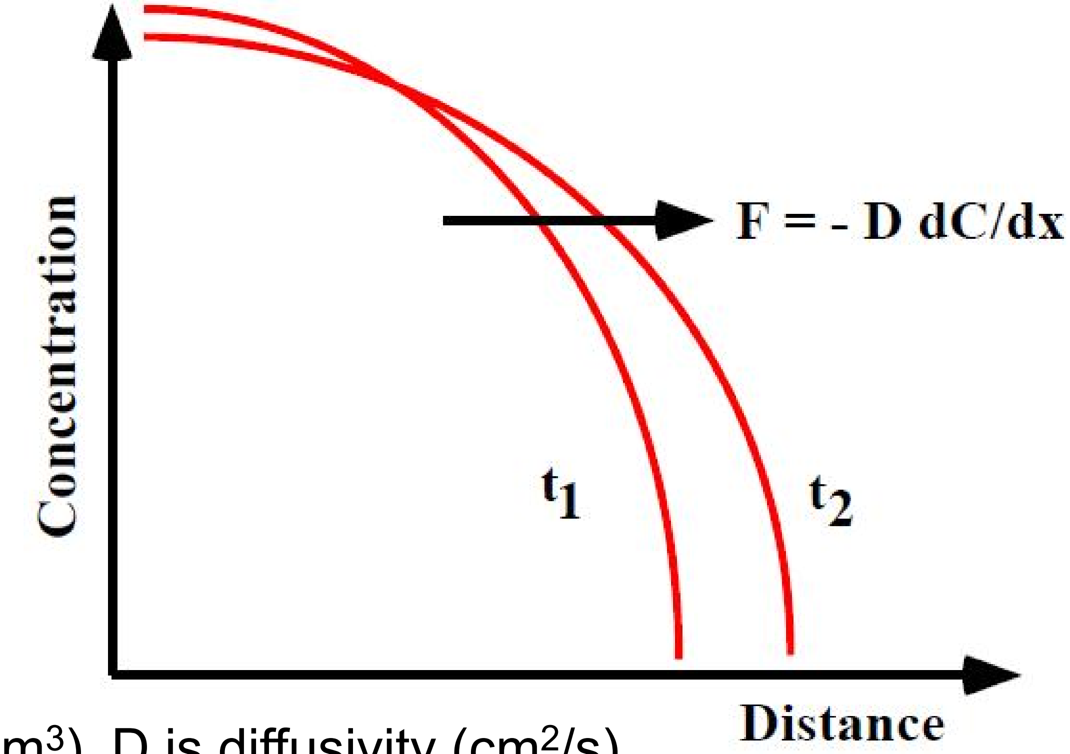
Diffusion from a macroscopic viewpoint

Fick's first law of diffusion

F is net flux.

$$F(x,t) = -D\frac{\partial C(x,t)}{\partial x}$$

Cf. Ohm's law



C is impurity concentration (#/cm^3), D is diffusivity (cm^2/s).

D is related to atomic hops over an energy barrier (formation and migration of mobile species) and is exponentially activated.

Negative sign indicates that the flow is down the concentration gradient.

Adapted from Bo Cui, ECE, University of Waterloo; and *Silicon VLSI Technology* by Plummer, Deal and Griffin

Intrinsic diffusivity D_i

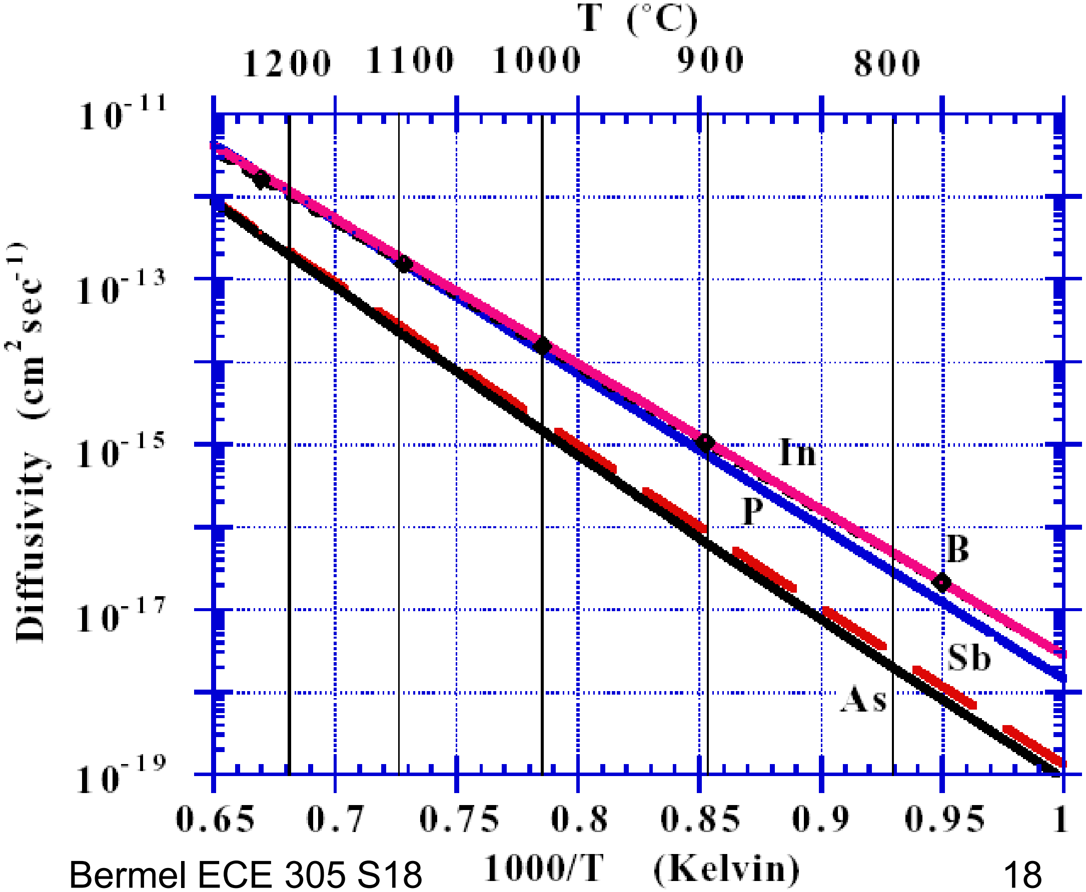
Intrinsic: impurity concentration N_A, $N_D < n_i$

Note that n_i is quite high at typical diffusion temperatures

$$D_i = D^0 \exp(-\frac{E_a}{kT})$$

E_a: activation energy

	D^0(cm²/s)	E_a(eV)
B	1.0	3.46
In	1.2	3.50
P	4.70	3.68
As	9.17	3.99
Sb	4.58	3.88



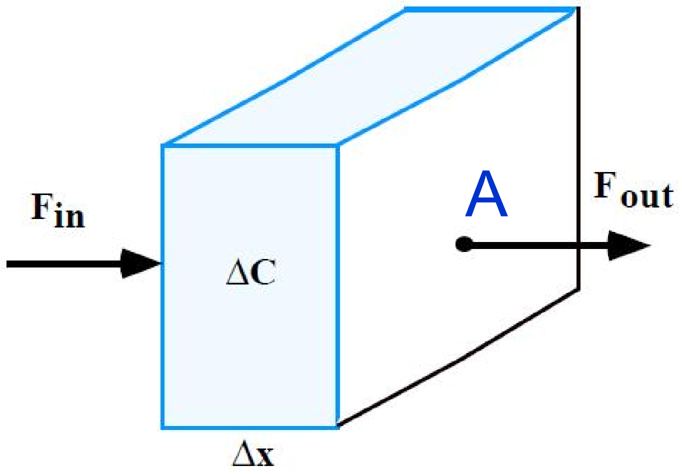
Adapted from Bo Cui, ECE, University of Waterloo; and *Silicon VLSI Technology* by Plummer, Deal and Griffin

Fick’s second law

Since:

$$\frac{\partial C(x,t)}{\partial t} = -\frac{\partial F(x,t)}{\partial x}$$

$$F(x,t) = -D\frac{\partial C(x,t)}{\partial x}$$



We have:

$$\frac{\partial C(x,t)}{\partial t} = -\frac{\partial F(x,t)}{\partial x} = \frac{\partial}{\partial x}\left[D\frac{\partial C(x,t)}{\partial x}\right]$$

If D is constant:

$$\boxed{\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2}}$$

Adapted from Bo Cui, ECE, University of Waterloo; and *Silicon VLSI Technology* by Plummer, Deal and Griffin

Solution to diffusion equation

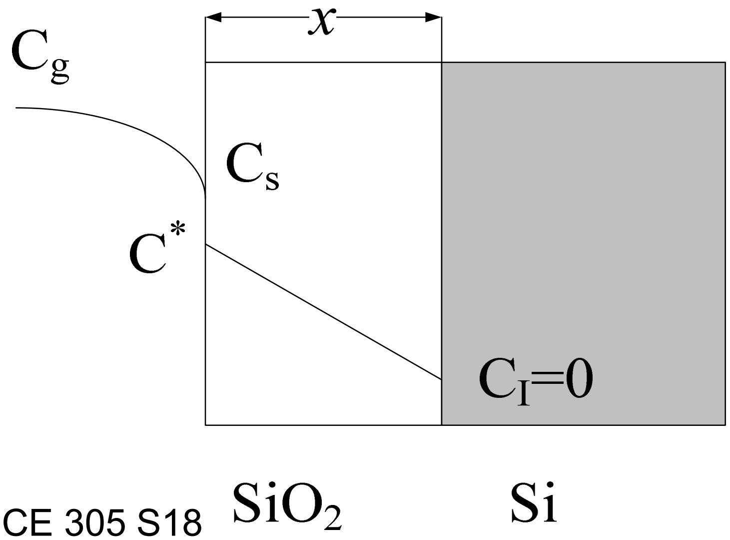
$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2}$$

In equilibrium, C doesn't change with time.

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} = 0$$

$$C = a + bx$$

Diffusion of oxidant (O_2 or H_2O) through SiO_2 during thermal oxidation.



Adapted from Bo Cui, ECE, University of Waterloo; and *Silicon VLSI Technology* by Plummer, Deal and Griffin

for more on IC manufacturing

ECE 612 Purdue University:

https://nanohub.org/resources/5788

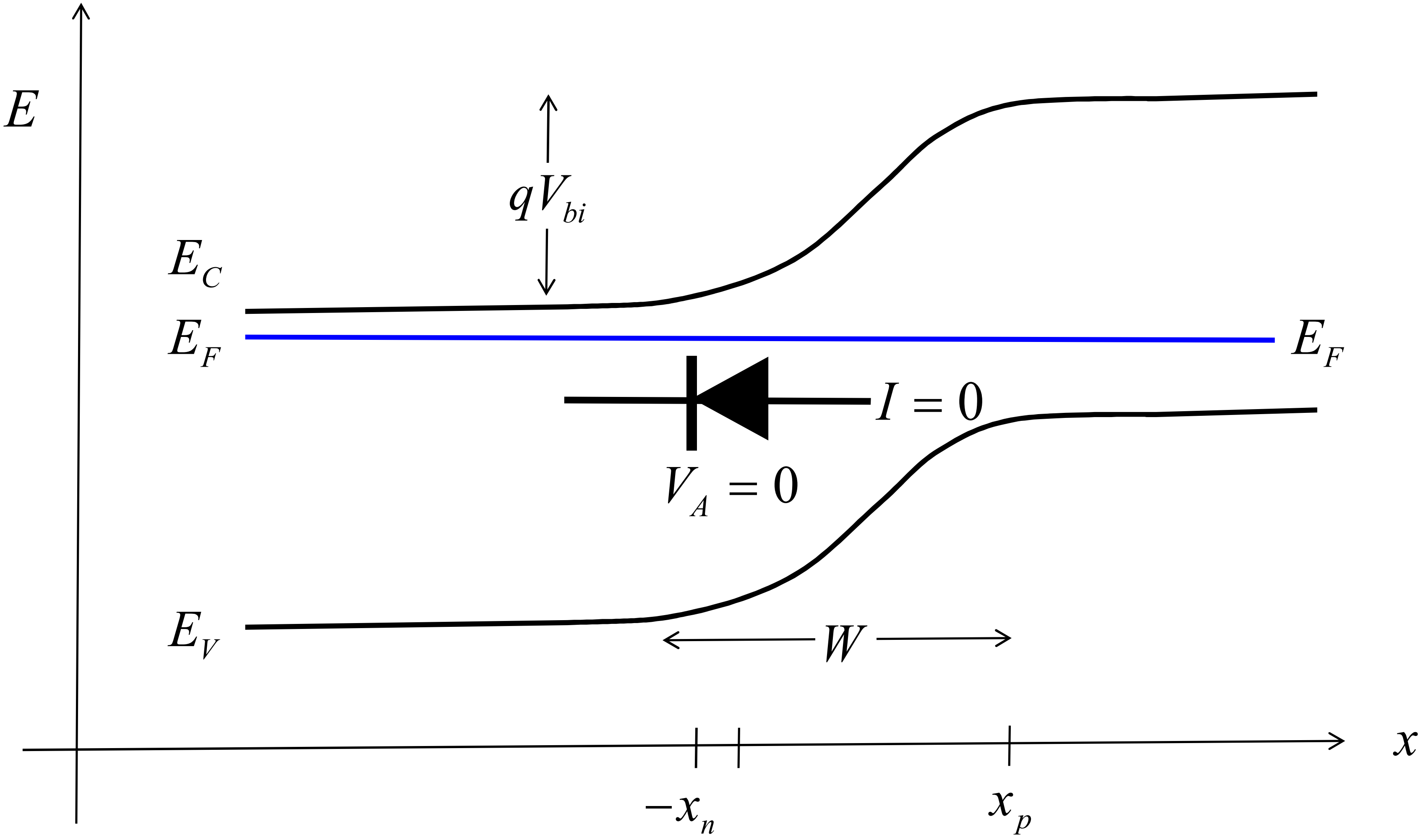
https://nanohub.org/resources/5855

ECE 557 Purdue University:

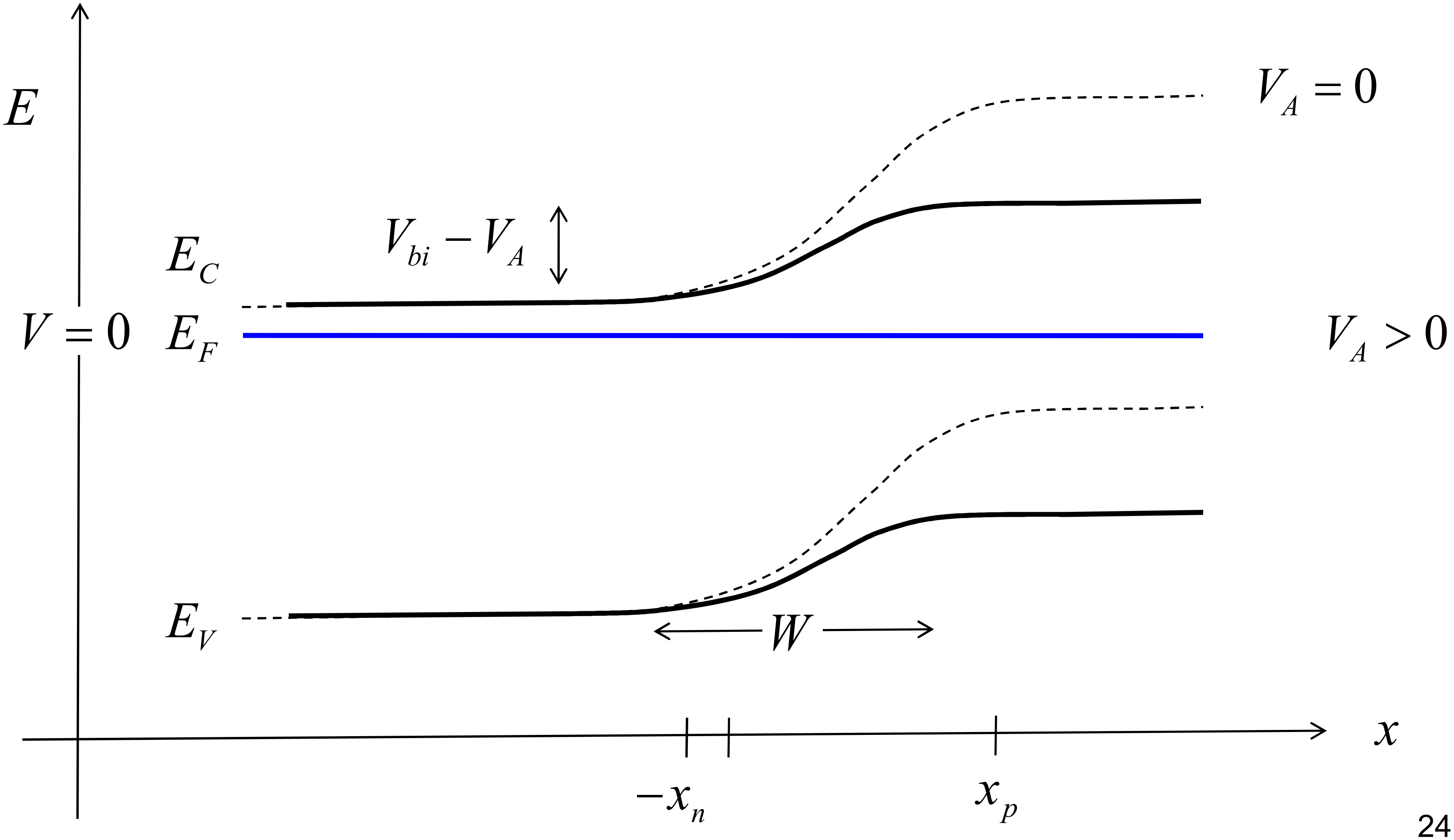
http://www.purdue.edu/newsroom/releases/2015/Q3/purdue-uses-nanotechnology-cleanroom-to-expand-undergrad-class,-expose-students-to-high-end-research.html

http://web.ics.purdue.edu/~ebaytok/projects/PMOS%20Report.pdf

equilibrium e-band diagram

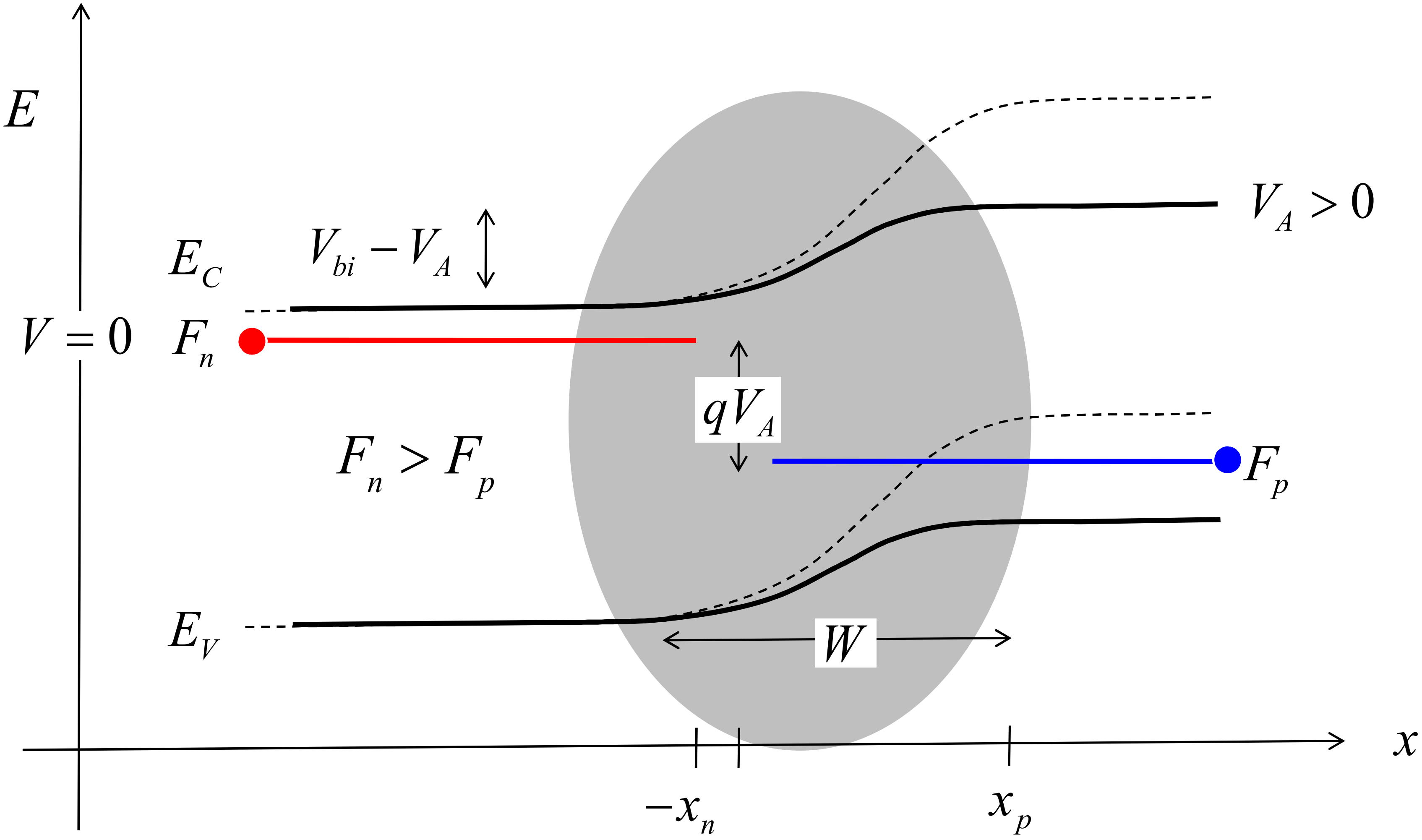


e-band diagram under forward bias

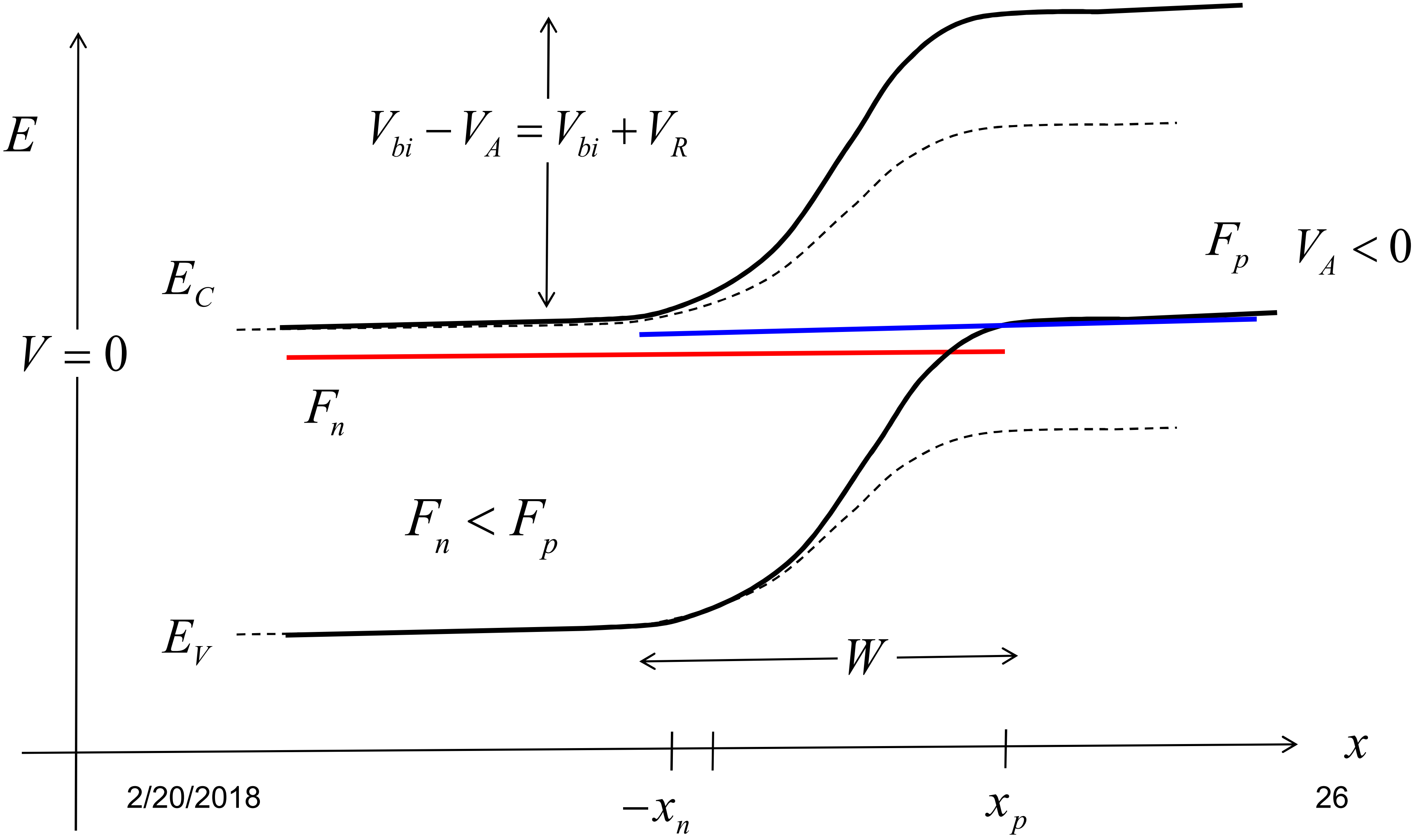


The applied voltage drops across the junction, but…

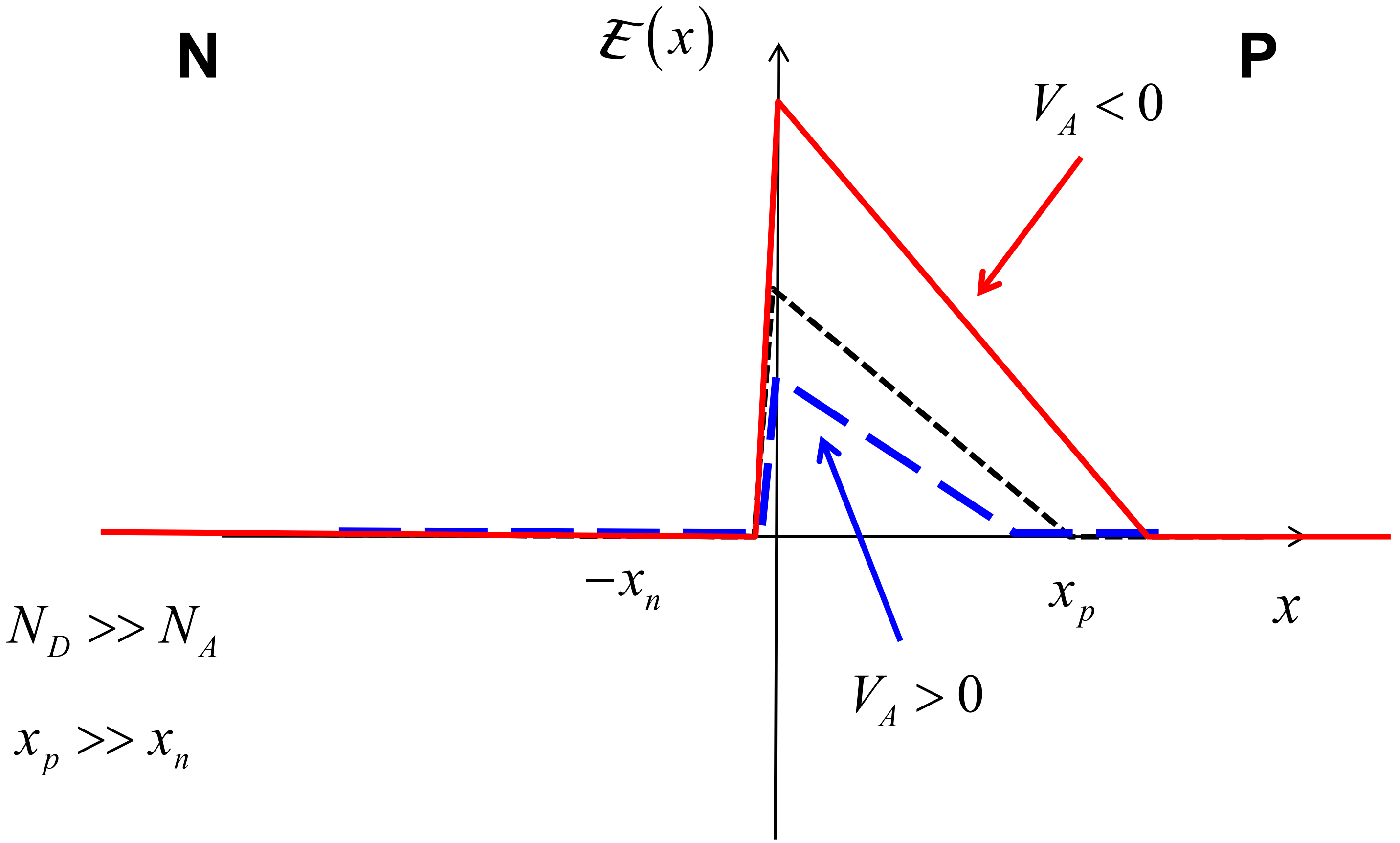
QFL’s split



e-band diagram under reverse bias



Forward bias reduces fields; Reverse bias increases them



$N_D >> N_A$

$x_p >> x_n$

key points (one-sided NP junctions)

$$V_{bi} \approx \frac{k_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

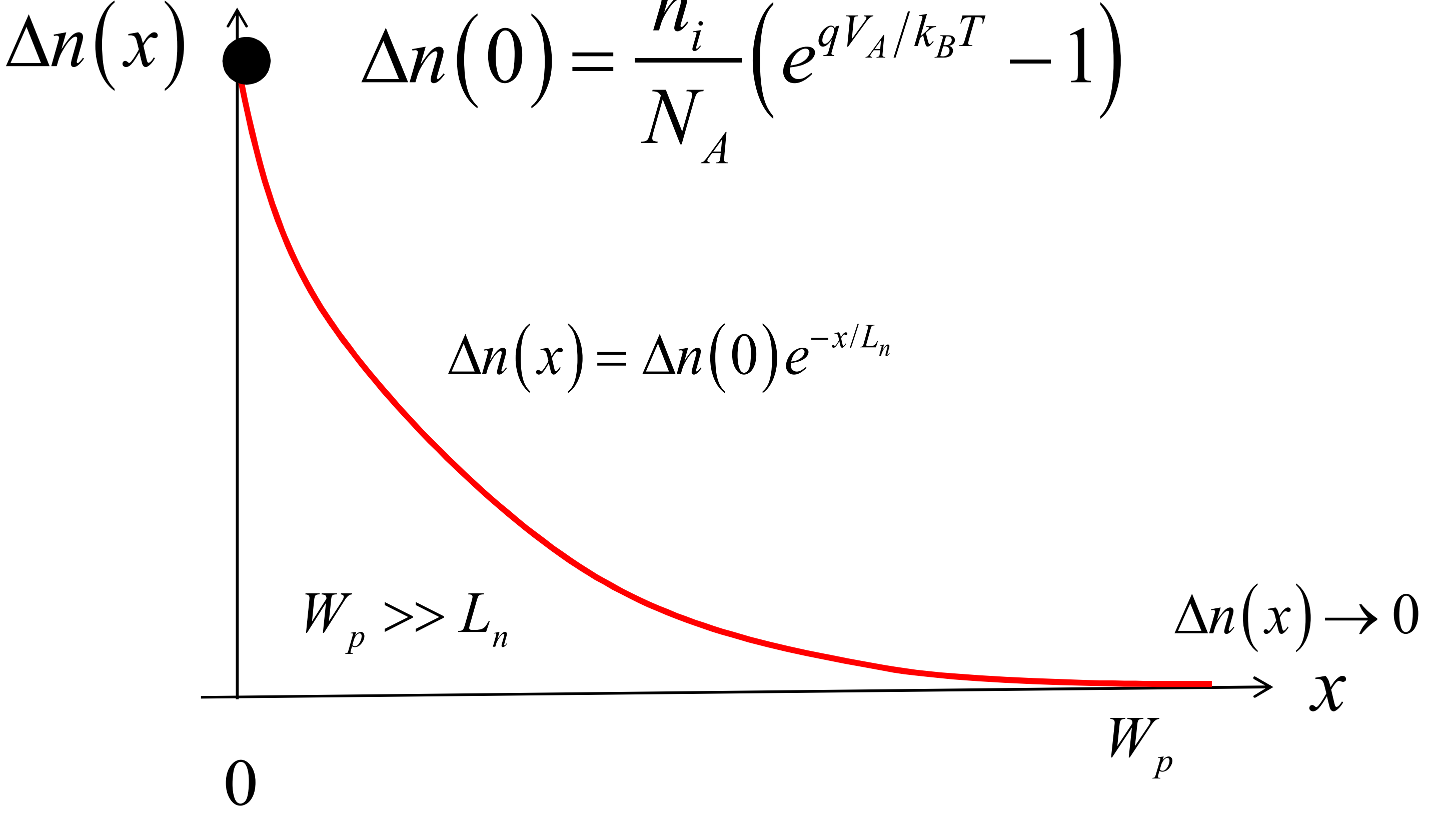
$$W = \left[\frac{2K_S\varepsilon_0}{qN_A}\left(V_{bi} - V_A\right)\right]^{1/2} \qquad W \propto \sqrt{V_{bi} - V_A} \qquad W \propto \frac{1}{\sqrt{N_A}}$$

$$\mathcal{E}(0) = \frac{2\left(V_{bi} - V_A\right)}{W} \qquad \mathcal{E}(0) \propto \sqrt{V_{bi} - V_A} \qquad \mathcal{E}(0) \propto \sqrt{N_A}$$

carrier concentrations in long regions

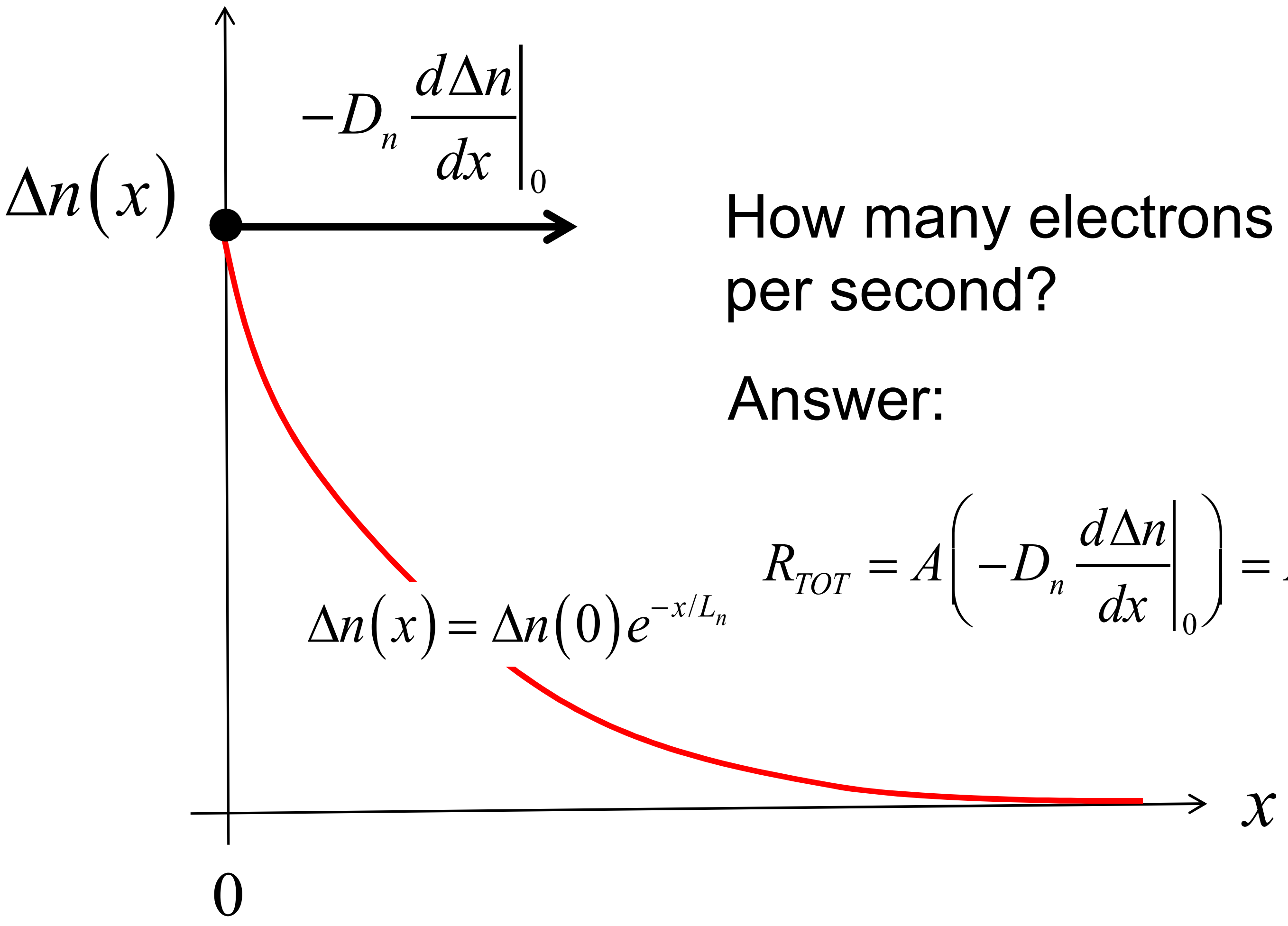
What is Δ*n*(*x*) on the p-side? Ans. **Solve the MCDE**.

$$\Delta n(0) = \frac{n_i^2}{N_A}\left(e^{qV_A/k_BT} - 1\right)$$



$$\Delta n(x) = \Delta n(0)e^{-x/L_n}$$

currents in long regions

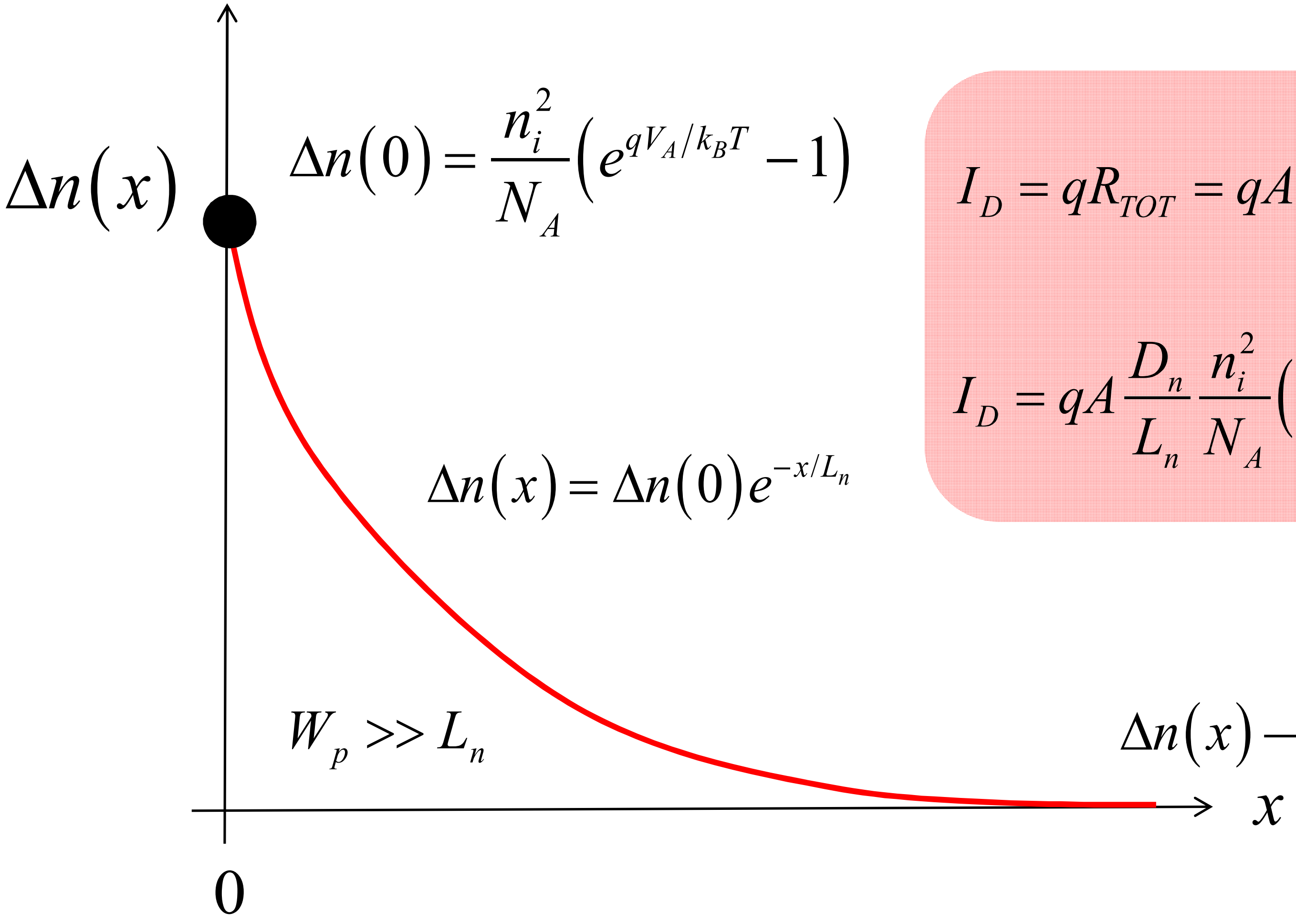


How many electrons recombine per second?

Answer:

$$R_{TOT} = A\left(-D_n \left.\frac{d\Delta n}{dx}\right|_0\right) = A\frac{D_n}{L_n}\Delta n(0)$$

currents in long regions



$$\Delta n(0) = \frac{n_i^2}{N_A}\left(e^{qV_A/k_BT} - 1\right)$$

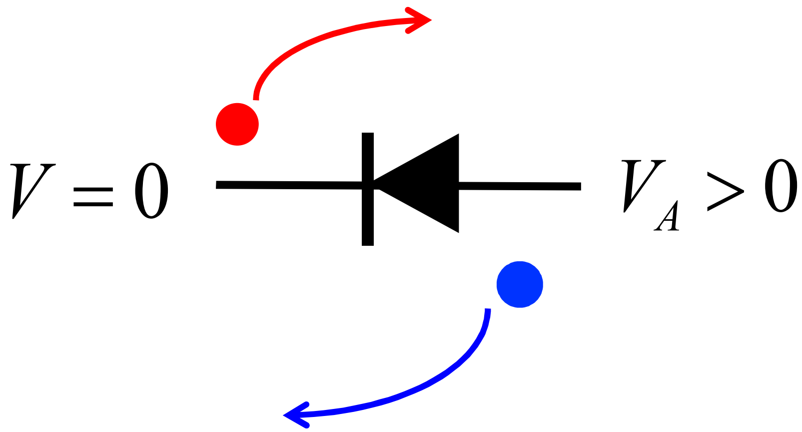
$$\Delta n(x) = \Delta n(0) e^{-x/L_n}$$

$$I_D = qR_{TOT} = qA\frac{D_n}{L_n}\Delta n(0)$$

$$I_D = qA\frac{D_n}{L_n}\frac{n_i^2}{N_A}\left(e^{qV_A/k_BT} - 1\right)$$

diode current in long regions

$$I_n = \frac{qA\Delta n(0) D_n}{L_n} = qA\left(\frac{D_n}{L_n}\frac{n_i^2}{N_A}\right)\left(e^{qV_A/k_BT} - 1\right)$$



$$I_p = \frac{qA\Delta p(0) D_p}{L_p} = qA\left(\frac{D_p}{L_p}\frac{n_i^2}{N_D}\right)\left(e^{qV_A/k_BT} - 1\right)$$

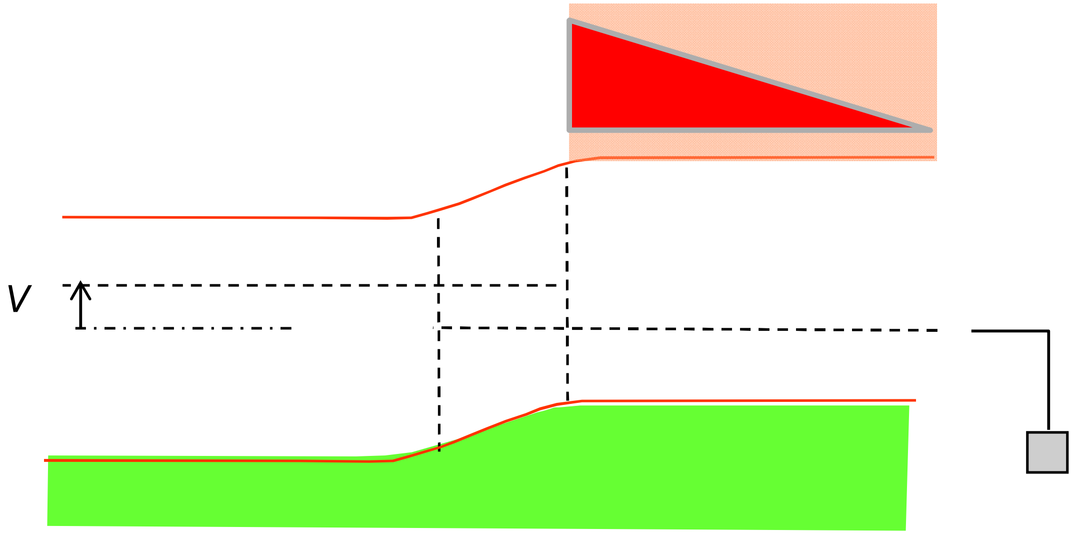
$$I_D(V_A) = I_p(V_A) + I_n(V_A)\ \mathrm{A}$$

carrier concentrations in short regions

What is Δ*n*(*x*) on the p-side? Ans. **Solve the MCDE**.

$$D_N \frac{d^2 n}{dx^2} = 0$$

$$\Delta n(x,t) = C + Dx$$



$$x = W_p, \quad \Delta n(x = W_p) = 0 \Rightarrow C = -DW_p$$

$$x = 0', \quad \Delta n(x = 0) = \frac{n_i^2}{N_A}\left(e^{qV_A\beta} - 1\right) = C$$

$$\Delta n(x,t) = \frac{n_i^2}{N_A}\left(e^{qV_A\beta} - 1\right)\left(1 - \frac{x}{W_p}\right)$$

currents in short regions

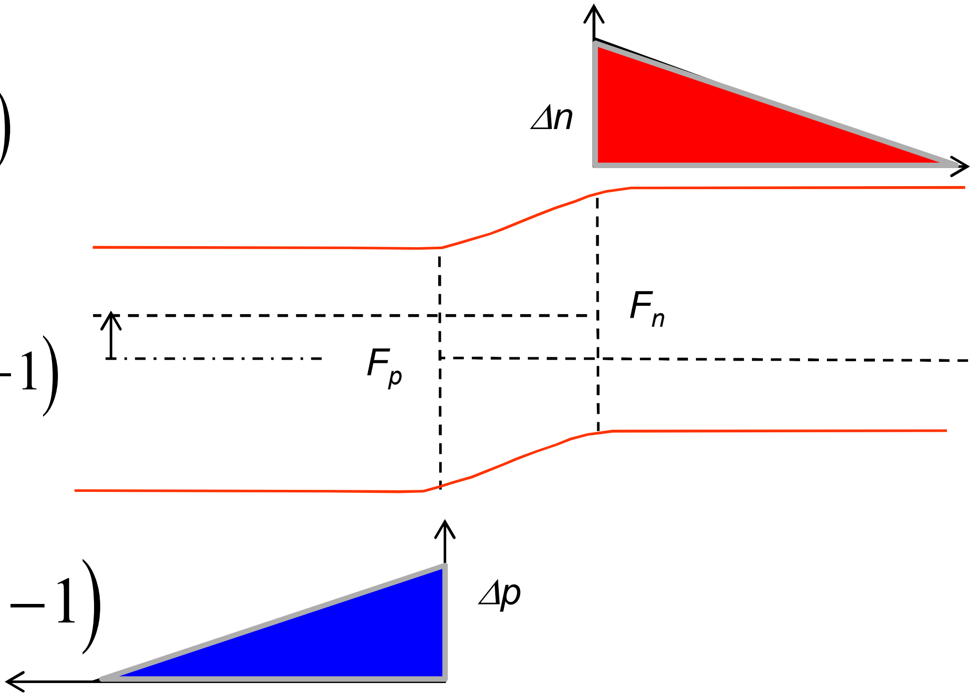
$$\Delta n(x) = \frac{n_i^2}{N_A}\left(e^{qV_A\beta} - 1\right)\left(1 - \frac{x}{W_p}\right)$$

$$\mathbf{J}_N = qn\mu_N\mathcal{E} + qD_N\nabla n$$

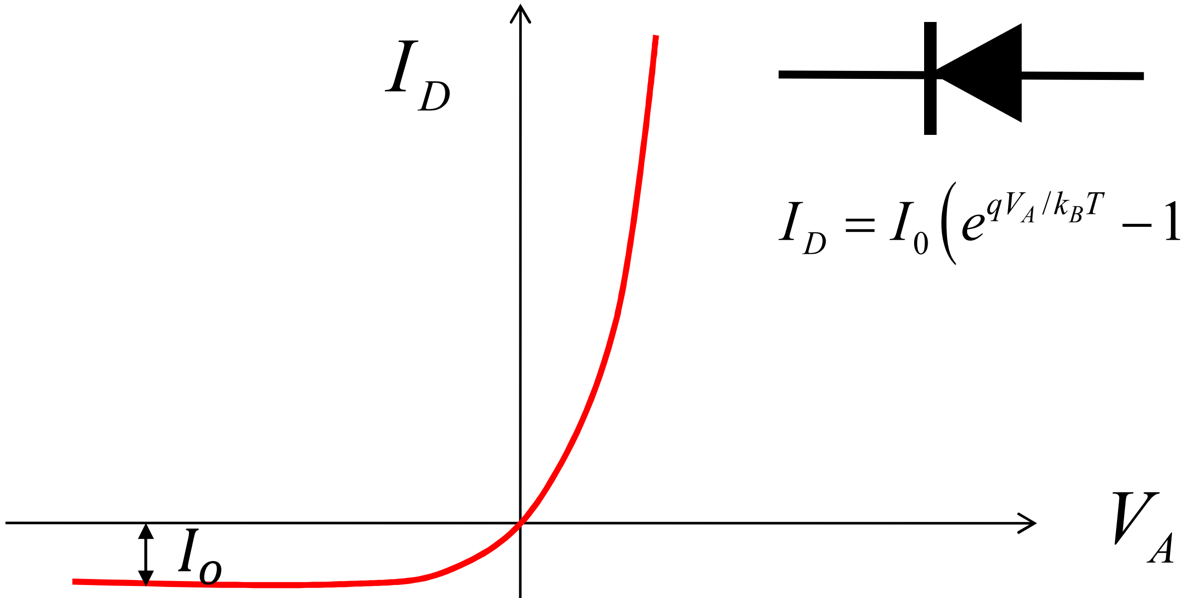
$$J_n = qD_n \left.\frac{dn}{dx}\right|_{x=0} = -\frac{qD_n}{W_p}\frac{n_i^2}{N_A}\left(e^{qV_A\beta} - 1\right)$$

$$J_p = -qD_p \left.\frac{dp}{dx}\right|_{x=0'} = -\frac{qD_p}{W_n}\frac{n_i^2}{N_D}\left(e^{qV_A\beta} - 1\right)$$

$$J_T = -q\left[\frac{D_n}{W_p}\frac{n_i^2}{N_A} + \frac{D_p}{W_n}\frac{n_i^2}{N_D}\right]\left(e^{qV_A\beta} - 1\right)$$



ideal diode equation summary



$$I_D = I_0\left(e^{qV_A/k_BT} - 1\right)$$

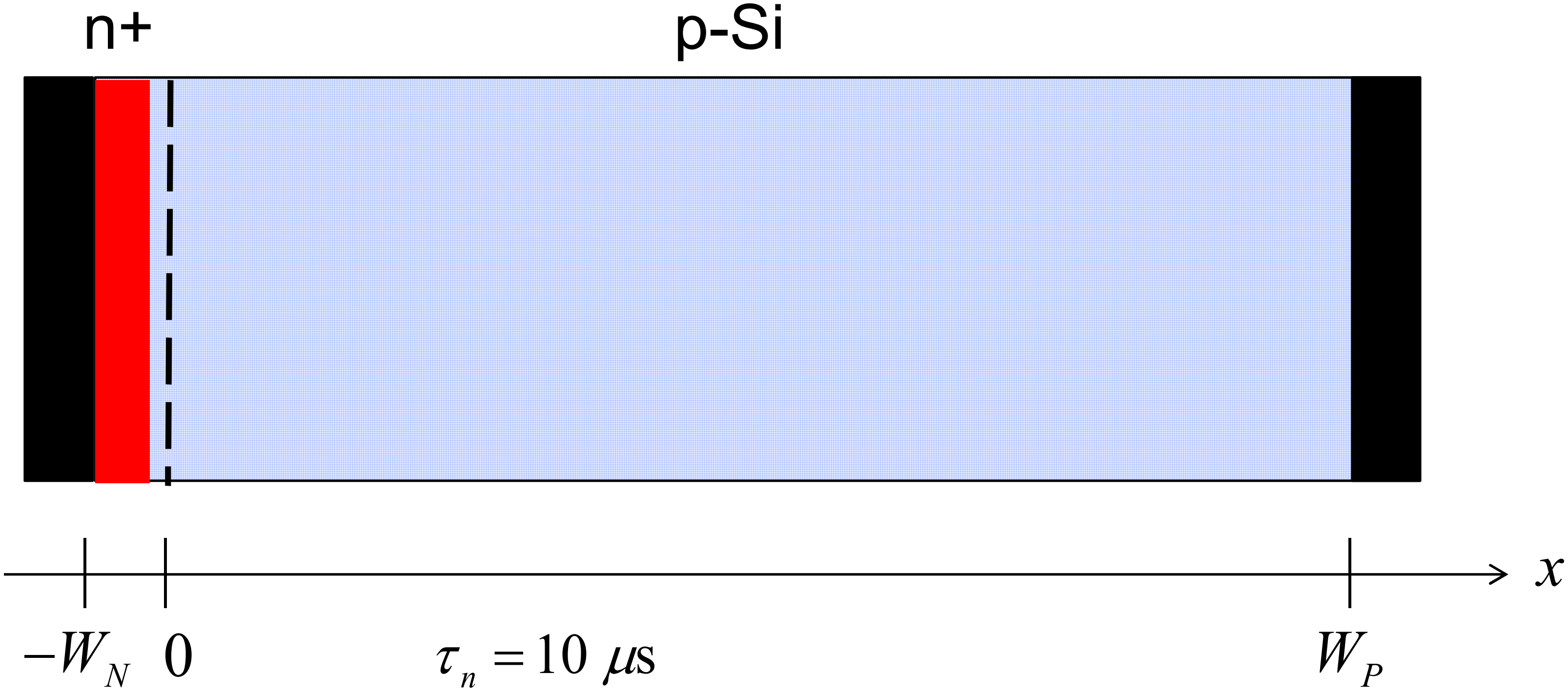
long

$$I_0 = qA\left(\frac{D_n}{L_n}\frac{n_i^2}{N_A} + \frac{D_p}{L_p}\frac{n_i^2}{N_D}\right)$$

short

$$I_0 = qA\left(\frac{D_n}{W_P}\frac{n_i^2}{N_A} + \frac{D_p}{W_N}\frac{n_i^2}{N_D}\right)$$

example



$\tau_n = 10\ \mu s$

$N_D = 10^{20}\ \text{cm}^{-3}$

$W_N = 0.1\ \mu m$

$\tau_p = 1\ \mu s$

$N_A = 10^{17}\ \text{cm}^{-3}$

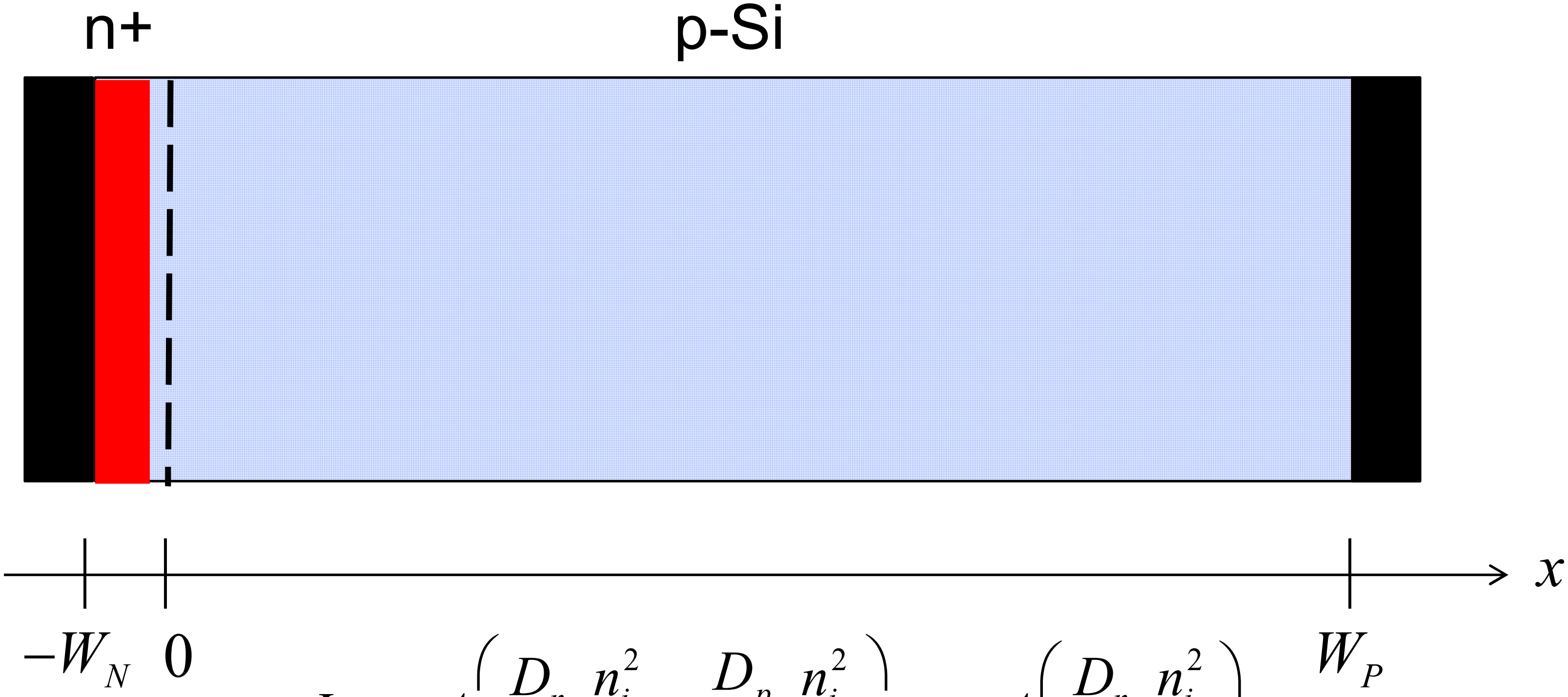
$W_P = 10\ \mu m$

$$I_D = I_0\left(e^{qV_A/k_BT} - 1\right)$$

$$I_0 = ?$$

Is this a one-sided diode?

example: one-sided diodes



$$I_0 = qA\left(\frac{D_n}{L_n}\frac{n_i^2}{N_A} + \frac{D_p}{L_p}\frac{n_i^2}{N_D}\right) \rightarrow qA\left(\frac{D_n}{L_n}\frac{n_i^2}{N_A}\right)$$

$$I_0 = qA\left(\frac{D_n}{W_P}\frac{n_i^2}{N_A} + \frac{D_p}{W_n}\frac{n_i^2}{N_D}\right) \rightarrow qA\left(\frac{D_n}{W_P}\frac{n_i^2}{N_A}\right)$$

conclusions

- Semiconductor fabrication is a mature, highly reproducible technology that underpins electronic devices we use today
- Each fabrication step is arranged in a logical sequence to create specific devices like interconnects and PN junctions
- PN junctions under bias act as ideal diodes; their properties (such as dark current) can be predicted from underlying materials, doping, and geometries