ECE-305: Spring 2018
MOS Capacitors and Transistors

Pierret, *Semiconductor Device Fundamentals* (SDF)
Chapters 15+16 (pp. 525-530, 563-599)

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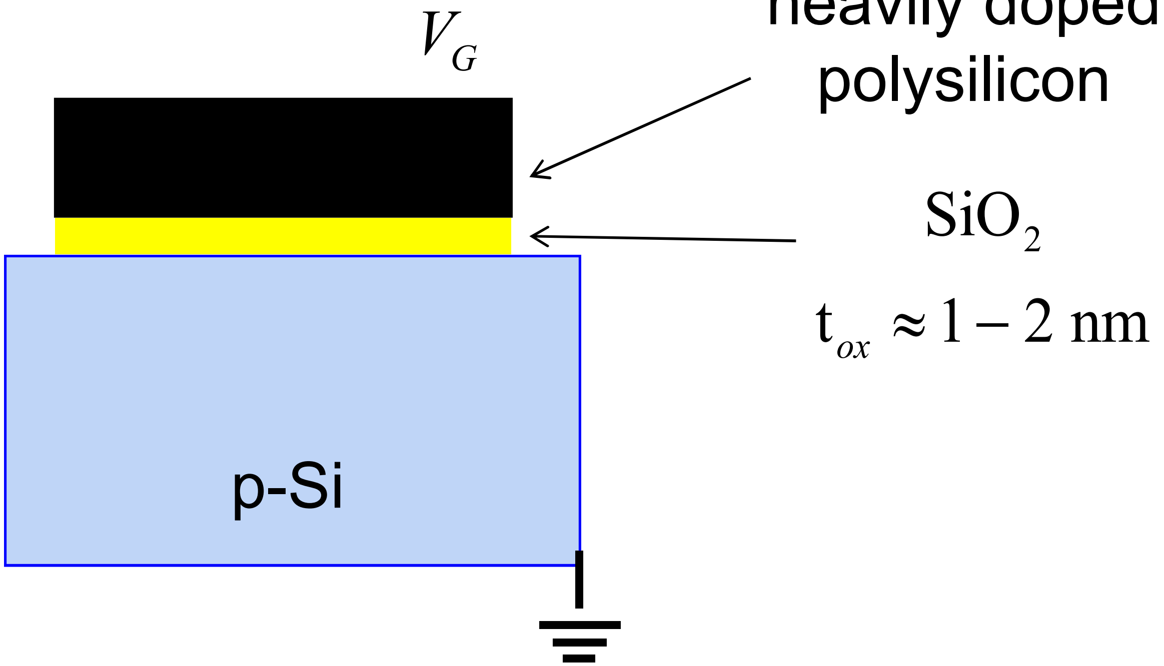
MOS capacitor

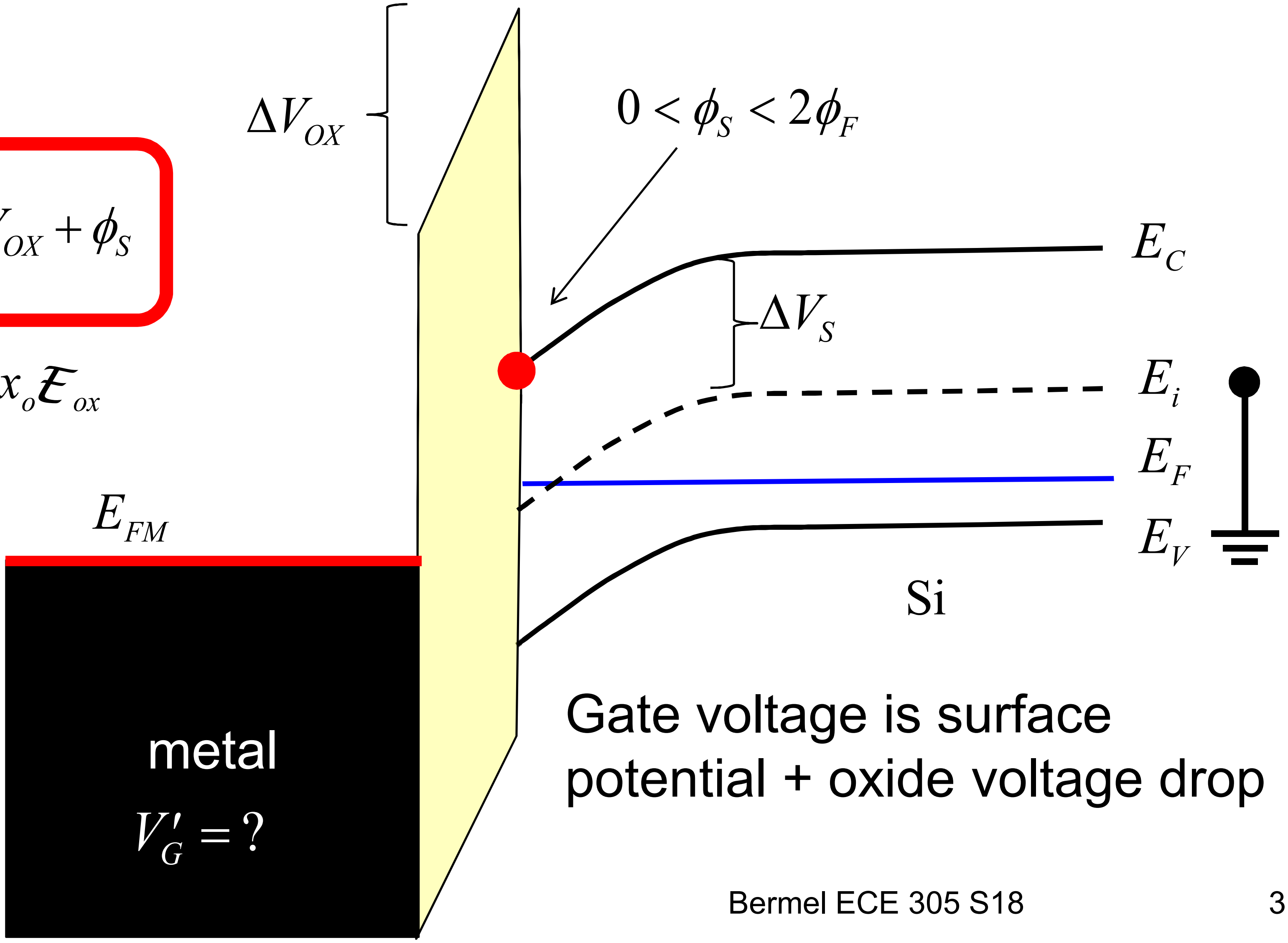
1) Gate voltage
2) Example problem
3) MOS capacitors
4) MOS field-effect transistors



gate voltage and surface potential

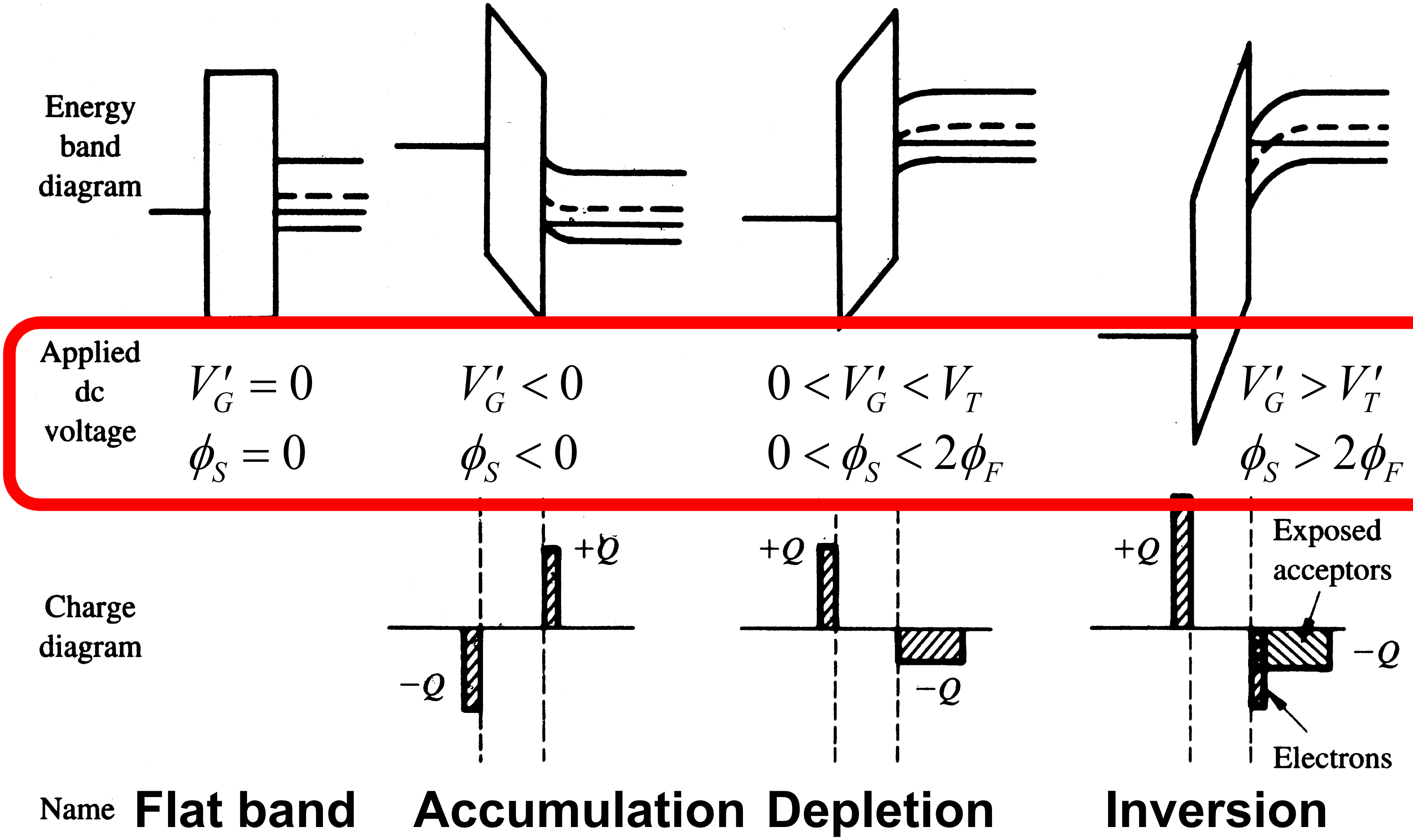
$$\boxed{V_G' = \Delta V_{OX} + \phi_S}$$

$$\Delta V_{ox} = x_o \mathcal{E}_{ox}$$



Gate voltage is surface potential + oxide voltage drop

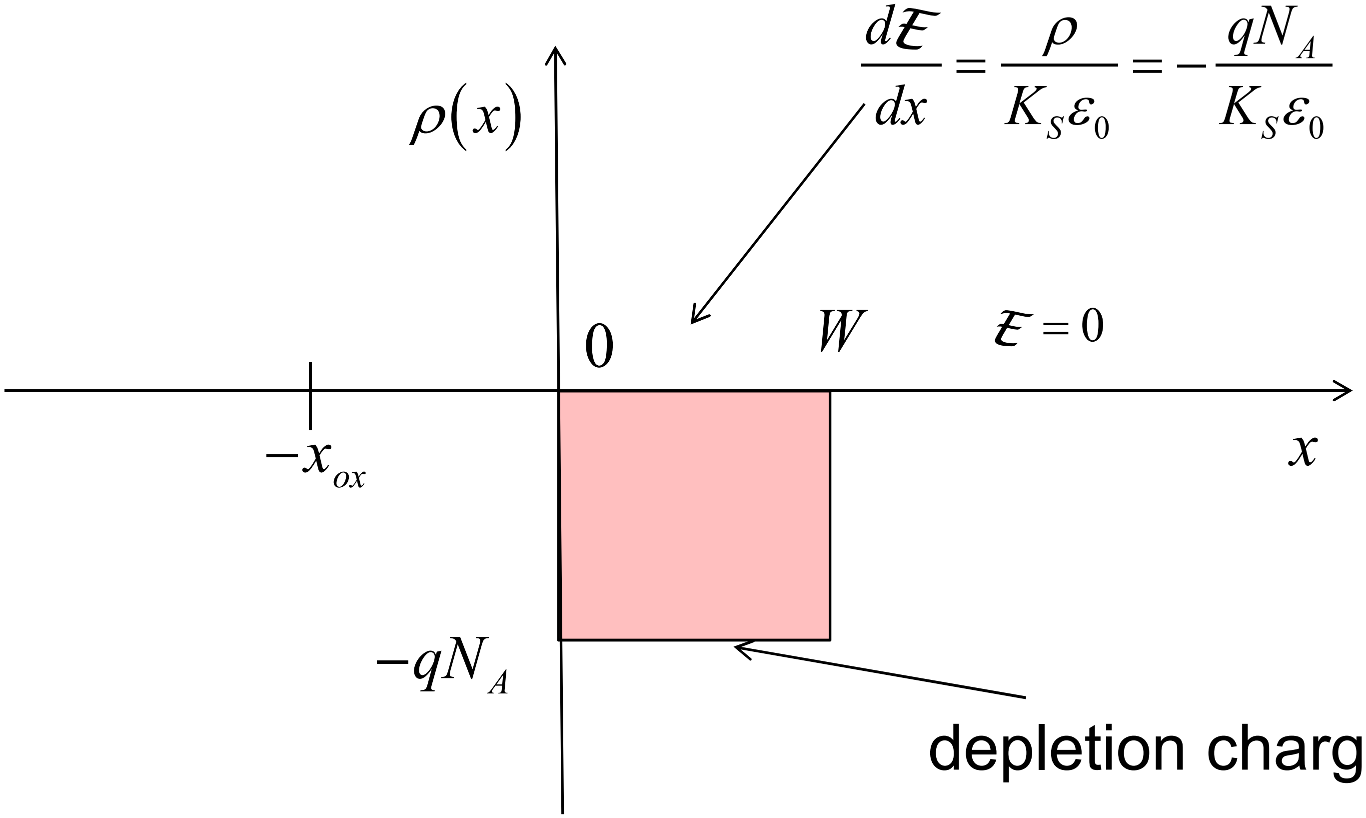
band banding in p-type MOS



Name	Flat band	Accumulation	Depletion	Inversion
Applied dc voltage	$V_G' = 0$ $\phi_S = 0$	$V_G' < 0$ $\phi_S < 0$	$0 < V_G' < V_T$ $0 < \phi_S < 2\phi_F$	$V_G' > V_T'$ $\phi_S > 2\phi_F$

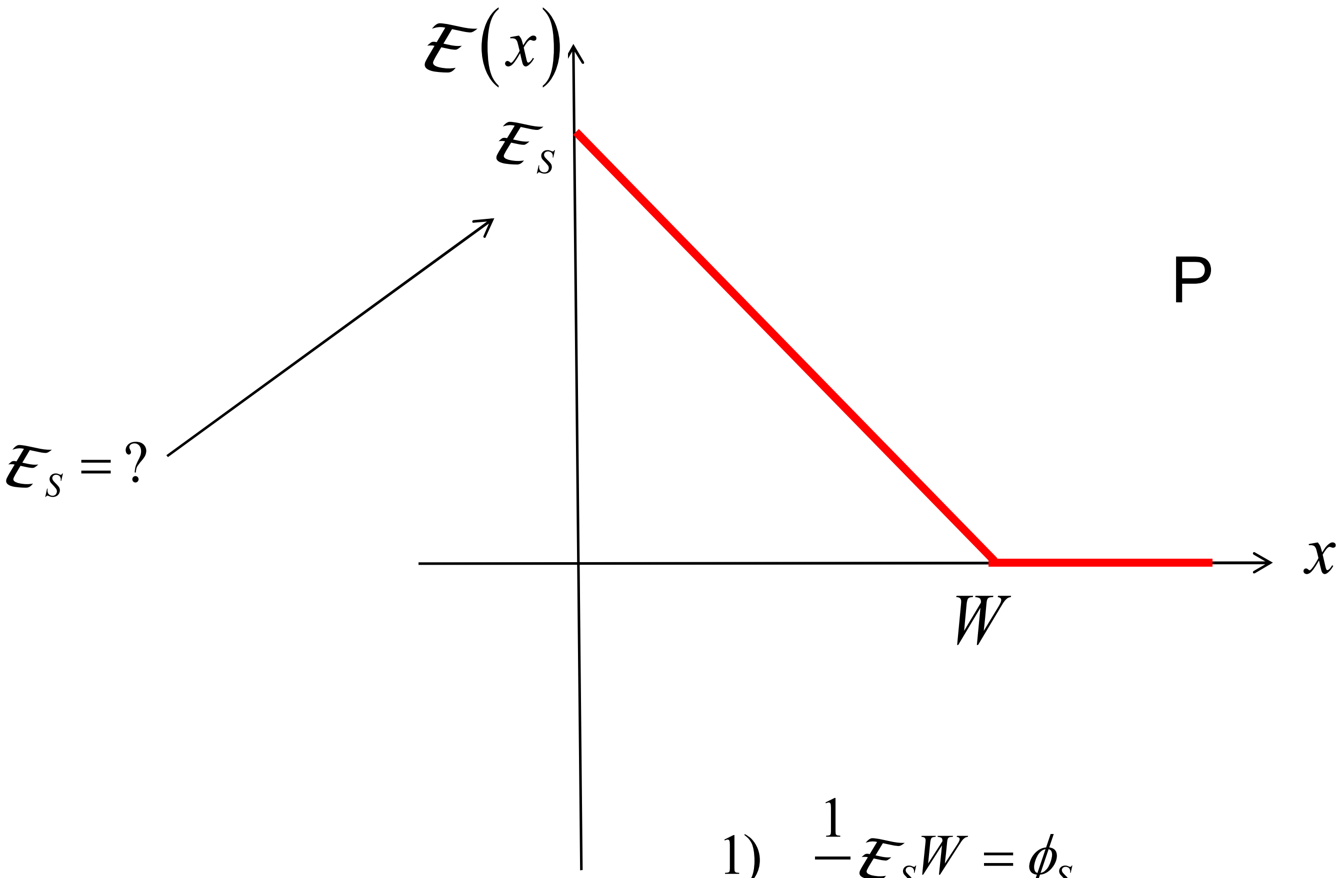
Fig. 16.6, Semiconductor Device Fundamentals, R.F. Pierret

space charge density vs. position



depletion charge

electric field (semiconductor)



$\mathcal{E}_S = ?$

1) $\frac{1}{2}\mathcal{E}_S W = \phi_S$

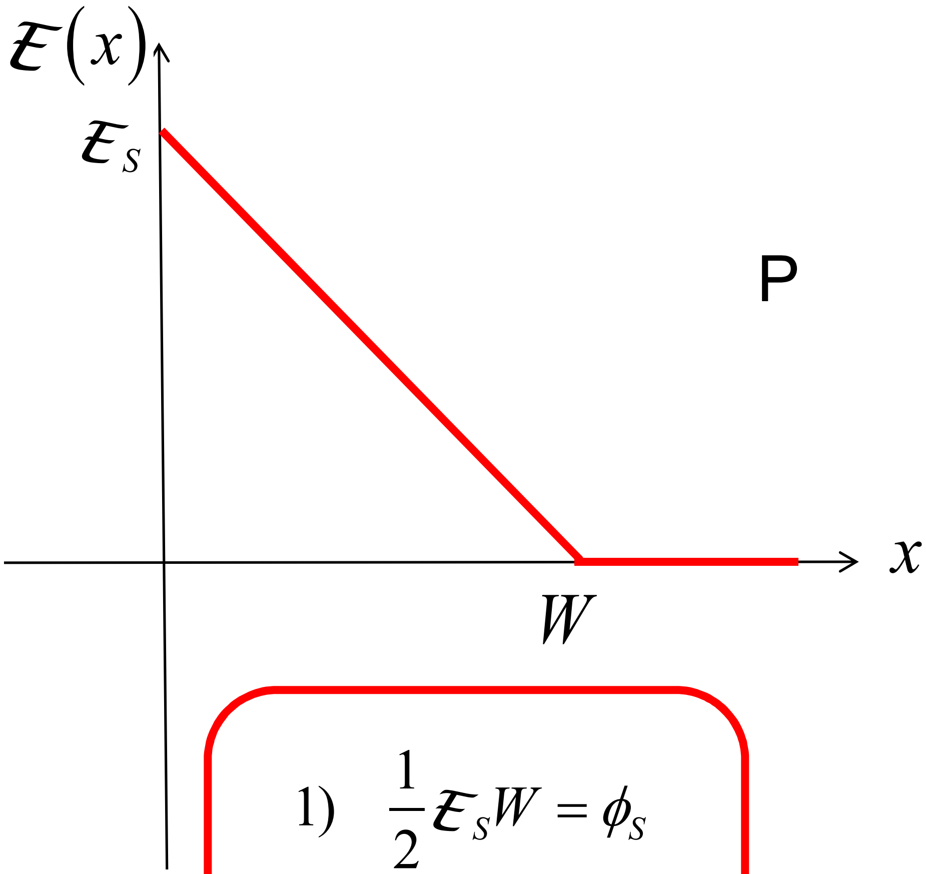
surface electric field (semiconductor)

$$\frac{d\mathcal{E}}{dx} = -\frac{qN_A}{K_S\varepsilon_0}$$

$$d\mathcal{E} = -\frac{qN_A}{K_S\varepsilon_0}dx$$

$$\int_{\mathcal{E}(W)}^{\mathcal{E}(0)} d\mathcal{E} = -\frac{qN_A}{K_S\varepsilon_0}\int_W^0 dx$$

$$2)\quad \mathcal{E}_S = \frac{qN_AW}{K_S\varepsilon_0}$$



$$1)\quad \frac{1}{2}\mathcal{E}_S W = \phi_S$$

$$2)\quad \mathcal{E}_S = \frac{qN_AW}{K_S\varepsilon_0}$$

final answers (MOS in depletion)

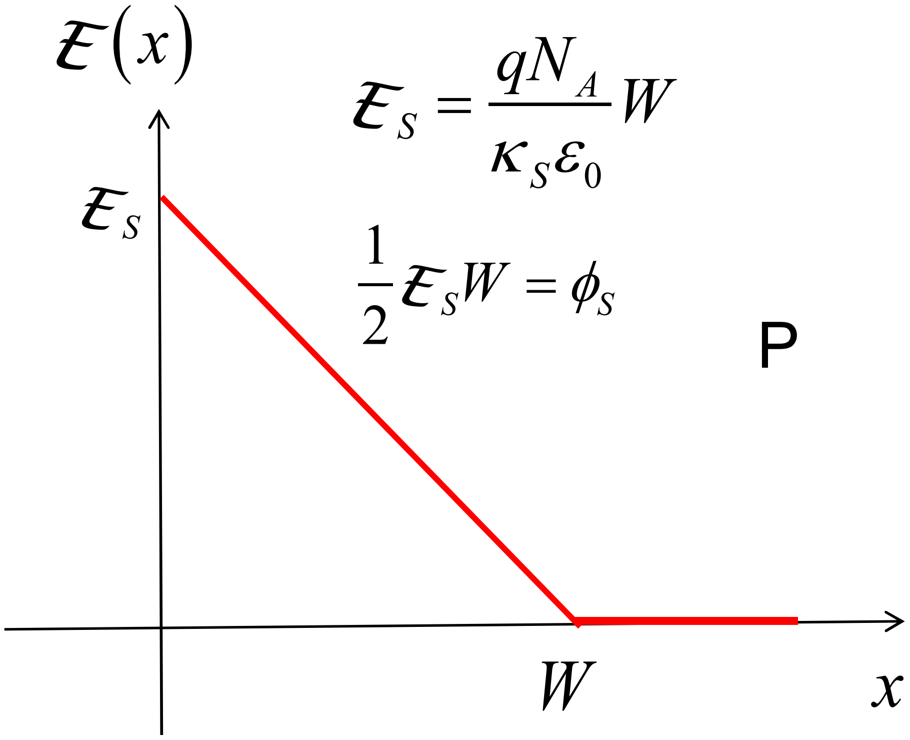
$$W = \sqrt{\frac{2\kappa_S \varepsilon_0 \phi_S}{qN_A}}\ \text{cm}$$

$$\mathcal{E}_S = \sqrt{\frac{2qN_A\phi_S}{\kappa_s \varepsilon_0}}\ \text{V/cm}$$

$$Q_B = -qN_A W\left(\phi_S\right)\ \text{C/cm}^2$$

$$Q_B\left(\phi_S\right) = -\sqrt{2q\kappa_s\varepsilon_0 N_A \phi_S}\ \text{C/cm}^2$$

$$0 < \phi_S < 2\phi_F$$

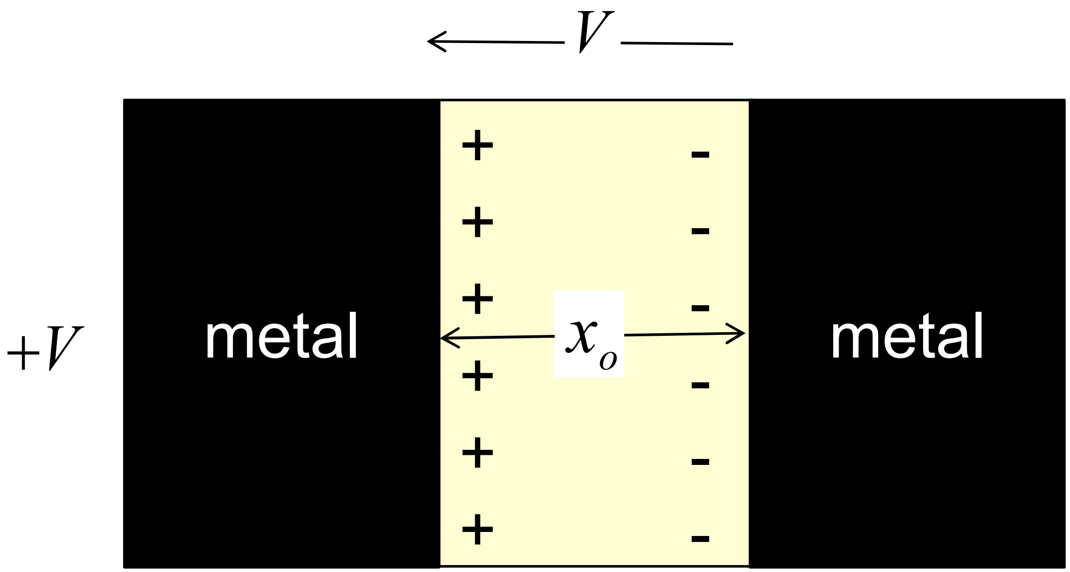


$$\mathcal{E}_S = \frac{qN_A}{\kappa_S\varepsilon_0}W$$

$$\frac{1}{2}\mathcal{E}_S W = \phi_S$$

What gate voltage produced this surface potential?

voltage drop across a capacitor



$$C_{ox} = -\frac{Q/A}{V}$$

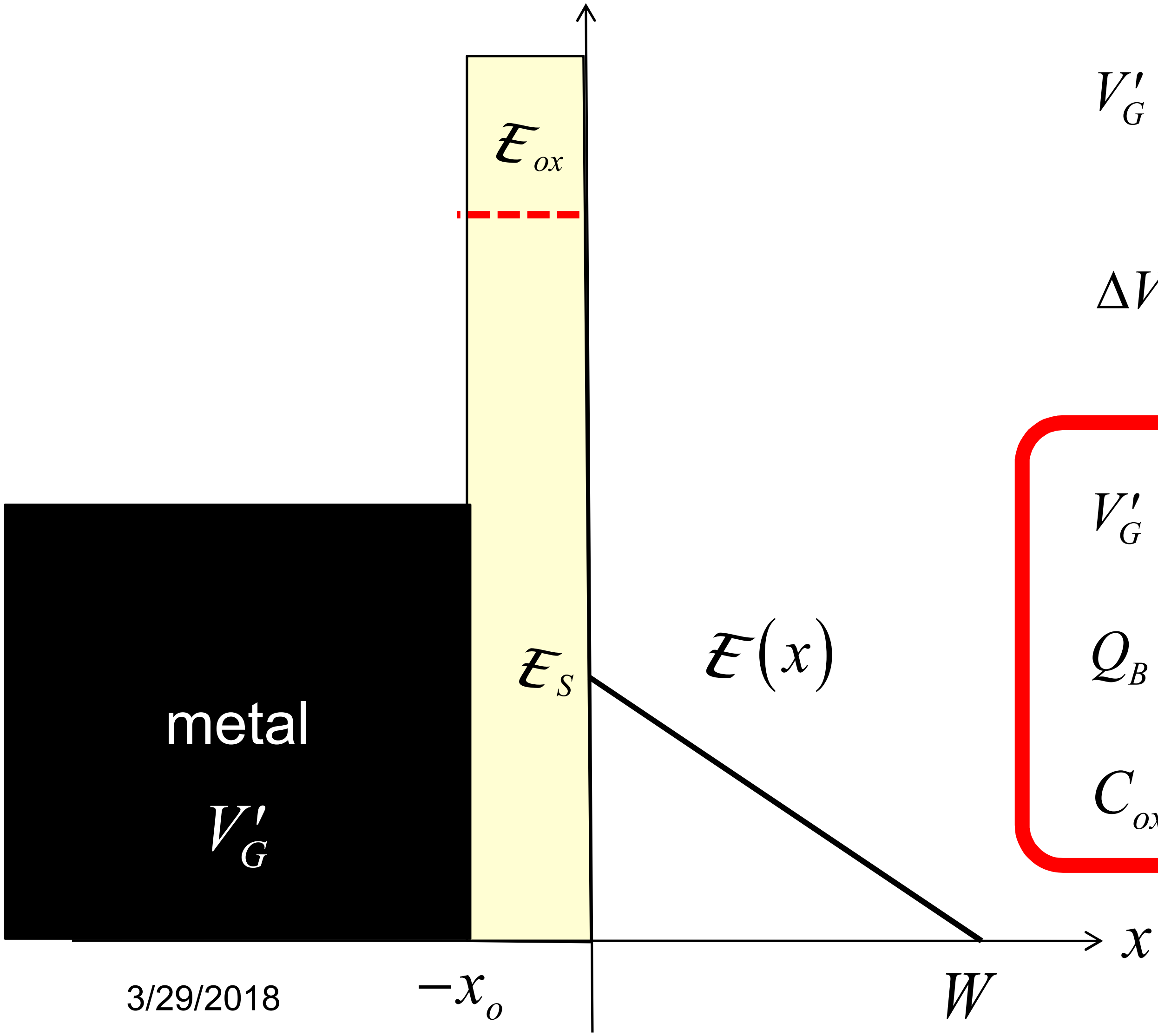
$$\boxed{V = -\frac{Q/A}{C_{ox}}}$$

$$C \equiv \frac{Q}{V} = \frac{K_O \varepsilon_0 A}{x_o} = \mathrm{F}$$

$$Q/A \ \ \mathrm{C/cm^2}$$

$$\frac{C}{A} \equiv \frac{Q/A}{V} = \frac{K_O \varepsilon_0}{x_o} = C_{ox} \ \mathrm{F/cm^2}$$

relation to gate voltage



$$V_G' = \Delta V_{ox} + \phi_S$$

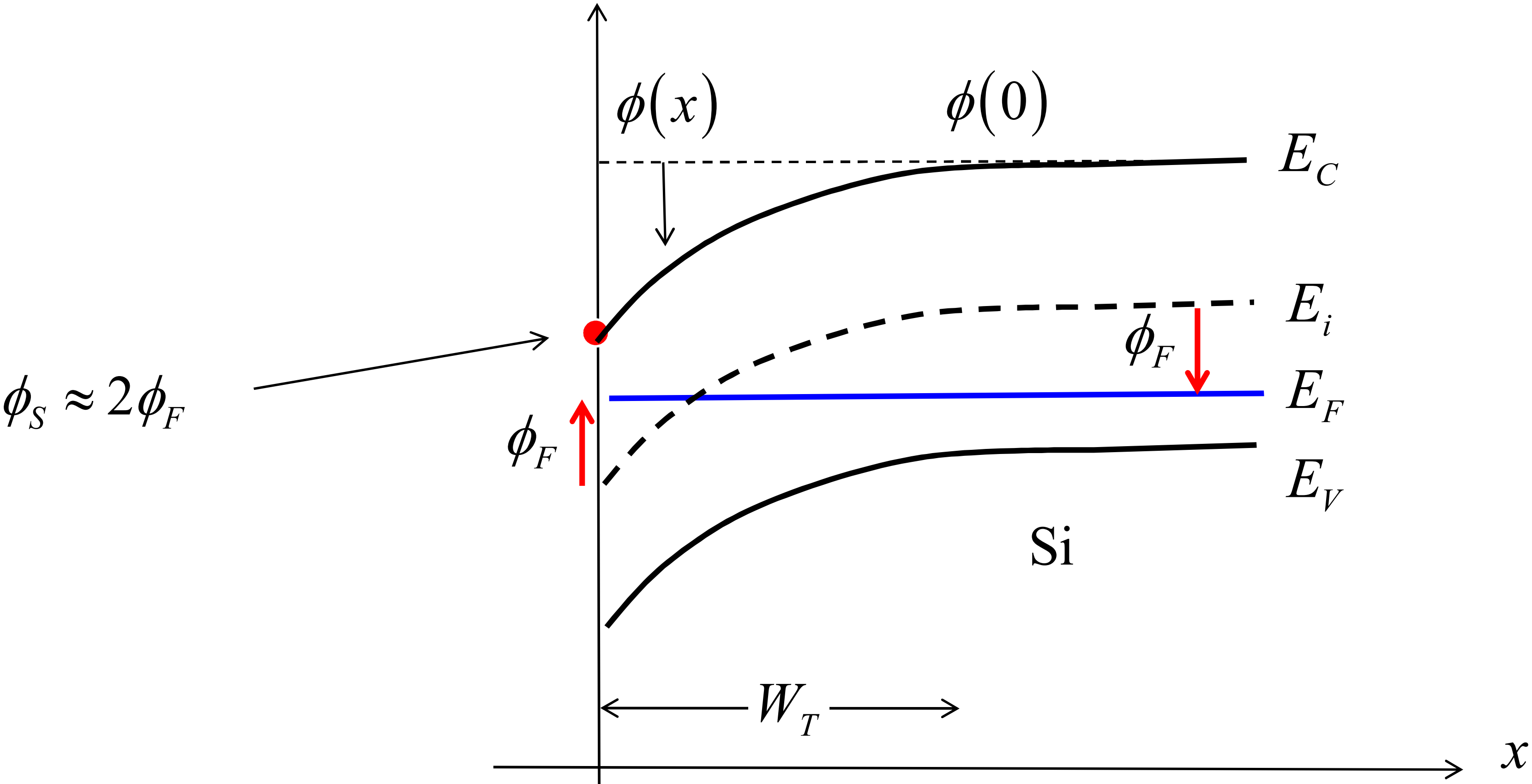
$$\Delta V_{ox} = \frac{-Q_B(\phi_S)}{C_{OX}}$$

$$V_G' = -\frac{Q_B(\phi_S)}{C_{ox}} + \phi_S$$

$$Q_B(\phi_S) = -qN_A W(\phi_S)$$

$$C_{ox} = K_O \varepsilon_0 / x_o$$

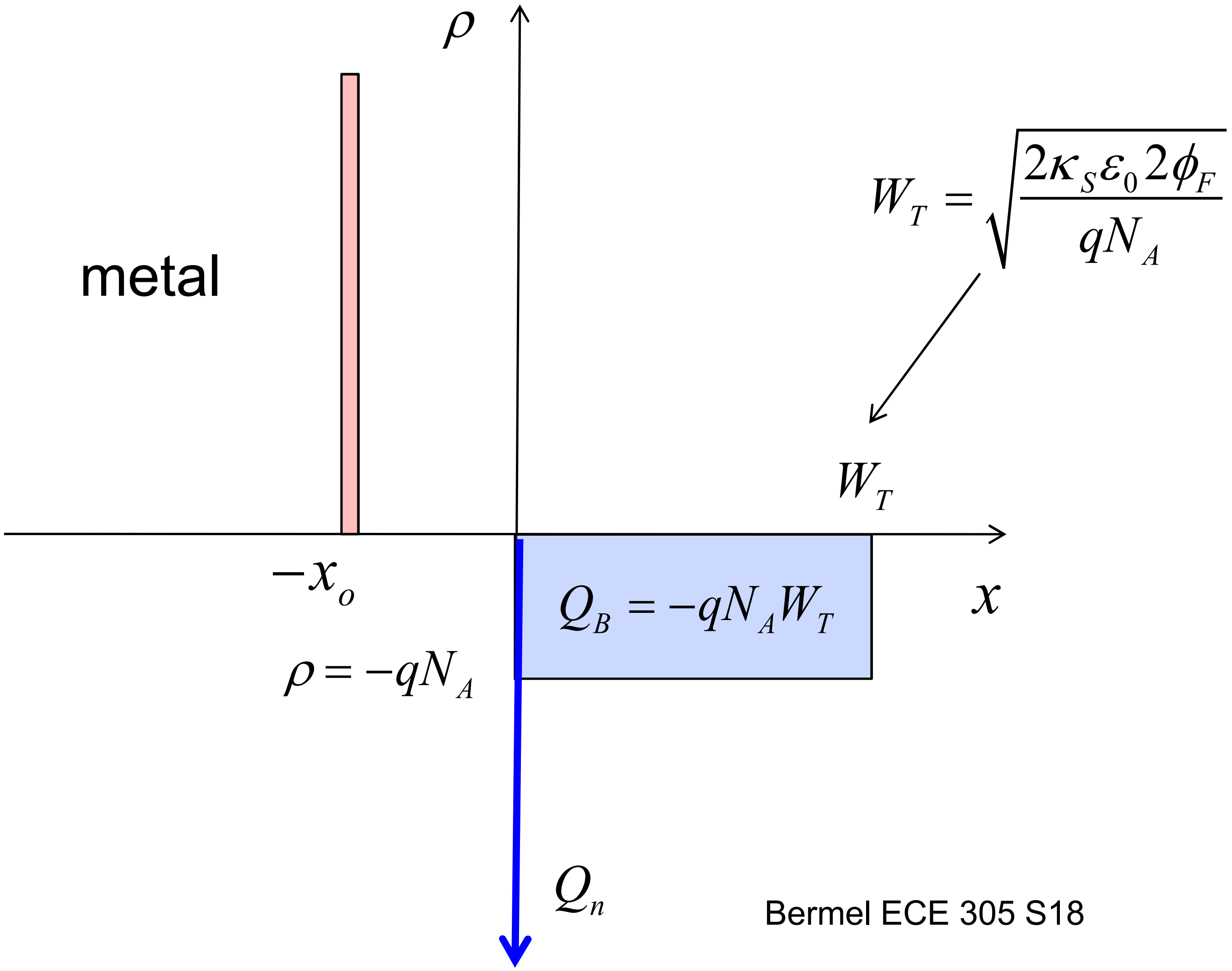
MOS electrostatics: **inversion**



$$W_T = \left[\frac{2K_S\varepsilon_0}{qN_A}2\phi_F\right]^{1/2}$$

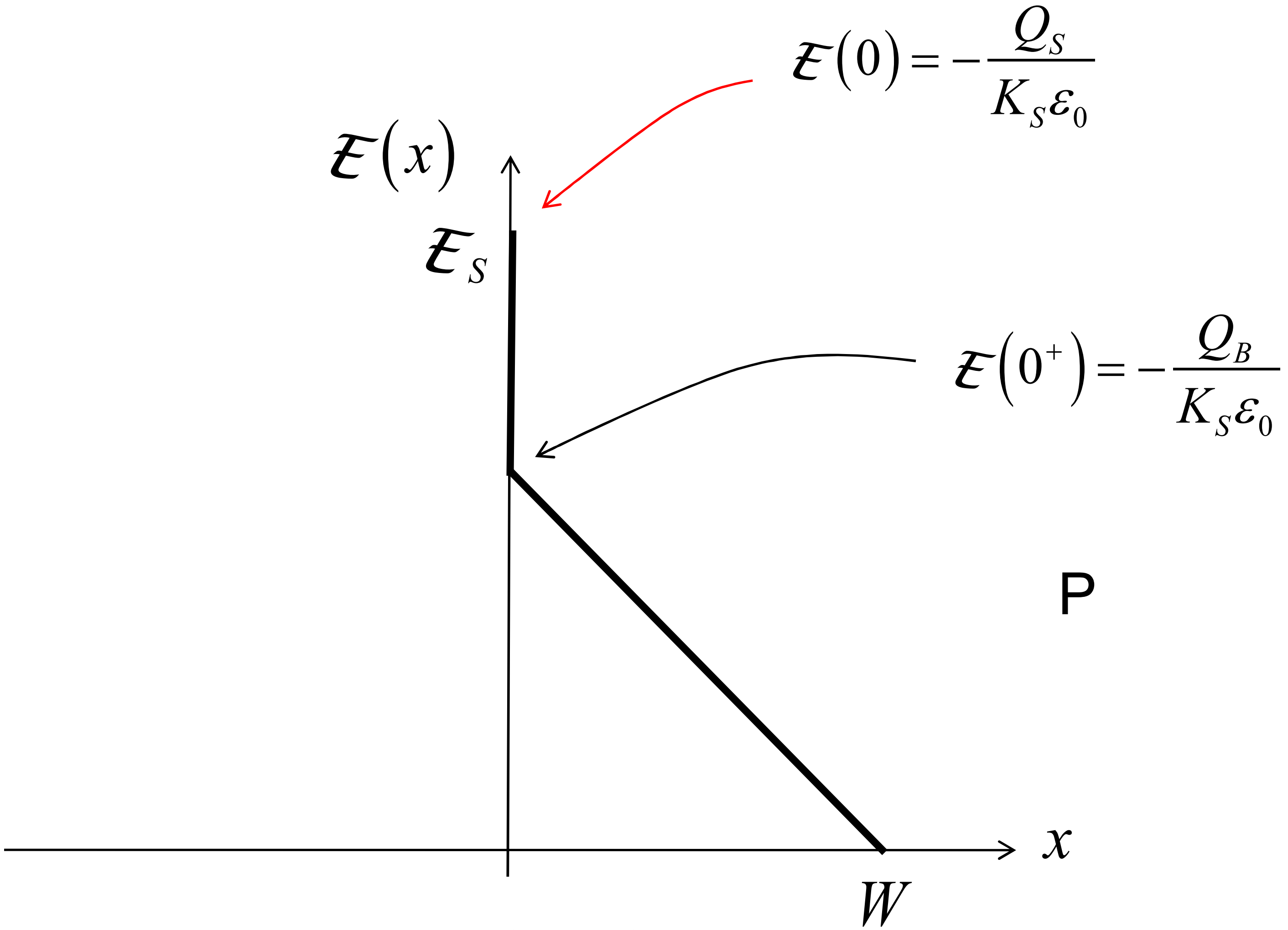
Maximum depletion region depth

delta-depletion approximation



$$W_T = \sqrt{\frac{2\kappa_S \varepsilon_0 2\phi_F}{qN_A}}$$

delta-depletion approximation



$$\mathcal{E}(0) = -\frac{Q_S}{K_S \varepsilon_0}$$

$$\mathcal{E}(0^+) = -\frac{Q_B}{K_S \varepsilon_0}$$

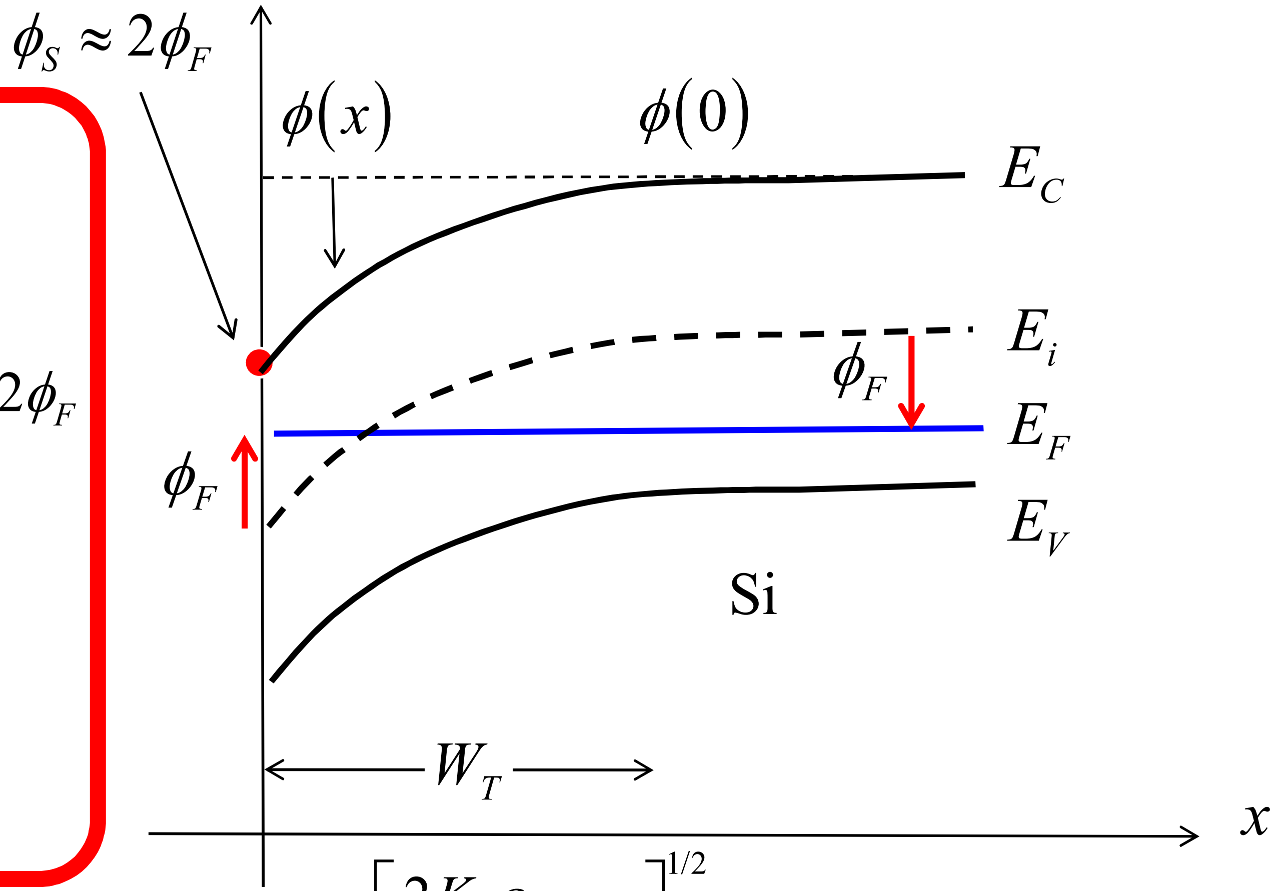
MOS electrostatics: inversion

$$V_G' = -\frac{Q_S}{C_{ox}} + 2\phi_F$$

$$V_G' = -\frac{Q_B(2\phi_F) + Q_n}{C_{ox}} + 2\phi_F$$

$$V_T' = -\frac{Q_B(2\phi_F)}{C_{ox}} + 2\phi_F$$

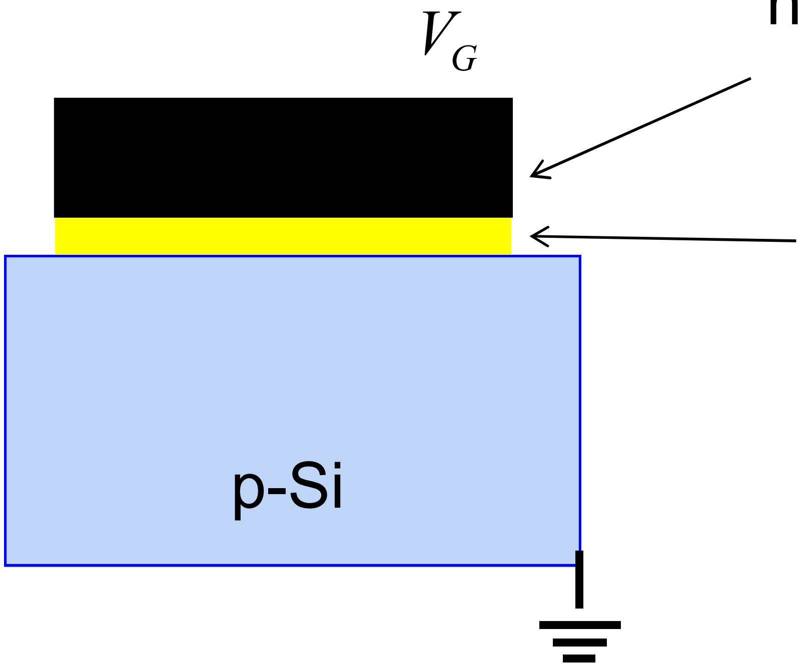
$$Q_n = -C_{ox}\left(V_G' - V_T'\right)$$



$$W_T = \left[\frac{2K_S\varepsilon_0}{qN_A}2\phi_F\right]^{1/2}$$

MOS capacitor

1) Gate voltage
2) **Example problem**
3) MOS capacitors
4) MOS field-effect transistors



‘metal’/
heavily doped
polysilicon

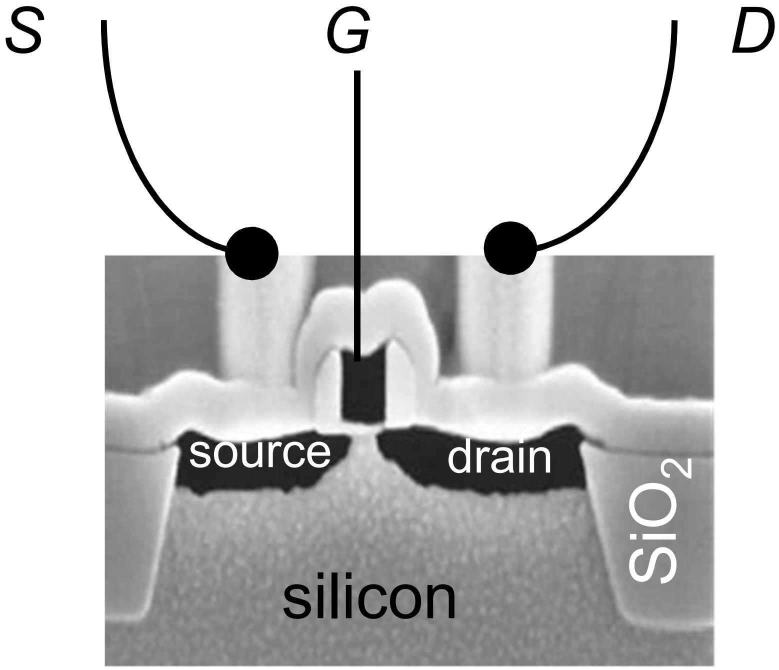
SiO_2

$t_{ox} \approx 1-2$ nm

example

Assume n+ poly Si gate
10^{18} channel doping
t_{ox} = 1.5 nm

What is V_T?
e-field in oxide at V_G = 1V?



MOS capacitor

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3) **MOS capacitors**
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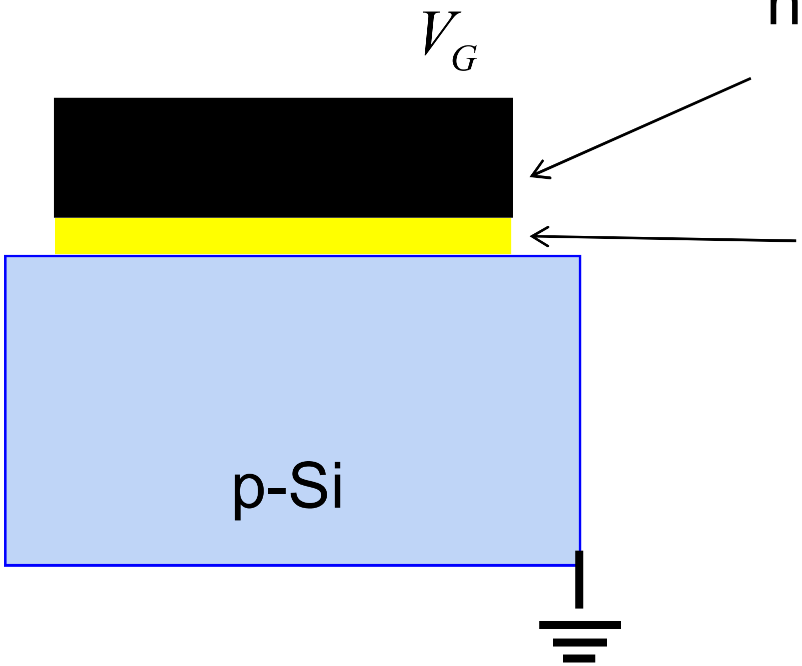
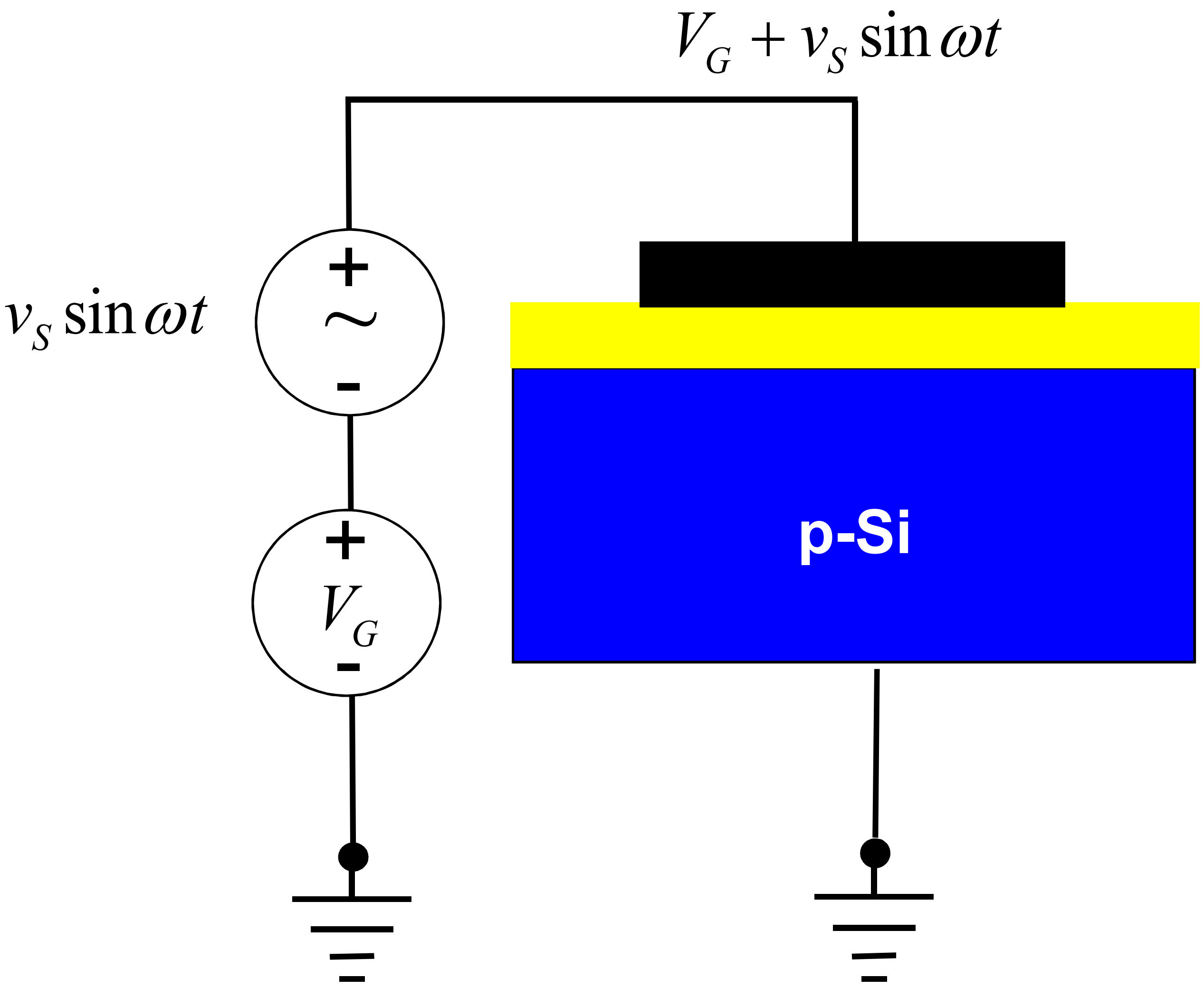


'metal'/
heavily doped
polysilicon

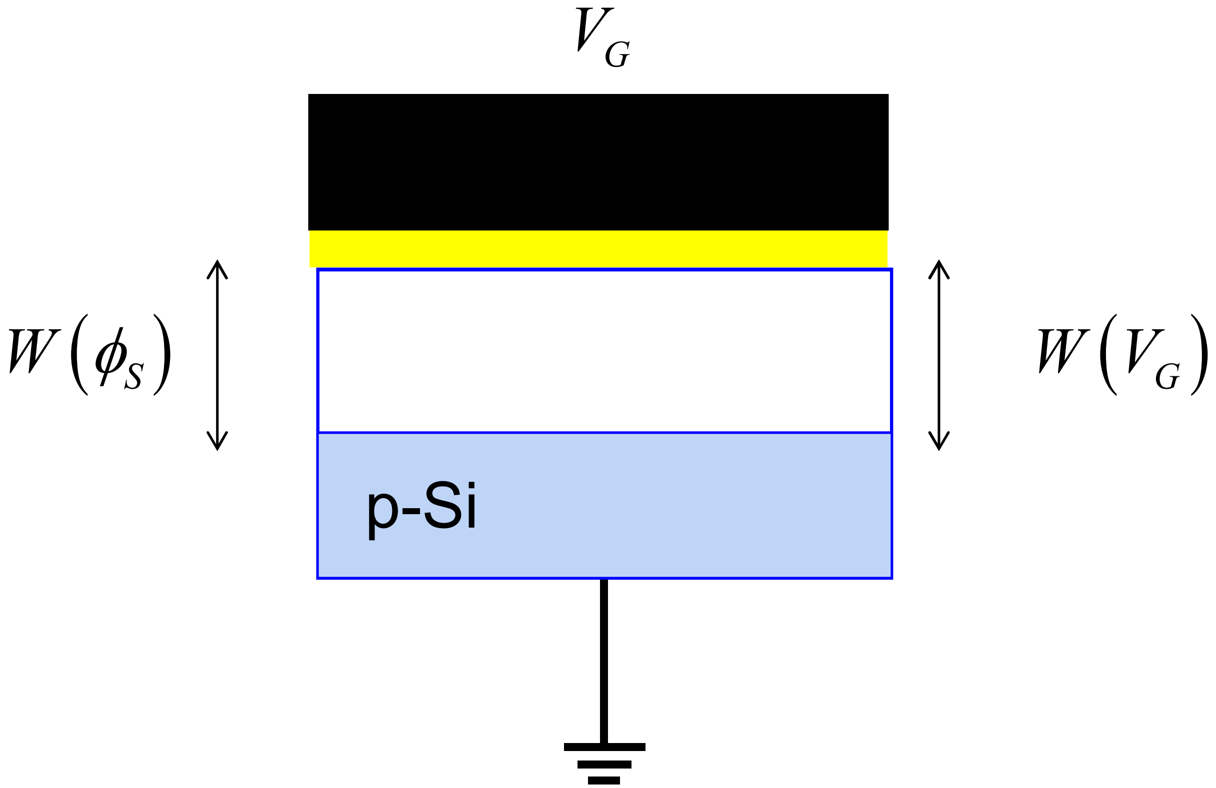
SiO_2

$t_{ox} \approx 1 - 2\ \text{nm}$

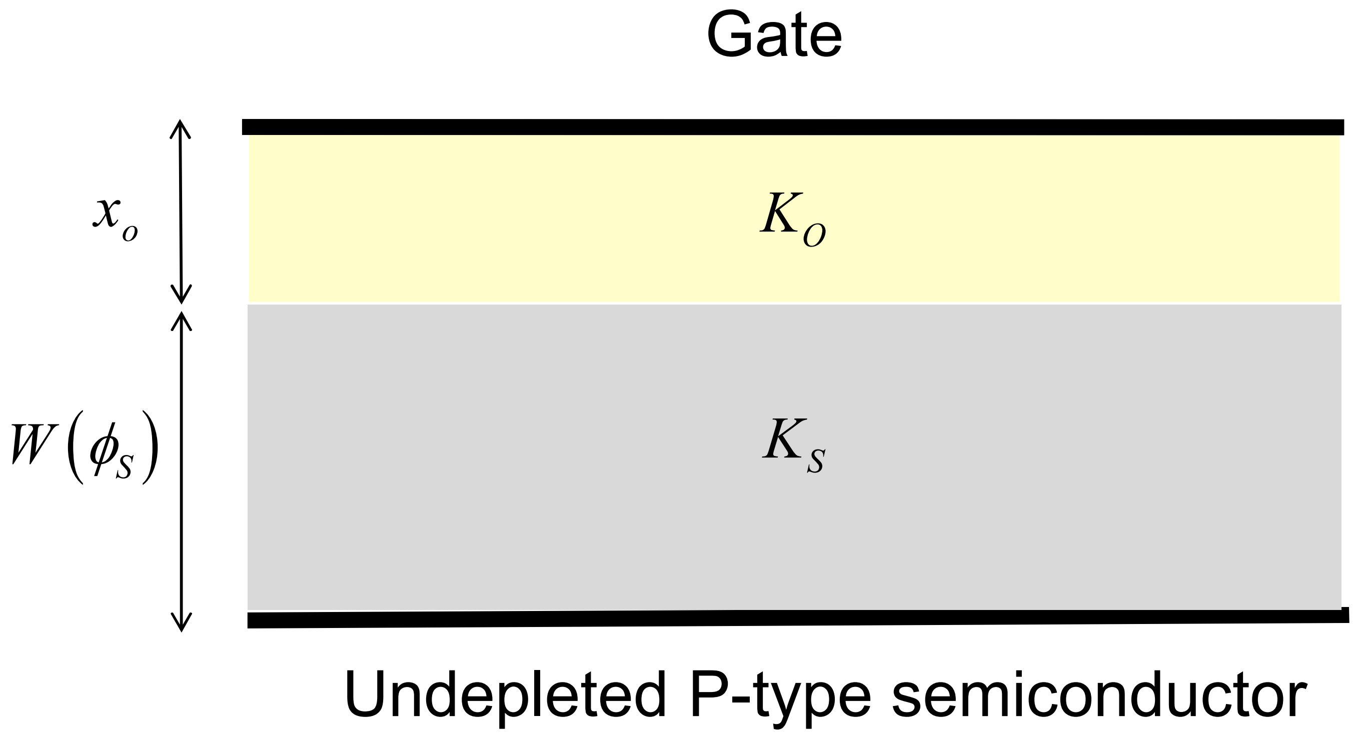
MOS capacitor



MOS capacitor in depletion

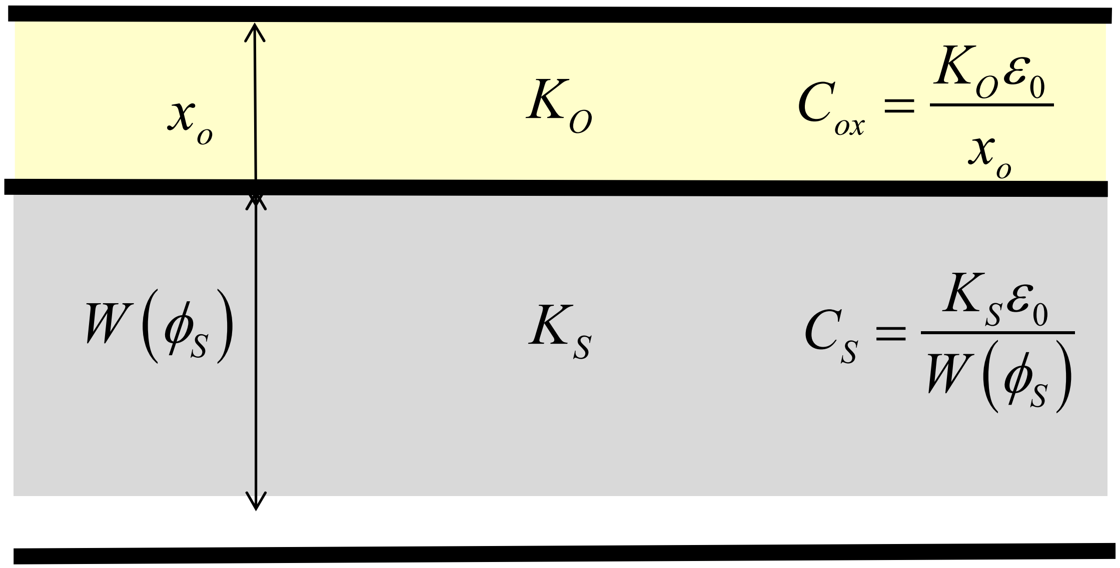


MOS capacitor in depletion



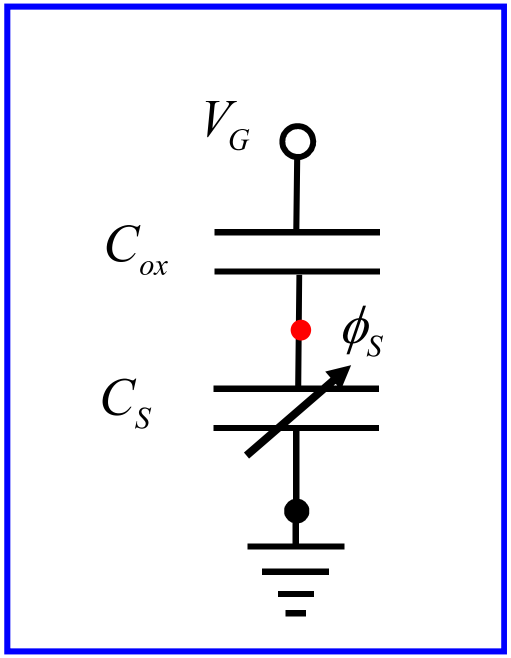
$C = ?$

a simpler problem



$$C_{ox} = \frac{K_O \varepsilon_0}{x_o}$$

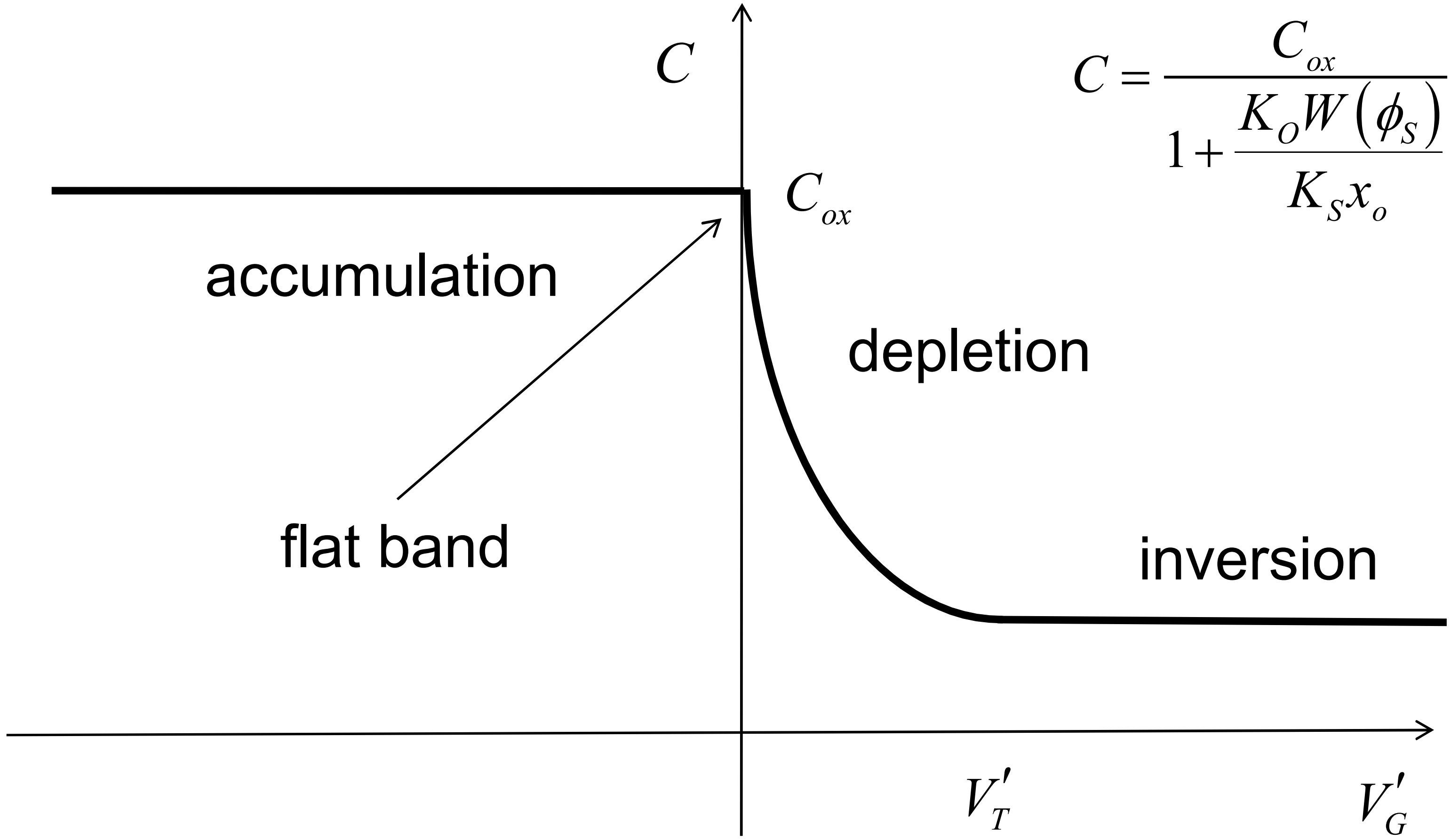
$$C_S = \frac{K_S \varepsilon_0}{W(\phi_S)}$$



$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_S} \qquad C = \frac{C_S C_{ox}}{C_S + C_{ox}} \qquad C = \frac{C_{ox}}{1 + C_{ox}/C_S}$$

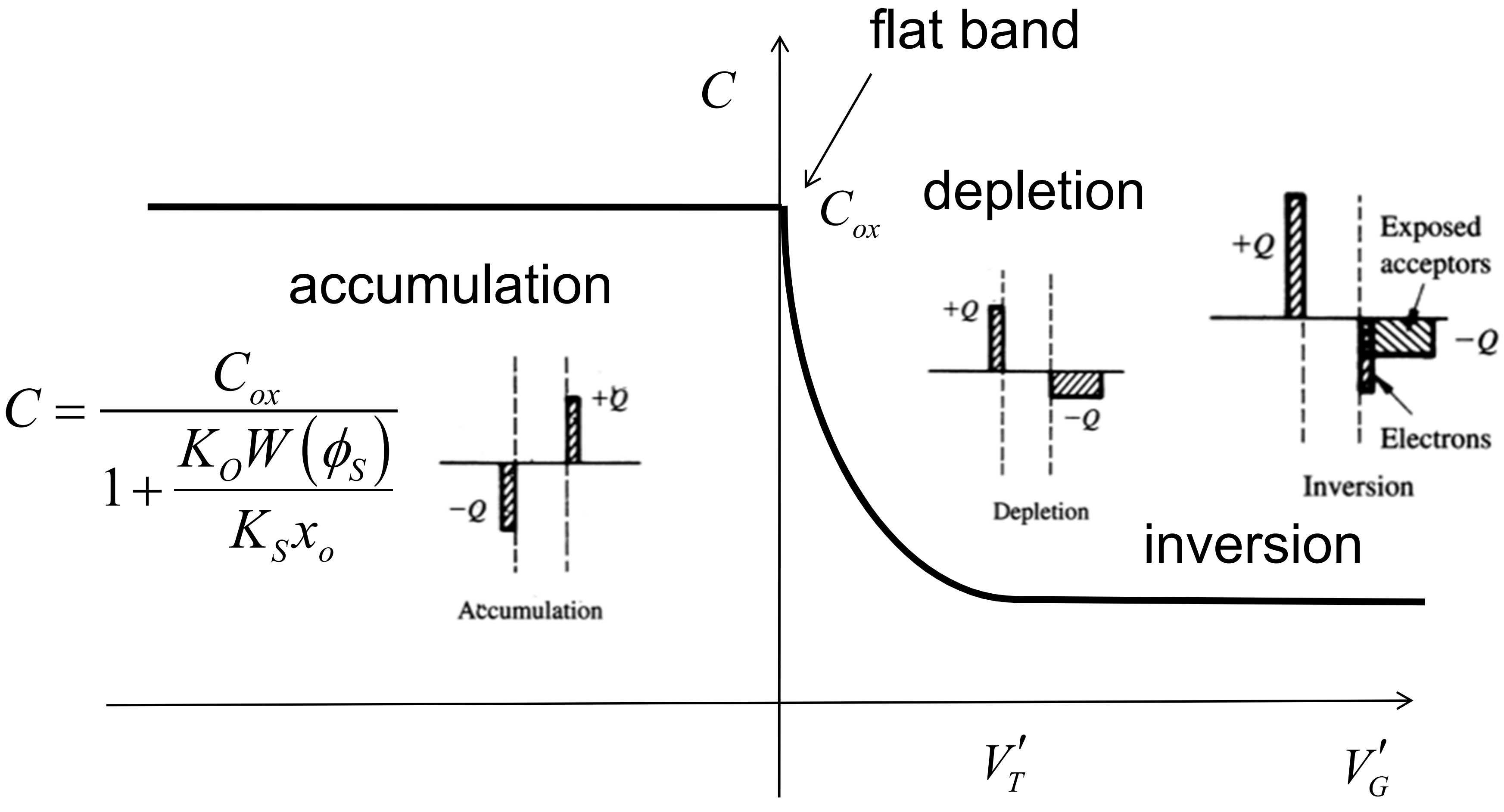
$$\boxed{C = \frac{C_{ox}}{1 + \dfrac{K_O W(\phi_S)}{K_S x_o}}}$$

s.s. gate capacitance vs. d.c. gate bias



$$C = \frac{C_{ox}}{1 + \dfrac{K_O W\left(\phi_S\right)}{K_S x_o}}$$

s.s. gate capacitance vs. d.c. gate bias



flat band

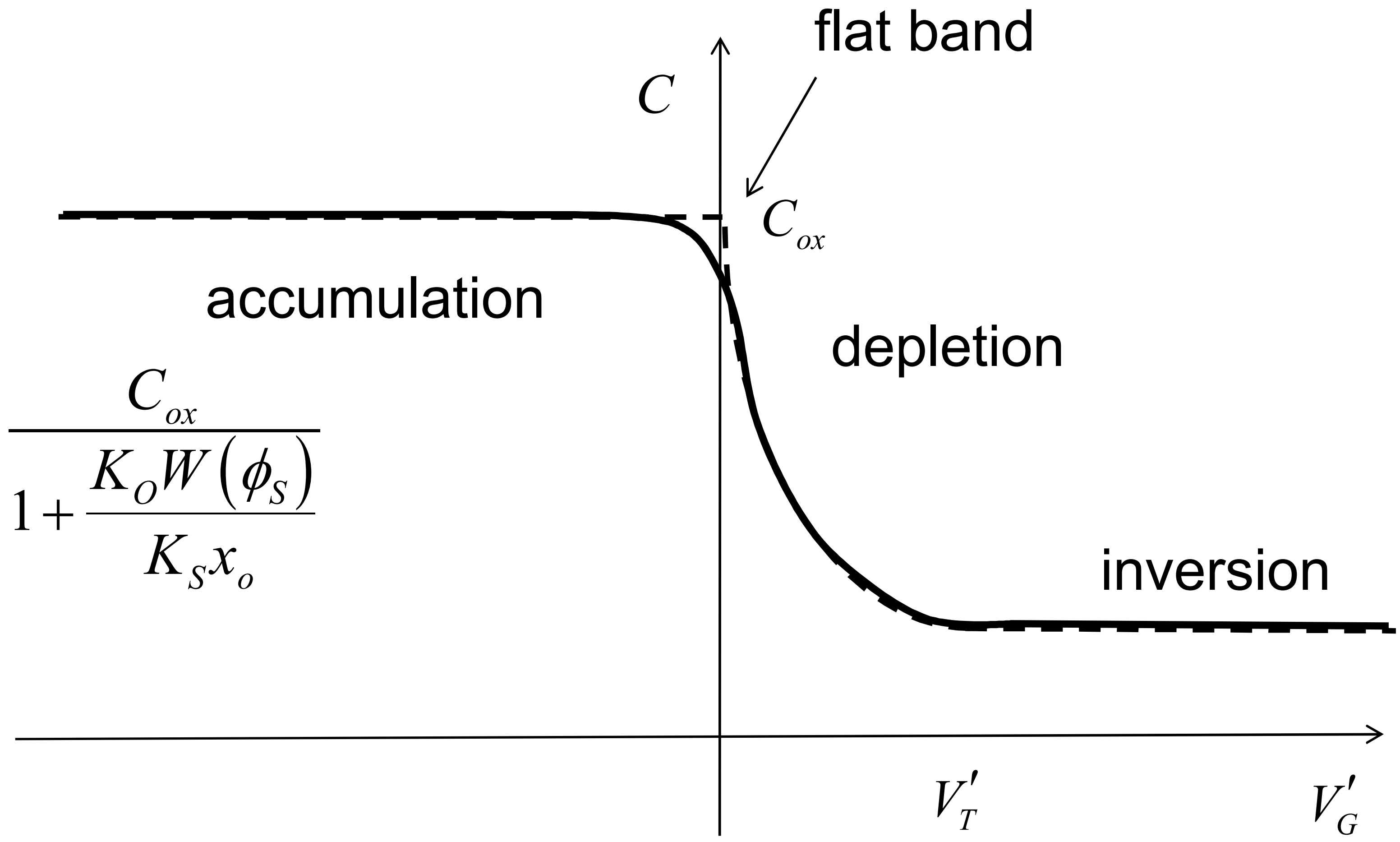
depletion

accumulation

inversion

$$C = \frac{C_{ox}}{1 + \frac{K_O W(\phi_S)}{K_S x_o}}$$

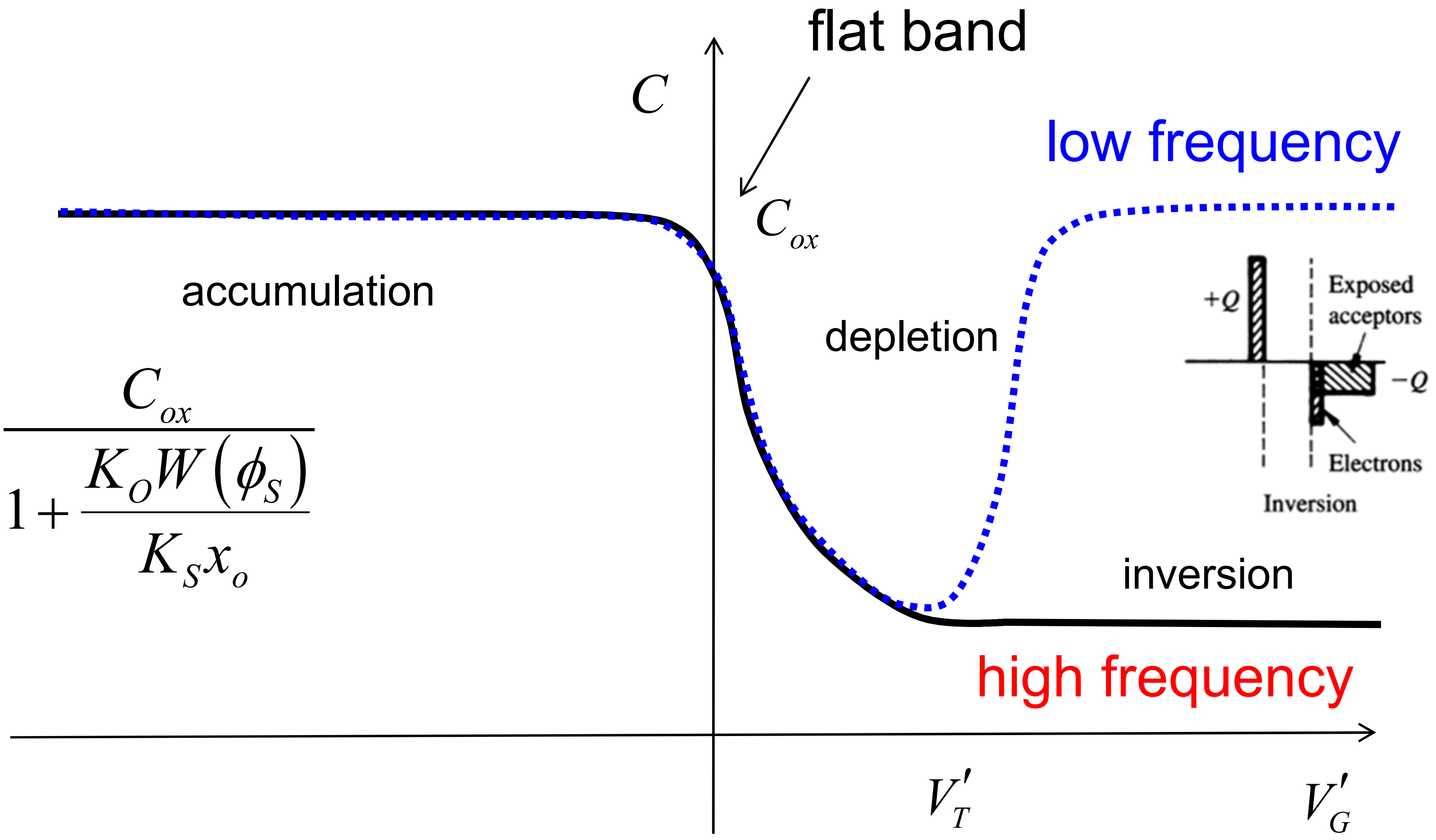
capacitance vs. gate voltage



$$C = \frac{C_{ox}}{1 + \dfrac{K_O W(\phi_S)}{K_S x_o}}$$

high frequency vs. low frequency

$$C = \frac{C_{ox}}{1 + \dfrac{K_O W\left(\phi_S\right)}{K_S x_o}}$$



MOS capacitor

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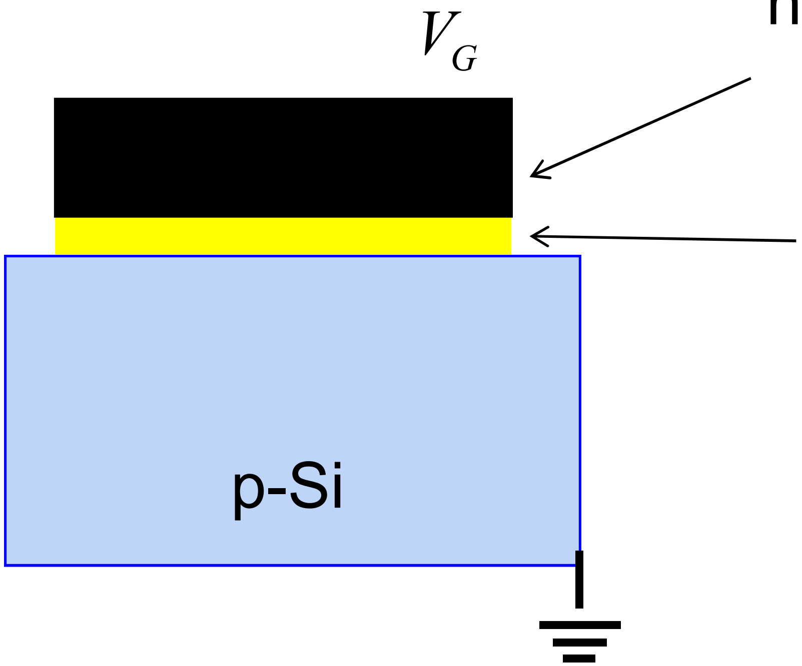
4) **MOS field-effect transistors**



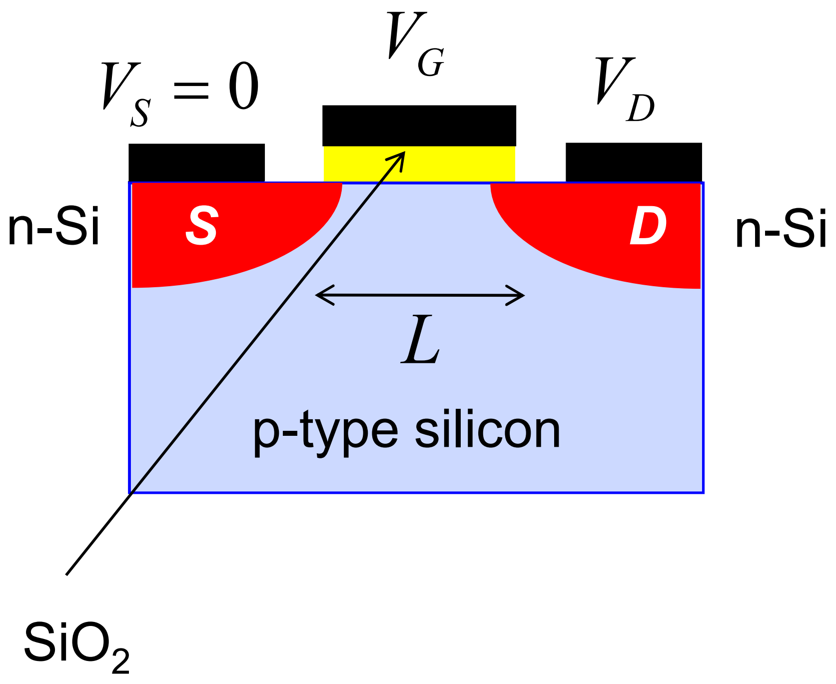
'metal'/ heavily doped polysilicon

SiO_2

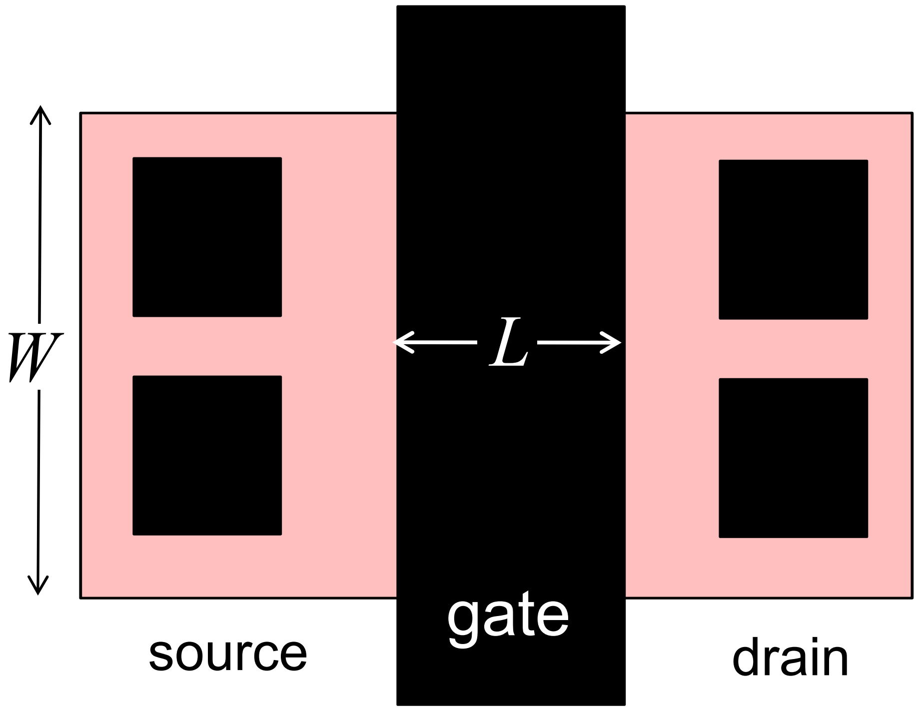
$t_{ox} \approx 1-2$ nm

side and top views of a **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor (MOSFET)

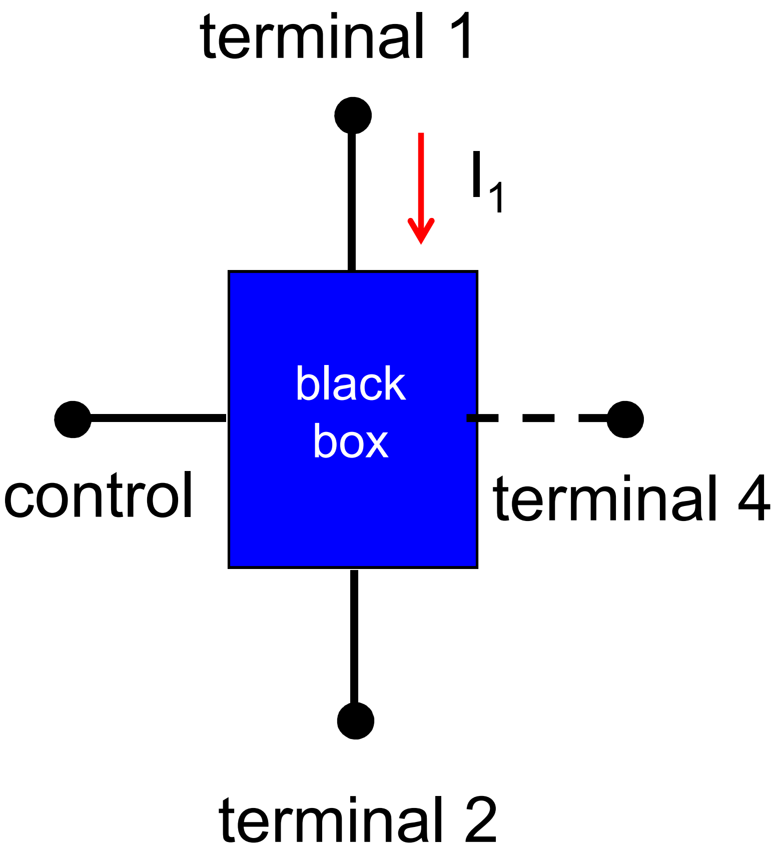
side view



top view



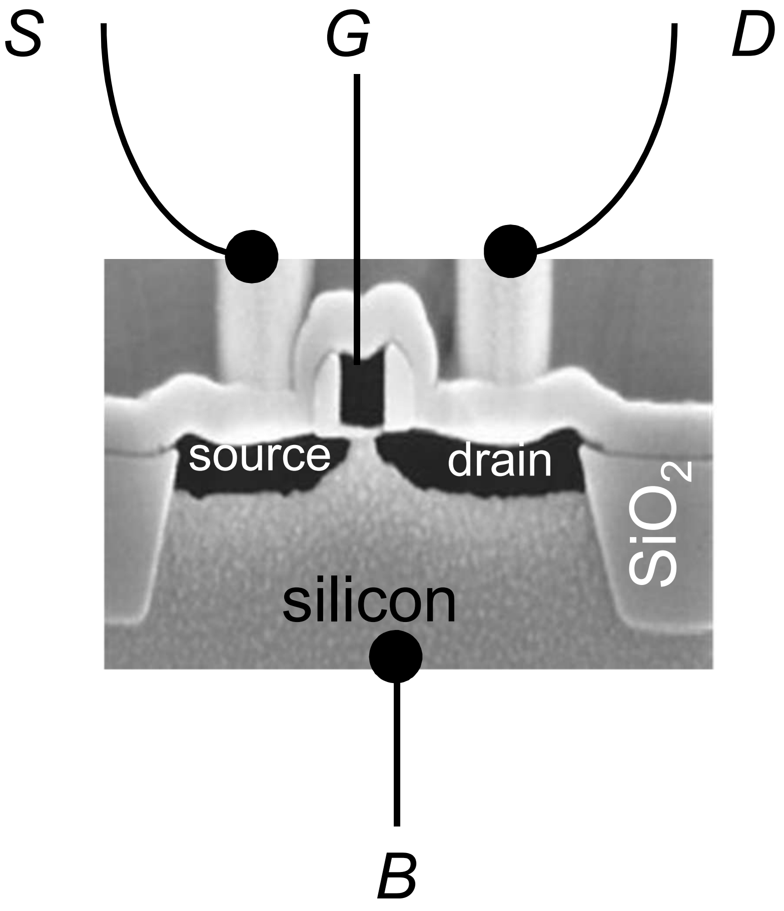
transistor as a “black box”



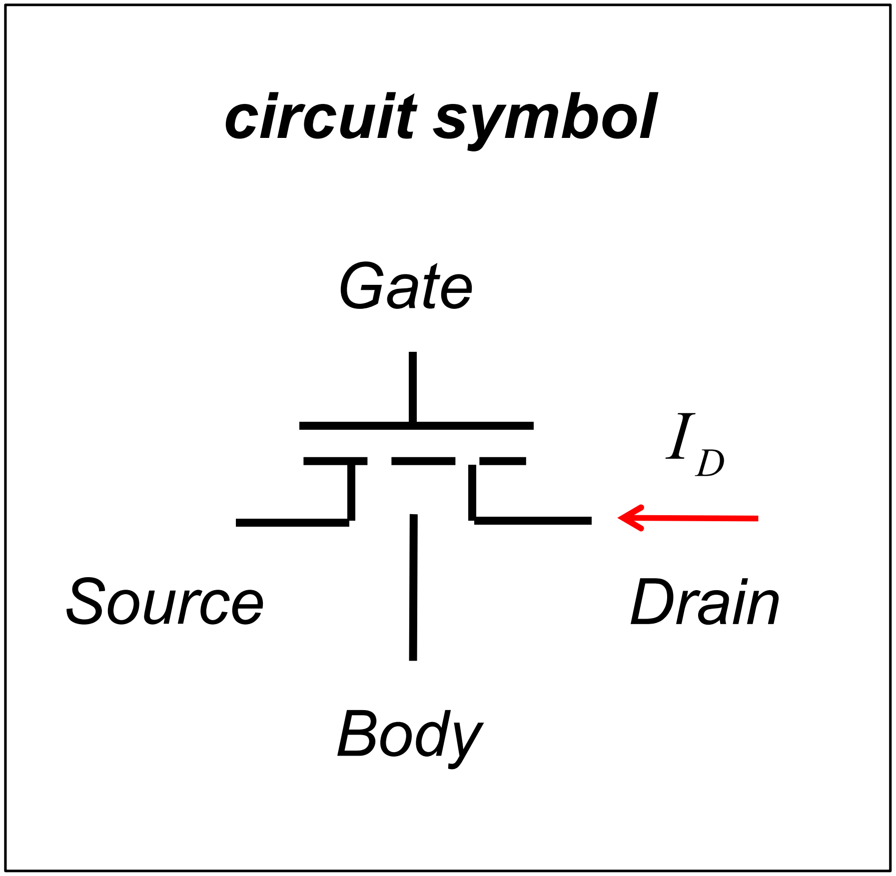
There are many kinds of transistors:

MOSFET
SOI MOSFET
SB FET
FinFET
MODFET (HEMT)
bipolar transistor
JFET
heterojunction bipolar transistor
BTBT FET
SpinFET
…

the bulk MOSFET

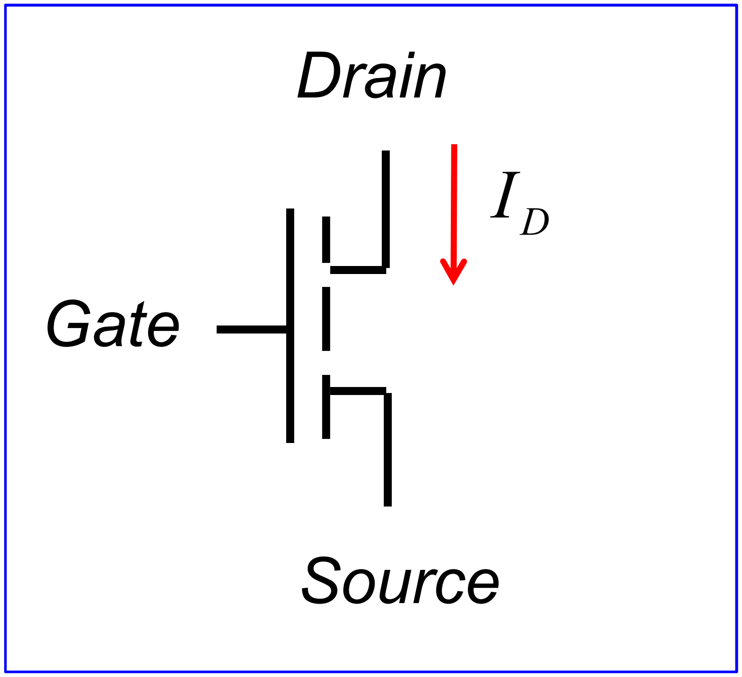


(Texas Instruments, ~ 2000)

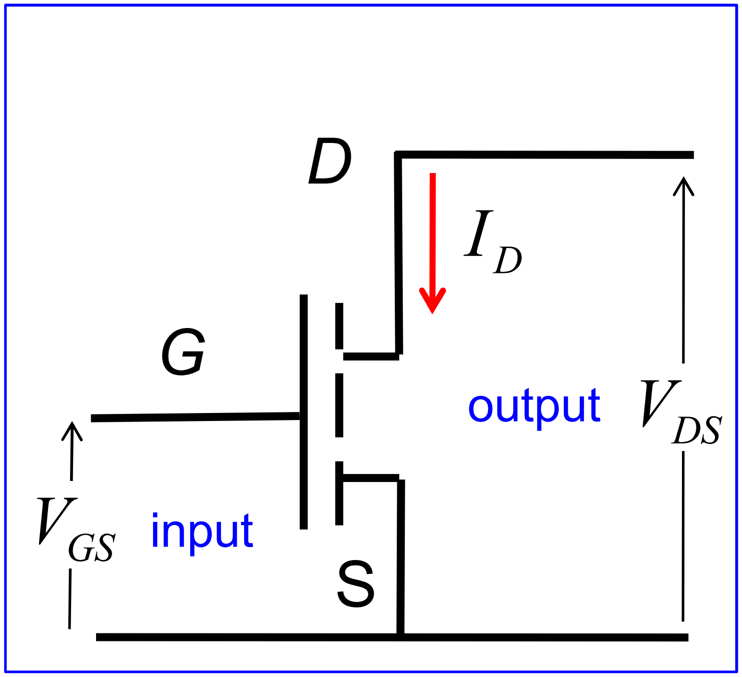

circuit symbol

the MOSFET as a 2-port device

MOSFET circuit symbol



common source



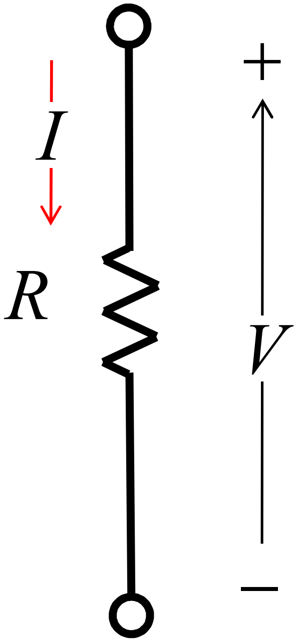
current vs. voltage (IV) characteristics

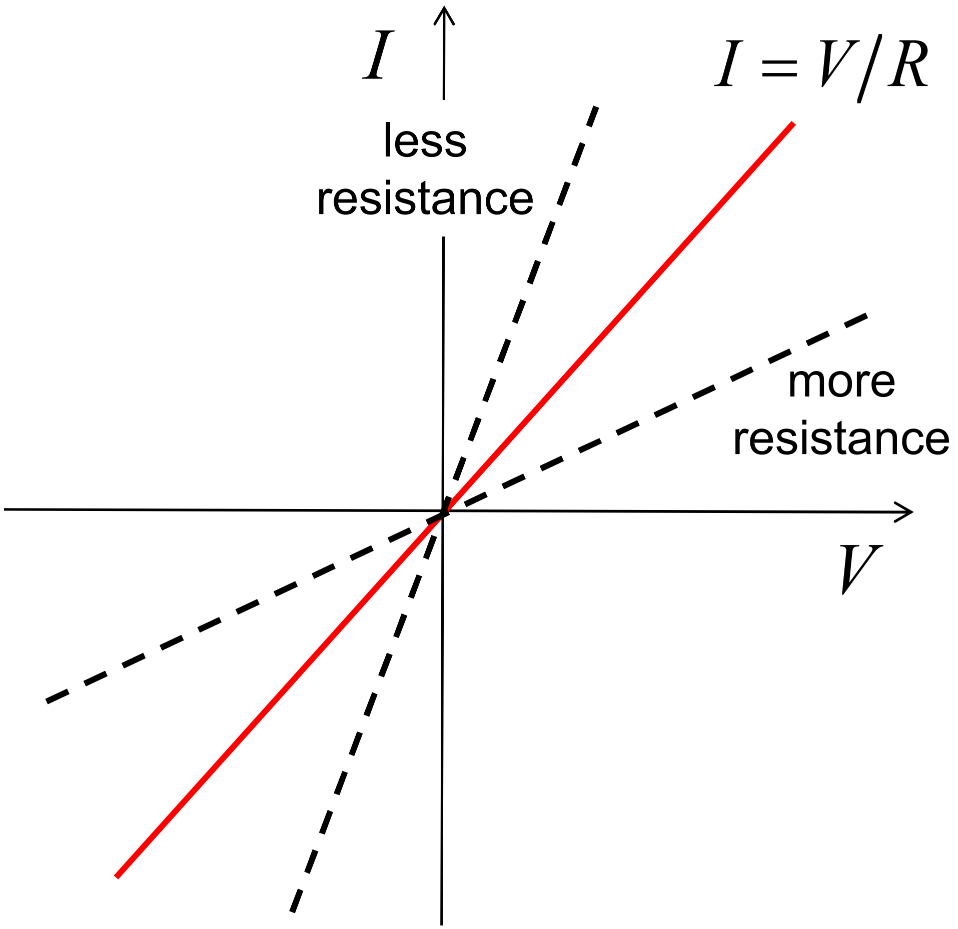
$$I_D\left(V_G, V_S, V_D\right)$$

$I_D\left(V_{GS}\right)$ at a fixed V_{DS} transfer

$I_D\left(V_{DS}\right)$ at a fixed V_{GS} output

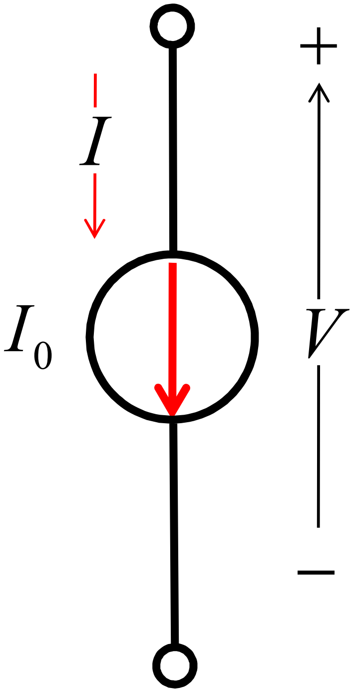
IV characteristics: resistor



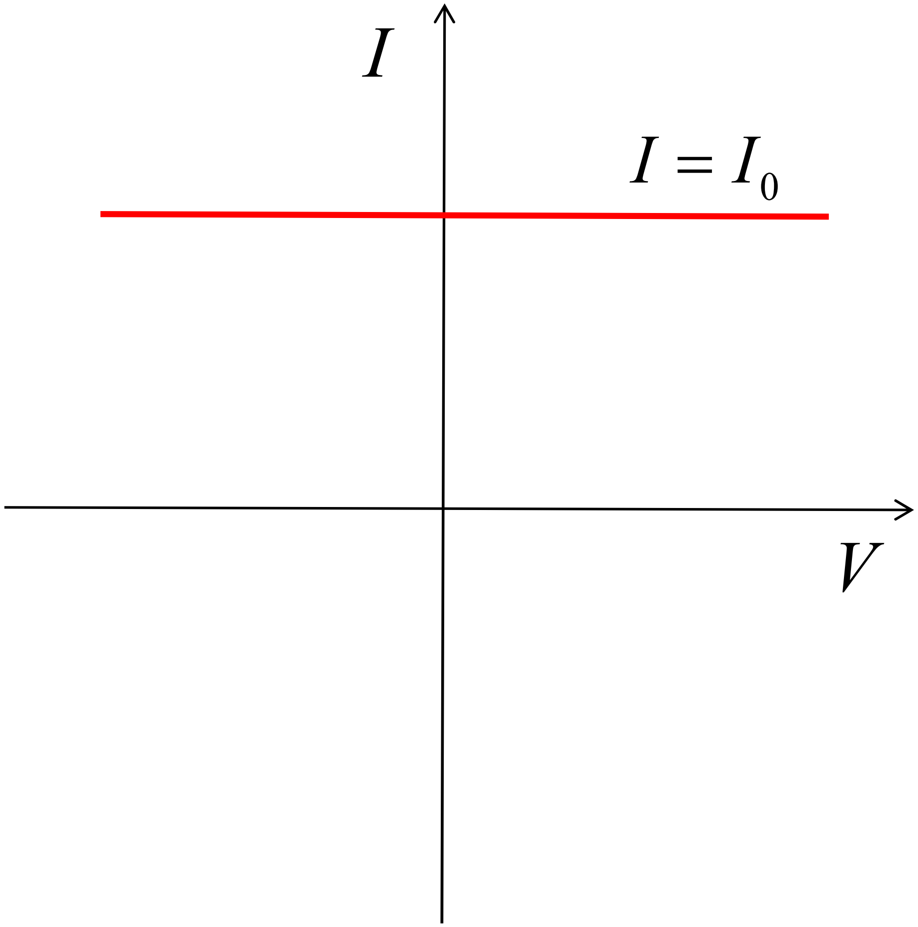


$I = V/R$ Ohm's Law

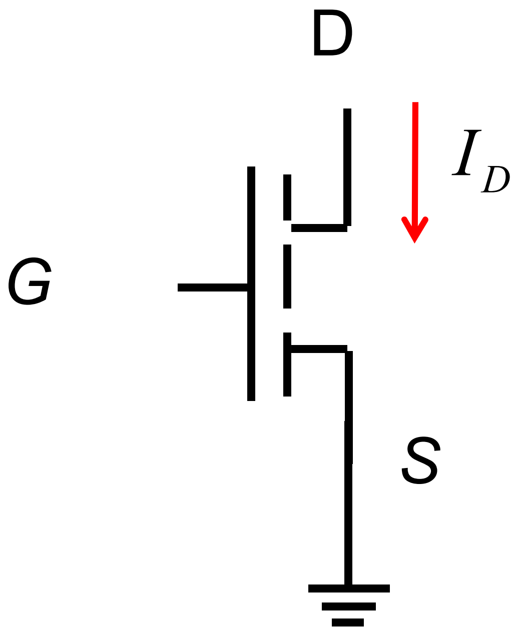
IV characteristics: ideal current source



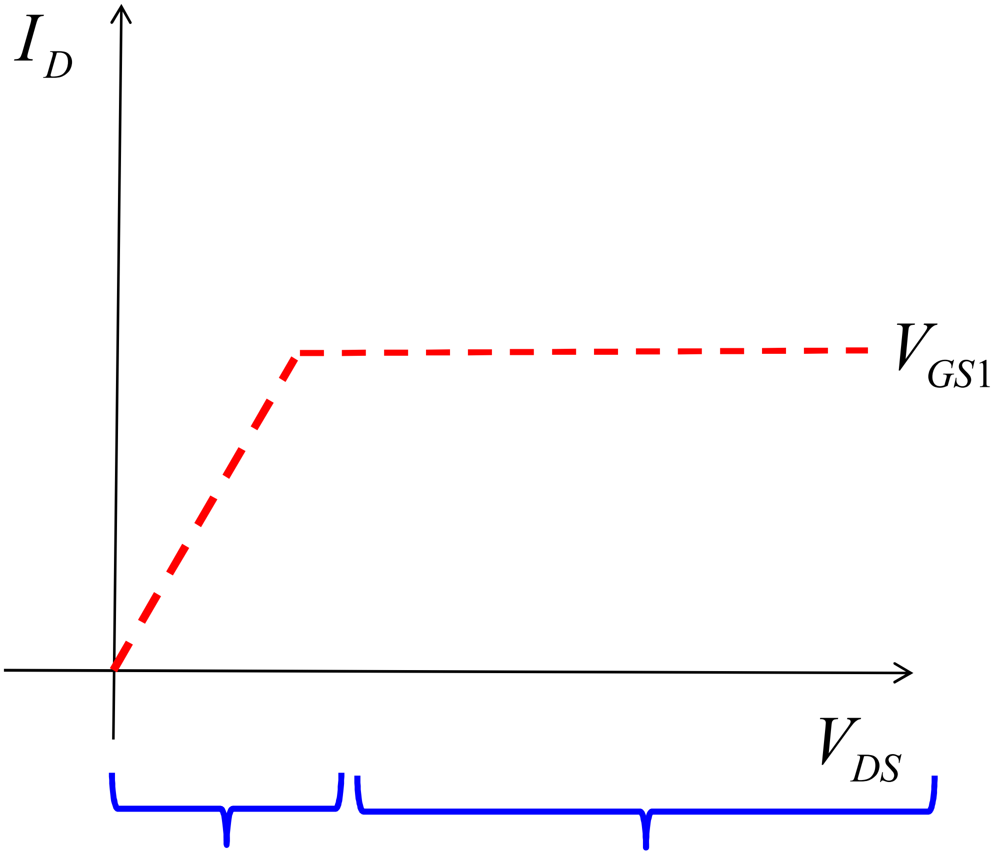
$$I = I_0$$



IV characteristics: transistors



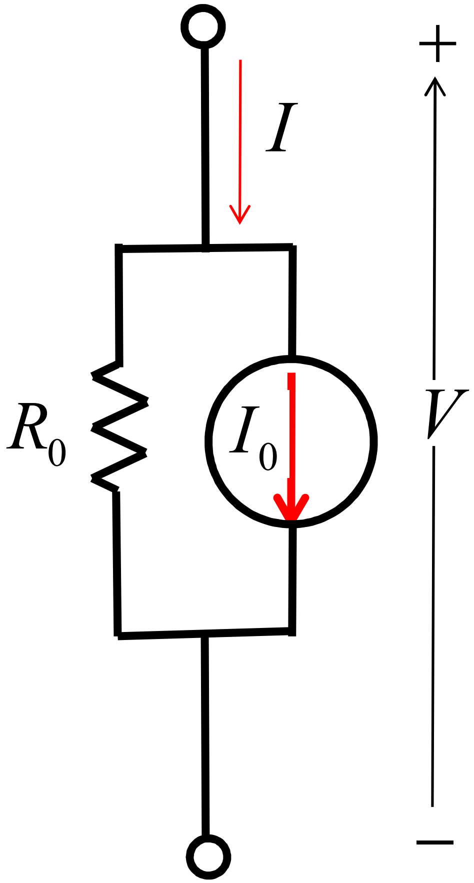
n-channel
enhancement
mode MOSFET

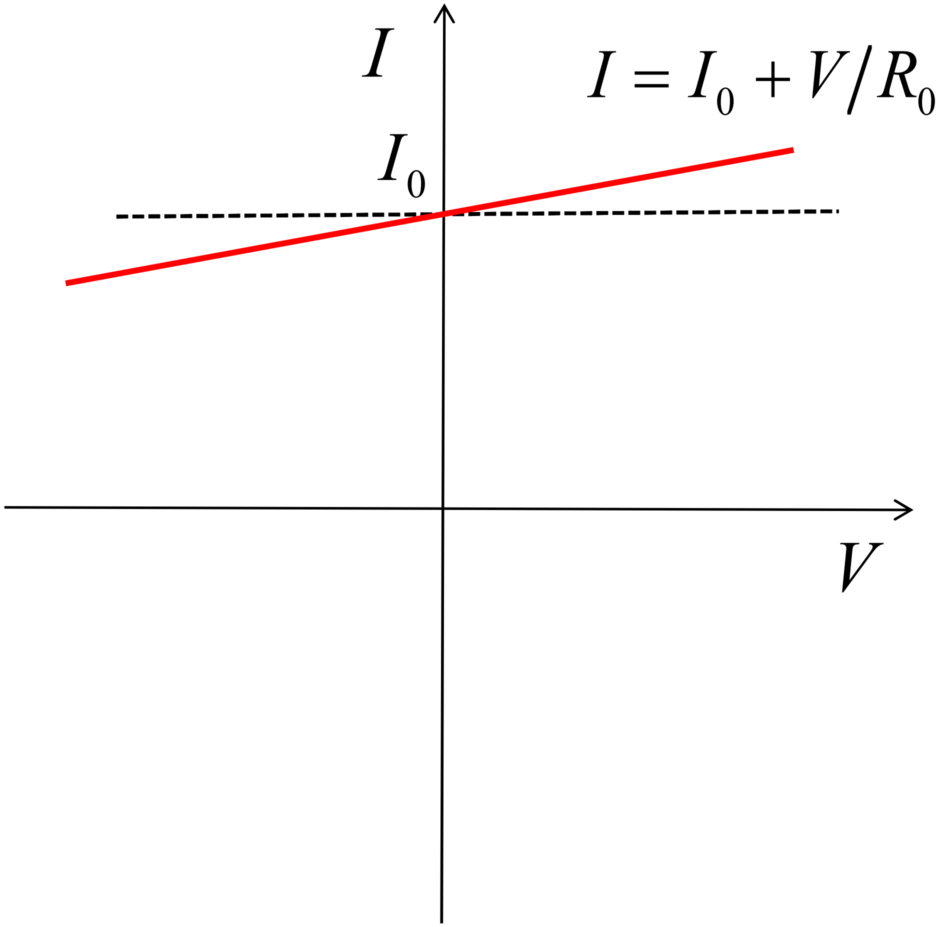


gate voltage
controlled resistor
“linear region”

gate voltage controlled
current source
“saturation region”

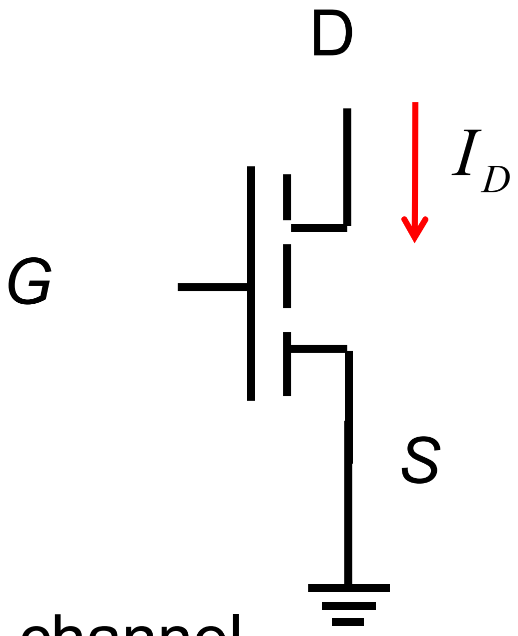
IV characteristics: real current sources



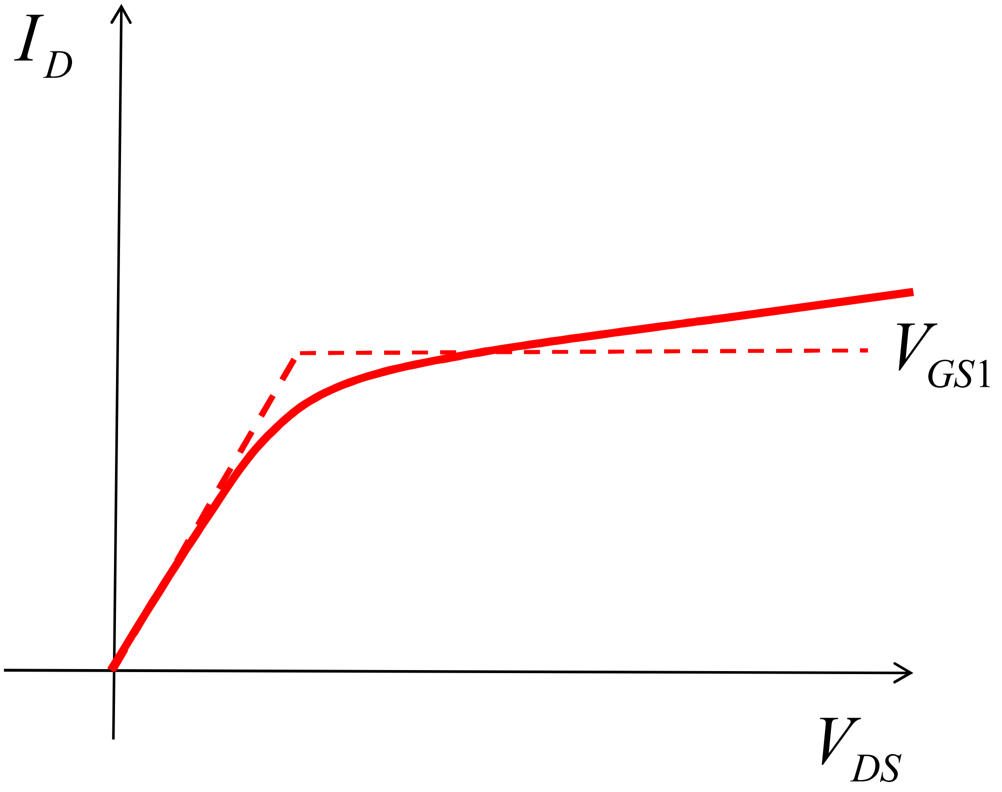


$$I = I_0 + V/R_0$$

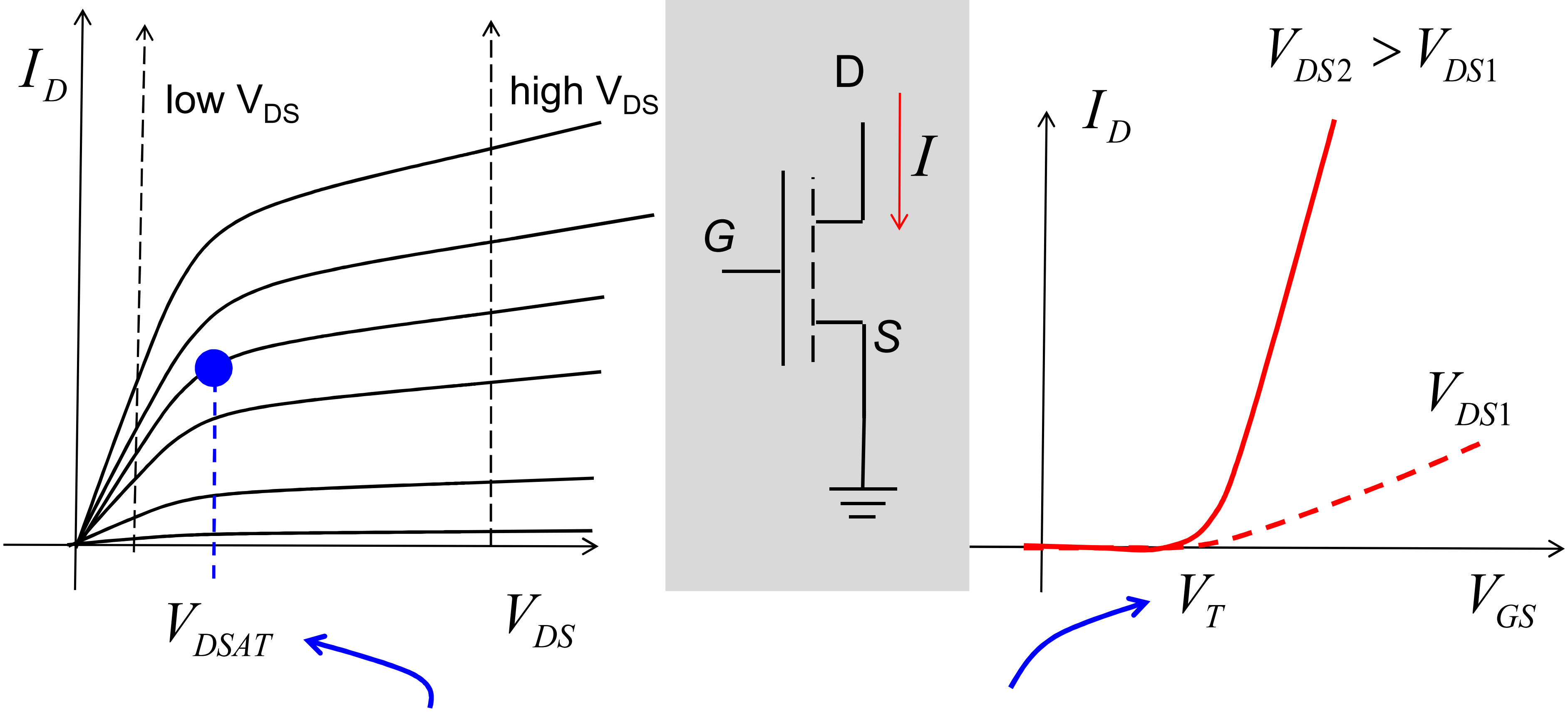
IV characteristics: transistors



n-channel enhancement mode MOSFET



output vs. transfer characteristics



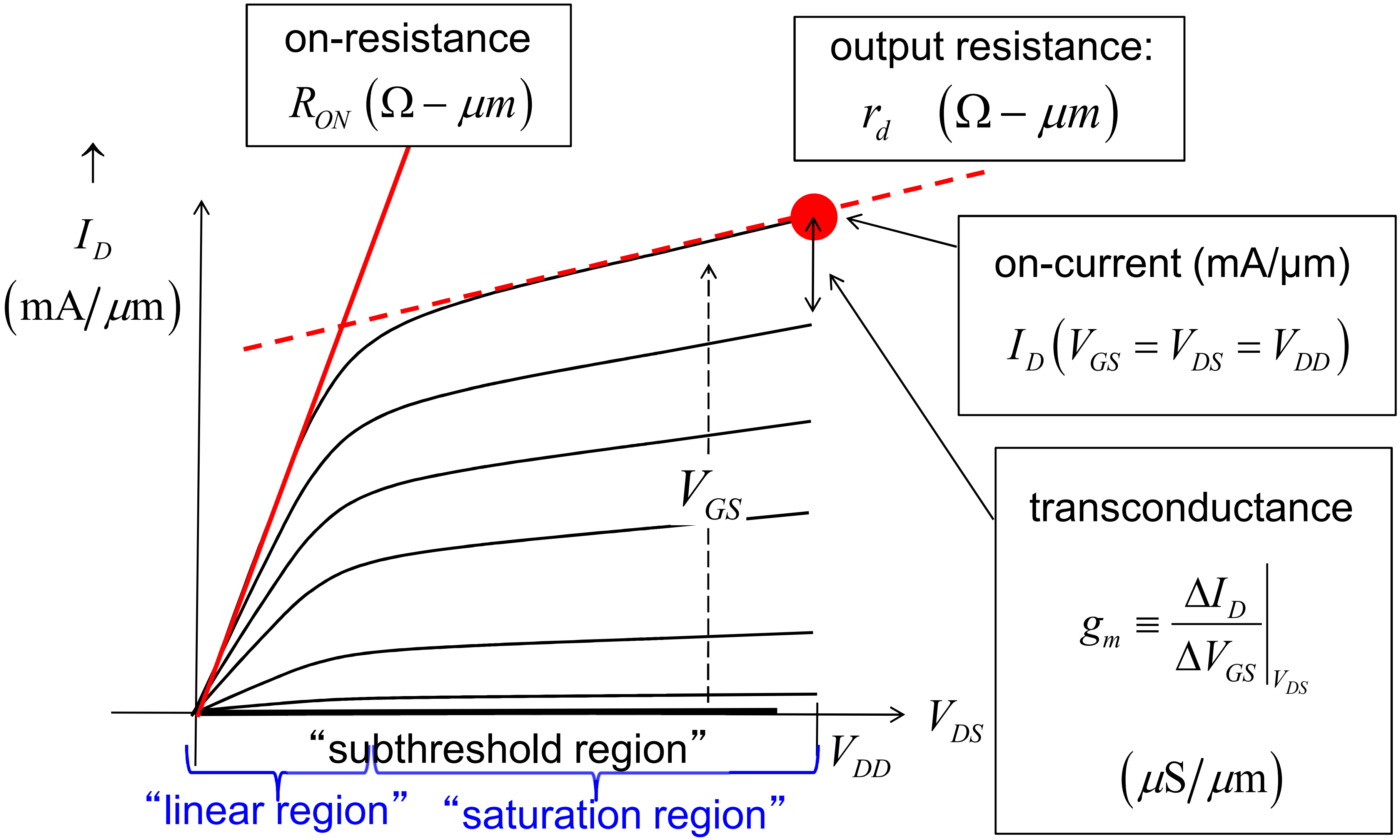
output characteristics

transfer characteristics

“saturation voltage”

“threshold voltage”

MOSFET output characteristics
n-channel, enhancement mode (E-mode)



on-resistance

$R_{ON}\ (\Omega - \mu m)$

output resistance:

$r_d\ \ (\Omega - \mu m)$

on-current (mA/μm)

$I_D\left(V_{GS} = V_{DS} = V_{DD}\right)$

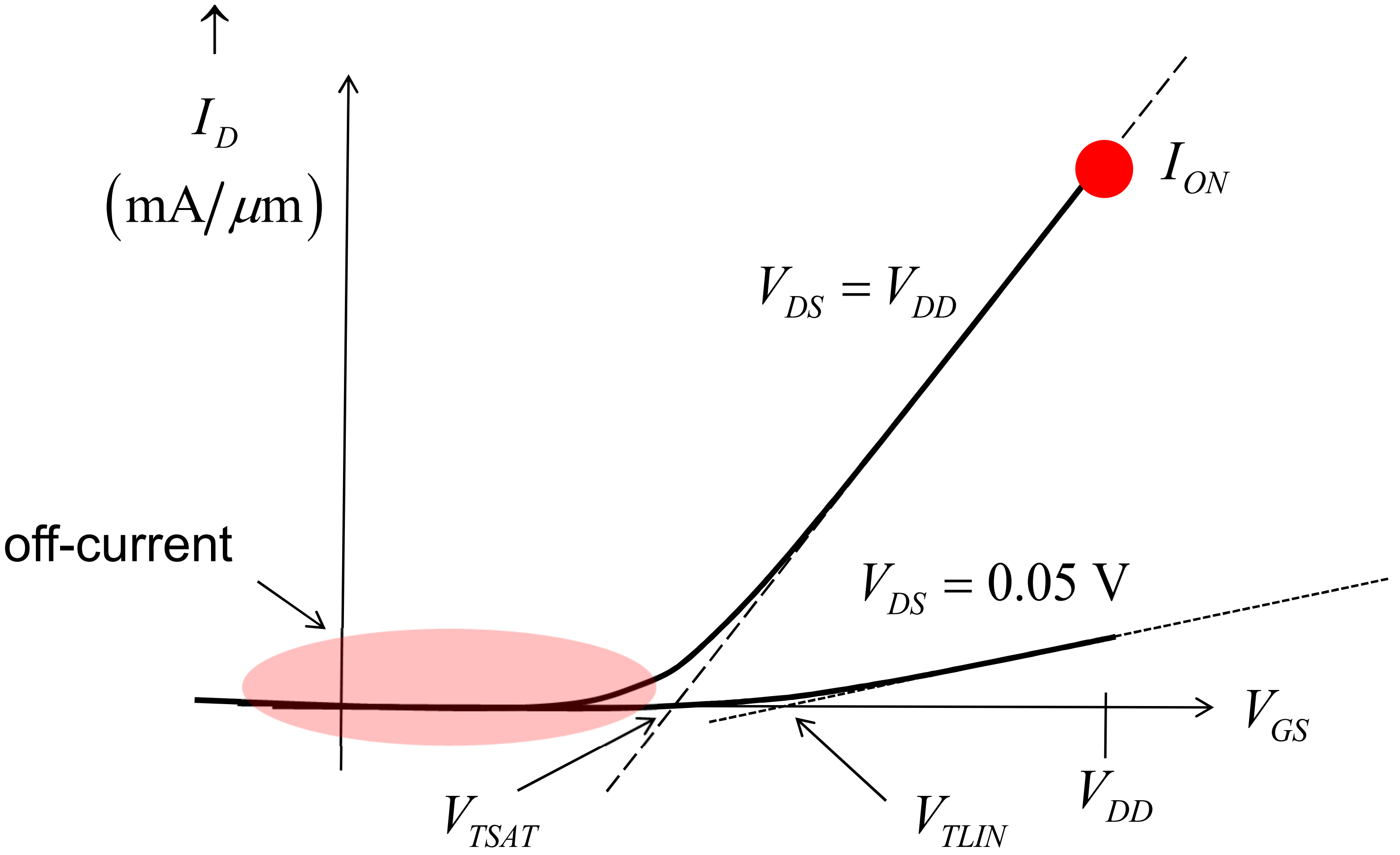
transconductance

$$g_m \equiv \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}}$$

$(\mu\mathrm{S}/\mu\mathrm{m})$

MOSFET device metrics (ii)

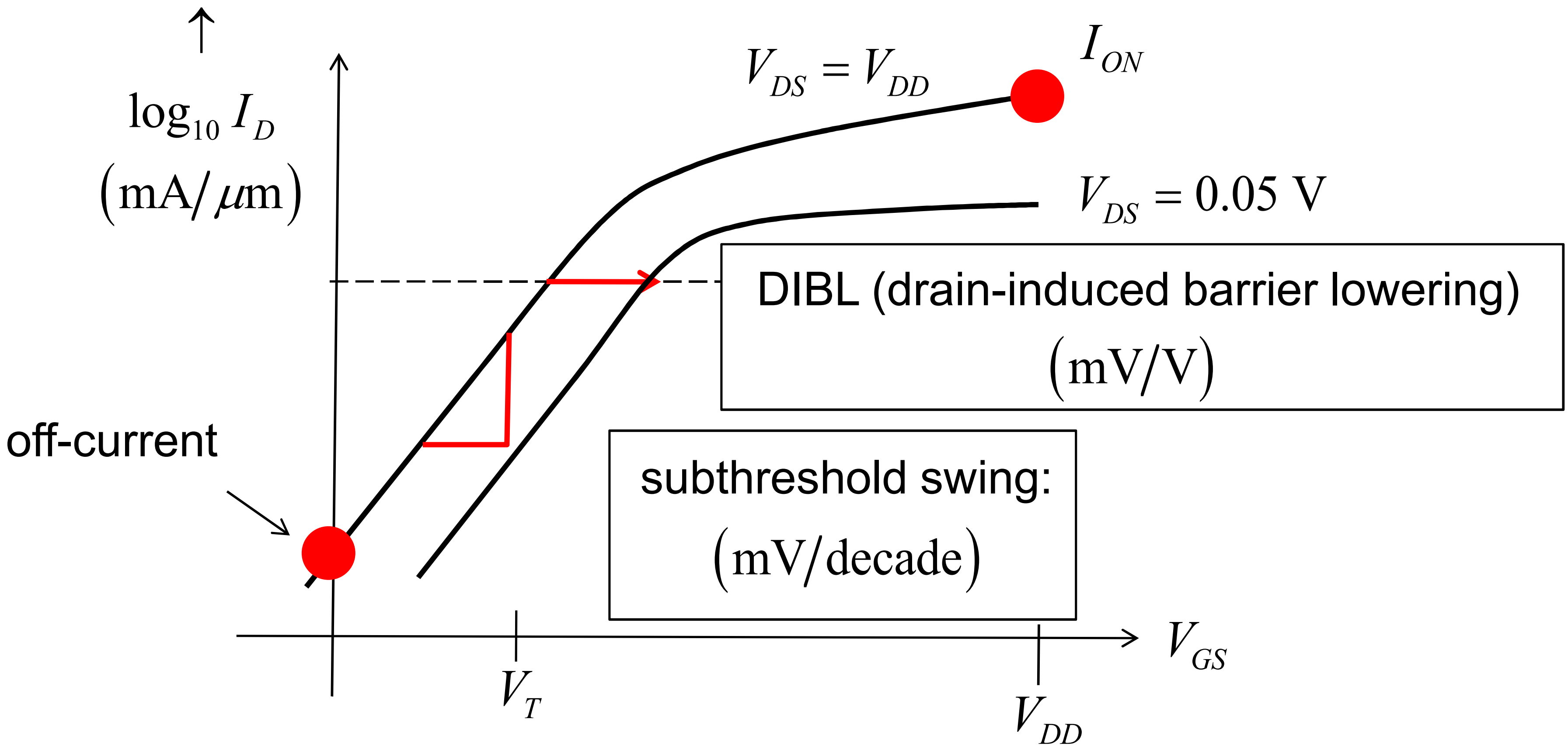
transfer characteristics:



threshold voltage

MOSFET device metrics (iii)

transfer characteristics:



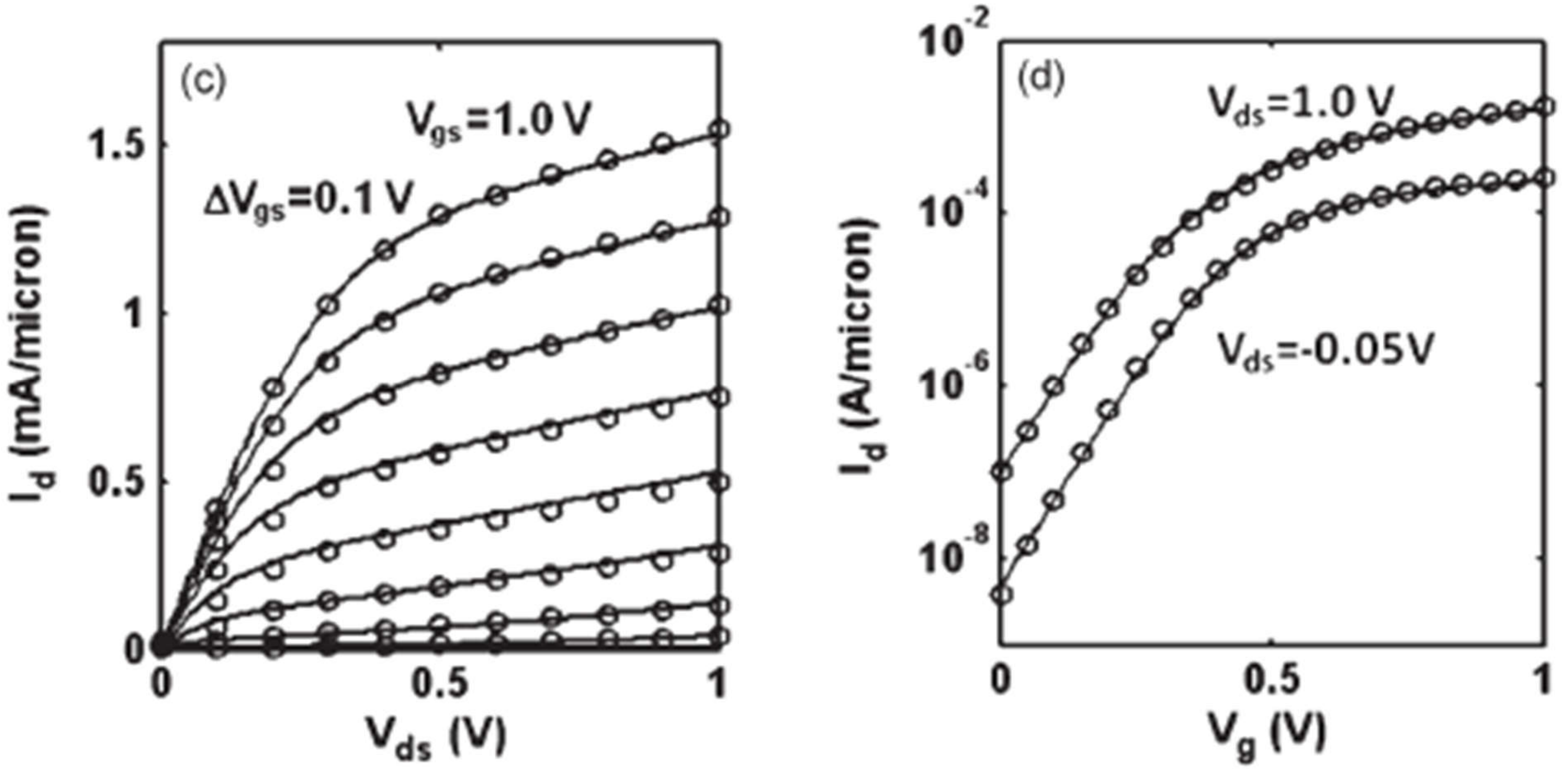
DIBL (drain-induced barrier lowering)

(mV/V)

subthreshold swing:

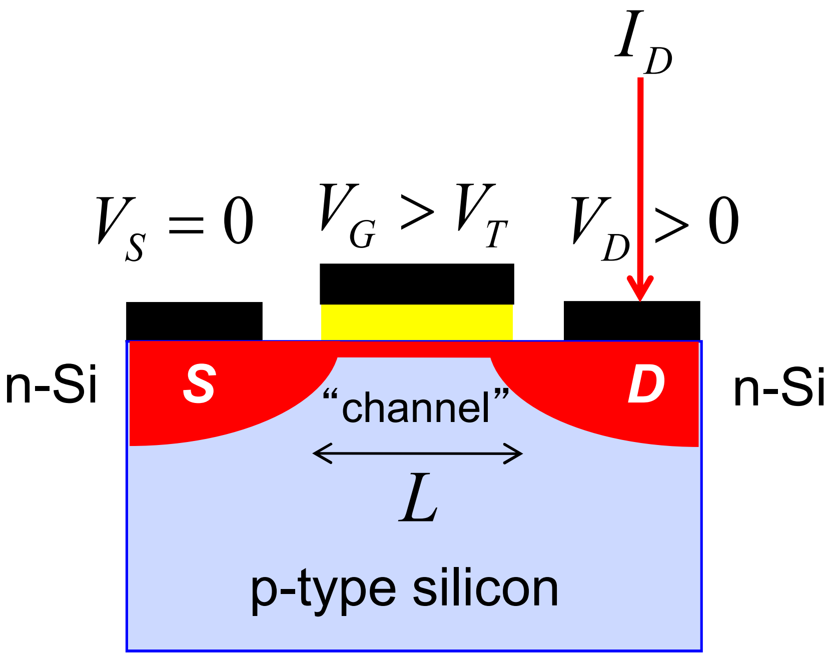
(mV/decade)

Example: 32 nm N-MOS technology



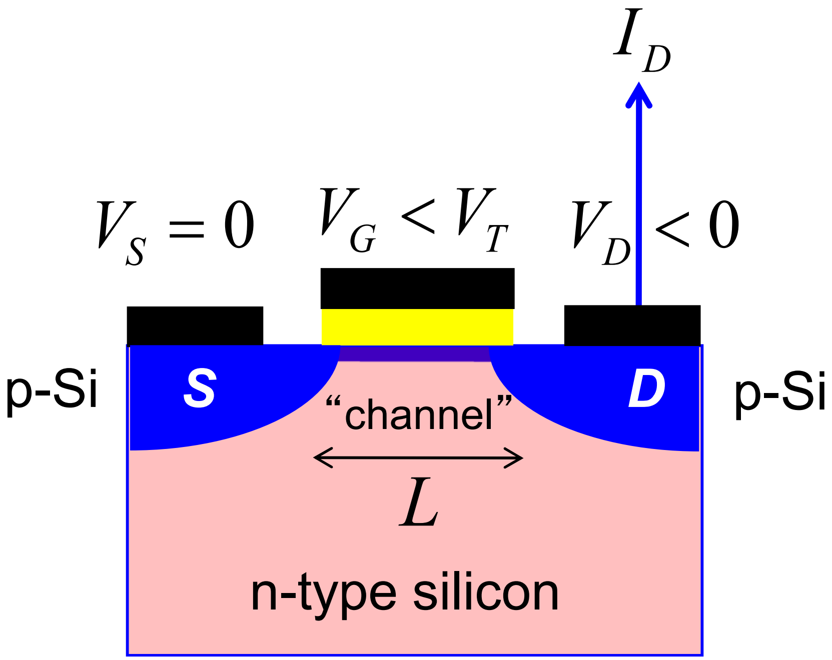
n-channel vs. p-channel MOSFET

n-MOSFET



side view

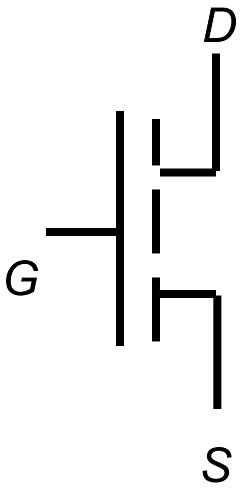
p-MOSFET

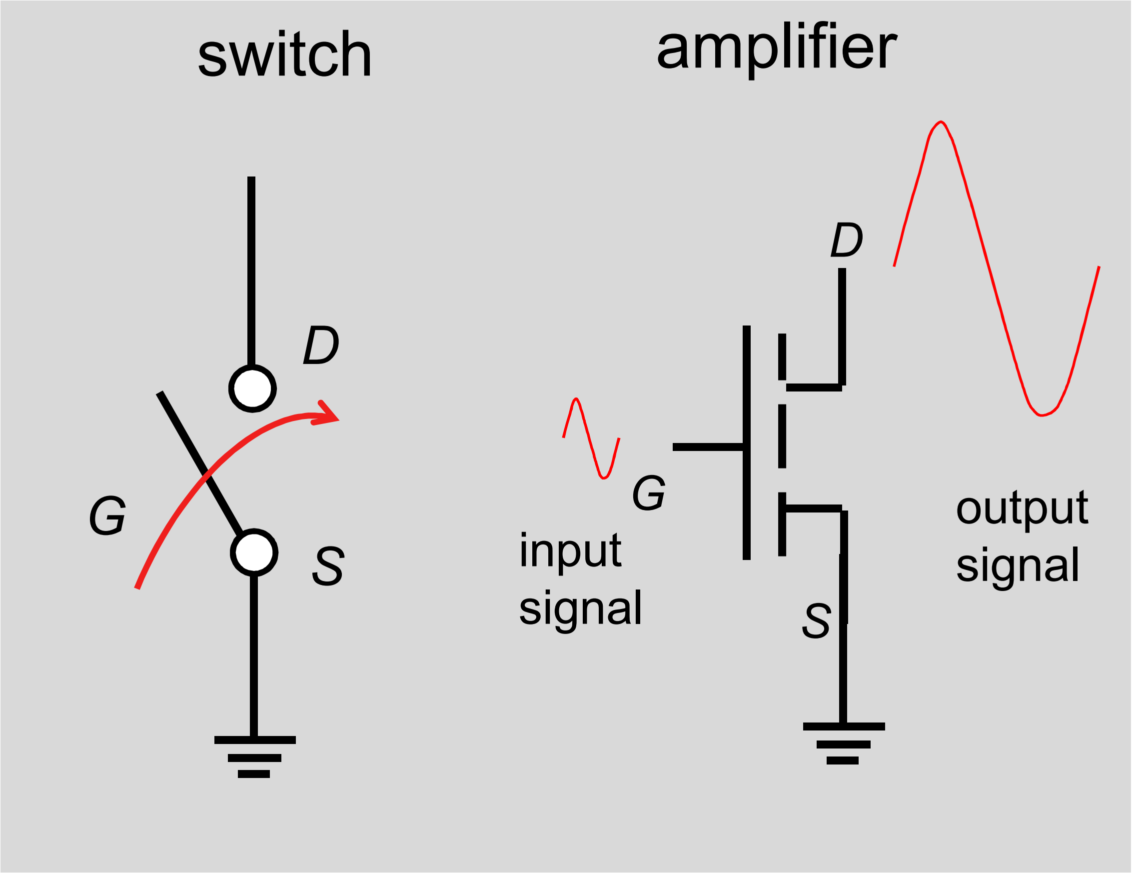


side view

applications of MOSFETs

symbol





summary

Given the measured characteristics of a MOSFET, you should be able to determine:

1. on-current: I_{ON}
2. off-current: I_{OFF}
3. subthreshold swing, S
4. drain induced barrier lowering: DIBL
5. threshold voltage: V_T (lin) and V_T (sat)
6. on resistance: R_{ON}
7. drain saturation voltage: V_{DSAT}
8. output resistance: r_o
9. *transconductance:* g_m

Our goal is to understand these device metrics.

conclusions

- Can calculate the charge distribution, surface potentials, and gate voltage ranges for each MOS regime
- Can then calculate capacitance as a function of frequency and gate voltage
- The MOS capacitor is the foundation for MOS field effect transistors, characterized by many device metrics
- Next time, we will use band structures to estimate the device metrics for MOSFETs