ECE-305: Spring 2018
MOS Field Effect Transistors (MOSFETs)

Pierret, *Semiconductor Device Fundamentals* (SDF)
Chapters 15+16 (pp. 525-530, 563-599)

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Outline

1. **Review from Tuesday**

2. Velocity saturation in simplified theory

3. Major Failure Modes

    A. Bulk charge theory for small transistors

    B. Bias Temperature Instability

    C. Short Channel Effects
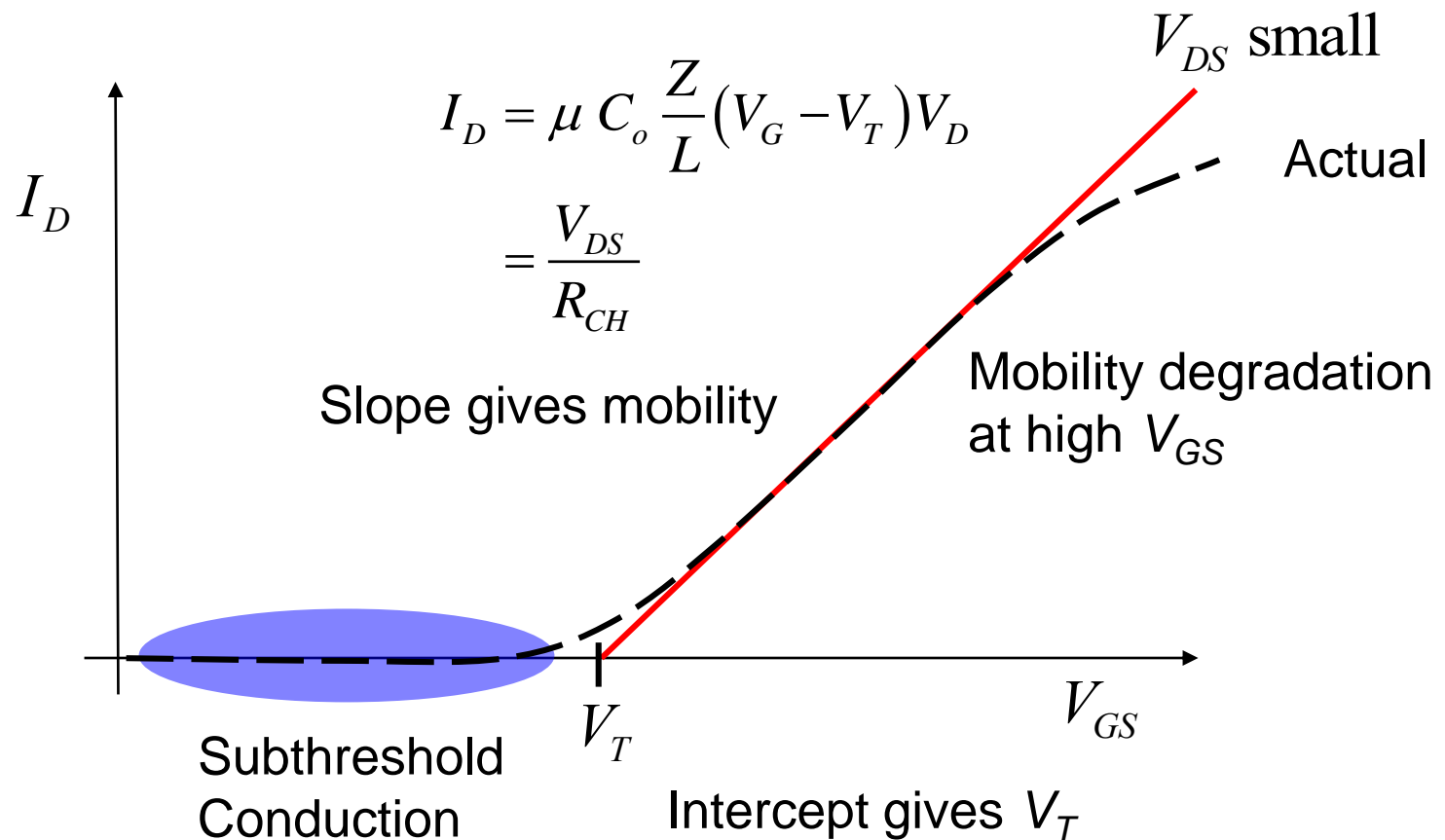
4. Conclusion

Approximations for Inversion Charge

$$Q_i = -C_o(V_G - V_T - V) + qN_A\left(W_T(V) - W_T(V=0)\right)$$

$$= -C_o(V_G - V_T - V) + \sqrt{2qk_S\varepsilon_o N_A\left(2\phi_B + V\right)} - \sqrt{2qk_S\varepsilon_o N_A\left(2\phi_B\right)}$$

Approximations:

$$Q_i \approx -C_o(V_G - V_T - V) \qquad \text{Square law approximation …}$$

$$Q_i \approx -C_o(V_G - V_T - mV) \qquad \text{Simplified bulk charge approximation …}$$

Linear Region (Low V_{DS})

$$I_D = \mu \, C_o \frac{Z}{L} \left(V_G - V_T \right) V_D$$

$$= \frac{V_{DS}}{R_{CH}}$$

V_{DS} small

Actual

Slope gives mobility

Mobility degradation at high V_{GS}

I_D

V_T

V_{GS}

Subthreshold Conduction

Intercept gives V_T

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Calculating V_{DSAT}

$$\upsilon_d = \frac{-\mu \mathcal{E}}{1 + \left(\left|\mathcal{E}\right|/\mathcal{E}_c\right)}$$

$$\frac{I_D}{Z} = \frac{\mu_o C_o}{L + \dfrac{V_D}{\mathcal{E}_c}}\left[\left(V_G - V_T\right)V_D - m\frac{V_D^2}{2}\right]$$

Take log on both sides and then set the derivative to zero ….

$$V_{DSAT} = \frac{2\left(V_G - V_T\right)/m}{1 + \sqrt{1 + 2\mu_o\left(V_G - V_T\right)/m\upsilon_{sat}L}} < \frac{\left(V_G - V_T\right)}{m}$$

Velocity Saturation

$$J_{D,sat} = \frac{\mu_0 C_o}{L + \dfrac{V_{D,sat}}{\mathcal{E}_C}}\left[(V_G - V_T)V_{D,sat} - \frac{mV_{D,sat}^2}{2} \right]$$

$$\sim \frac{\mu_0 \mathcal{E}_C C_o}{V_{D,sat}}\left[(V_G - V_T)V_{D,sat} - \frac{mV_{D,sat}^2}{2} \right] \sim \upsilon_{sat} C_o (V_G - V_T)$$
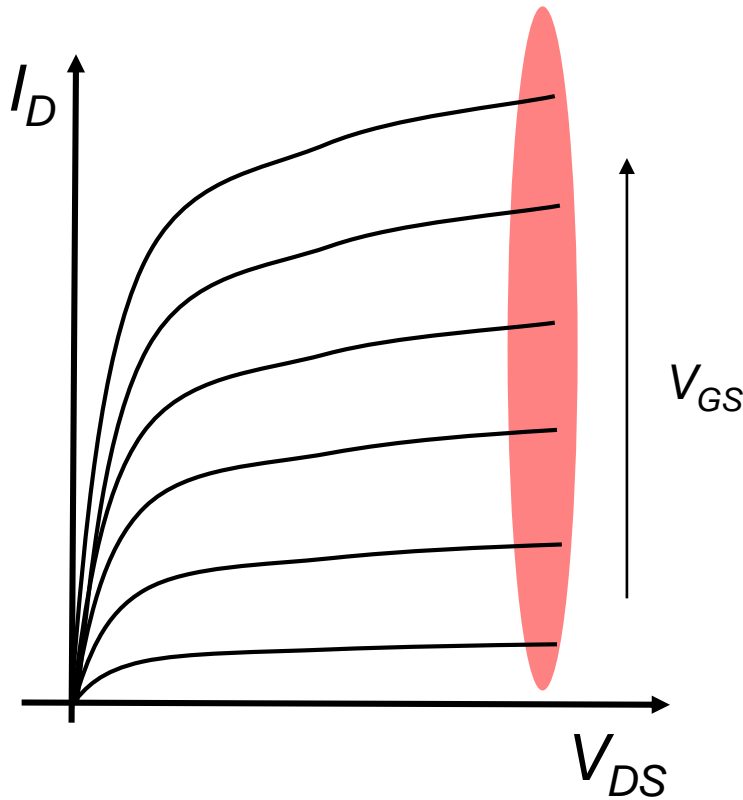
$$I_D = WC_{ox}\upsilon_{sat}(V_G - V_T)$$
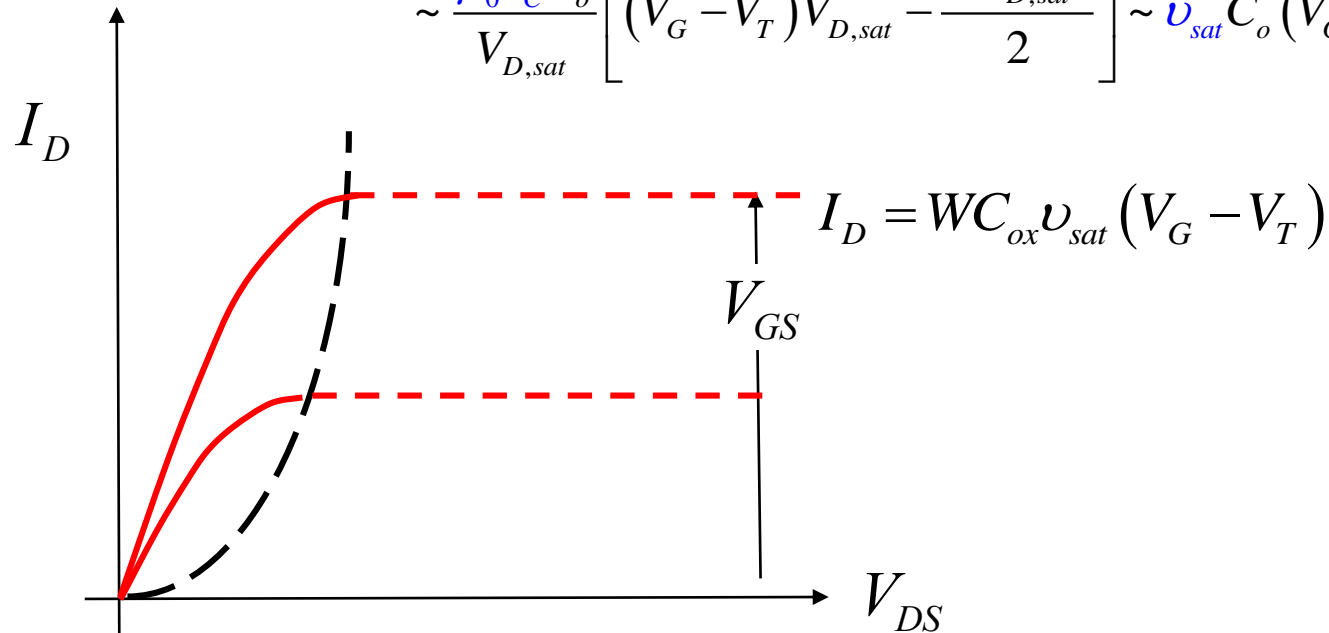
'Signature' of Velocity Saturation

$$I_D = \frac{Z\mu_0 C_o}{2L} \frac{(V_G - V_T)^2}{m}$$

$$I_D = Z\upsilon_{sat} C_o (V_G - V_T)$$
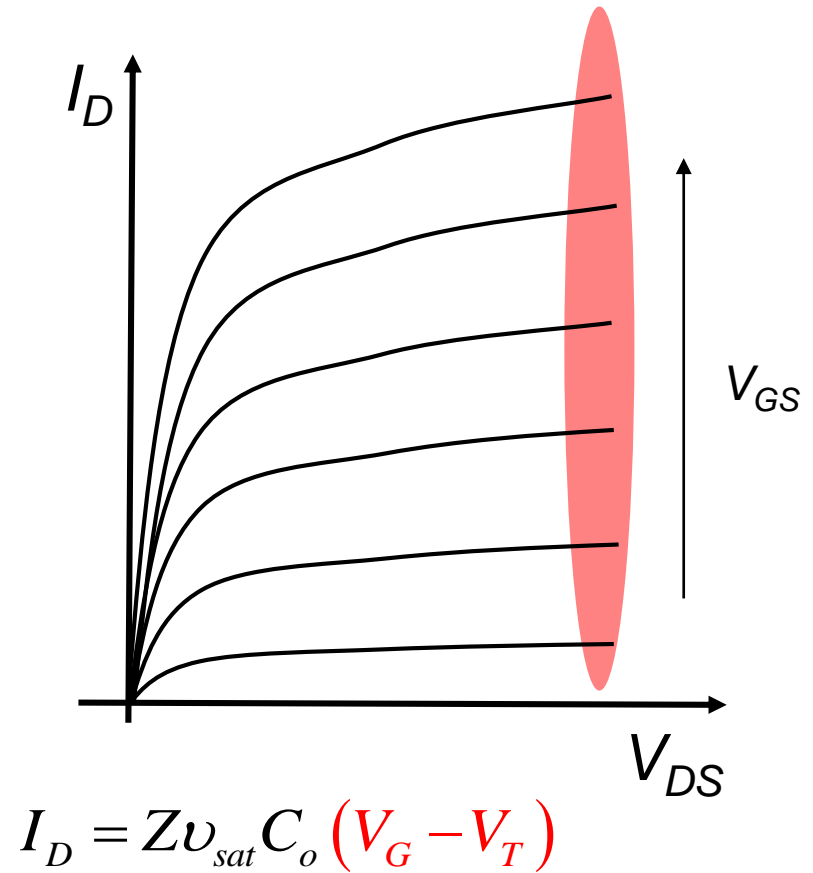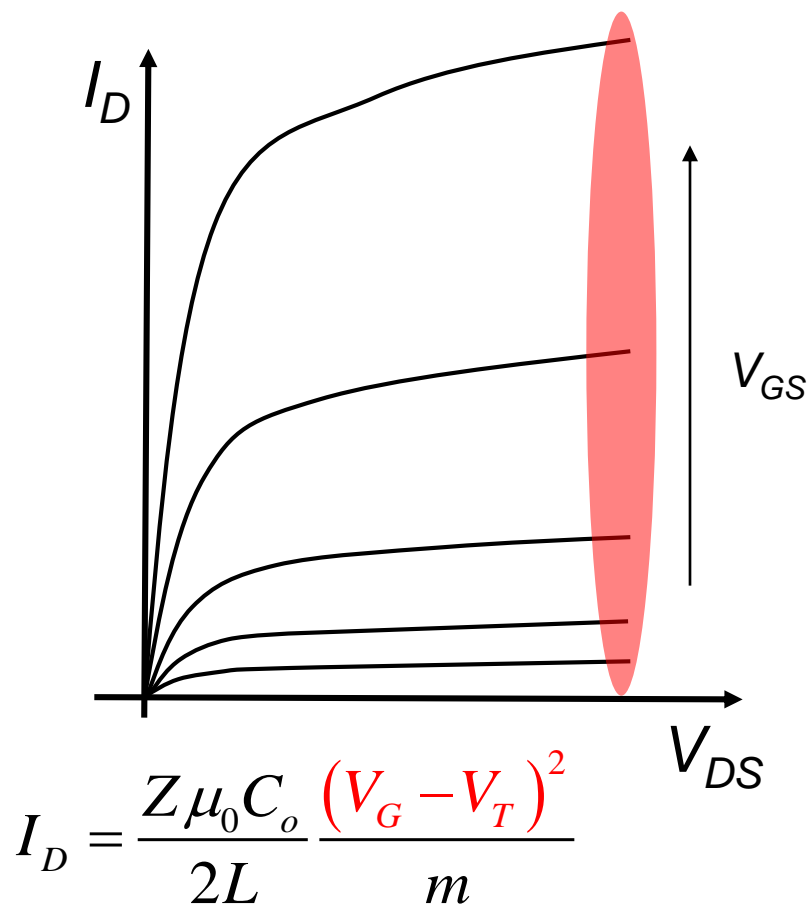
I_D and $(V_{GS} - V_T)$: In practice

. . . . .

$$I_D(V_D = V_{DD}) \sim \left(V_G - V_T\right)^{\alpha}$$

$$1 < \alpha < 2$$

Complete velocity saturation

Long channel

Topic: MOS-Capacitors

Objective: Being comfortable in calculating the internal quantities of a MOS-capacitor, including depletion width, surface electric field, oxide field, threshold voltage, etc.

Consider a silicon MOS-CAP with $N_A = 10^{16}\ cm^{-3}$. Calculate the maximum depletion width. Also, calculate the threshold voltage given the oxide thickness is 2 nm.

$\phi_B = k_B\ T/q \ln(N_A/n_i) = 0.3473$ V, and $\psi_s = 2\phi_B = 0.6946 V$

$$x_D = \left[\frac{2\ \kappa_s\ \epsilon_0\ (\psi_s)}{qN_A}\right]^{0.5} = 0.3 \times 10^{-4} cm$$

$$V_t = \phi_s - \frac{Q_B}{C_o} = 0.6946 + \frac{1.6 \times\ 10^{-19} \times 10^{16} \times 0.3 \times 10^{-4}}{3.9 \times\ 8.854 10^{-14}/(2 \times 10^{-7})} = 0.7225V$$

Explain to your satisfaction why: Capacitor area is absent, the dielectric constant is that of oxide, mobile charges are absent, and $E_{ox} = -\frac{Q_B}{x_0} C_0$

Topic: Nonideal MOS-Capacitors

Objective: Given various nonideal quantities, such as workfunction difference, trapped charges, interface defects, calculate MOS-C electrical performance.

For an Al-Silicon MOS-C, with Φ_M=4.10 eV and χ_{Si} =4.05eV. If the doping is $N_A = 10^{15}\ cm^{-3}$, then calculate the flat band voltage.

$\phi_B = k_B T/q\ \ln(N_A/n_i)$ = 0.29 V,

$$\phi_{ms} = \left(\chi_{Si} + \frac{E_G}{2} + \phi_B \right) - \Phi_M = 0.89V$$

Therefore, one must apply -0.89V to make the band flat.

Explain to your satisfaction why:
(a) In the ϕ_{ms} expression, if I wished to use E_G (not E_G/2), how should I have modified the expression to get the same result.
(b) Flatband voltage is negative, but the ϕ_{ms} is positive?
(c) Flatband voltage looks similar to the built-in voltage.

Topic: Nonideal MOS-Capacitors

Objective: Learning to interpret an experimental C-V characteristics

Based on the C-V characteristics, answer the following questions

1. Is this a MOSCAP or MOSFET ?
Ans. MOSCAP. Only a MOS-CAP shows such
High-frequency inversion capacitance behavior.

2. What is the threshold voltage?   Ans. -1V.

3. What is the flatband voltage? Ans. -2V

4. Is this a p-doped or n-doped semiconductor?
Ans. Accumulation occurs at negative voltage. Here, negative charge in the gate brings further increases the positive charge; hence, the substrate is p-type.
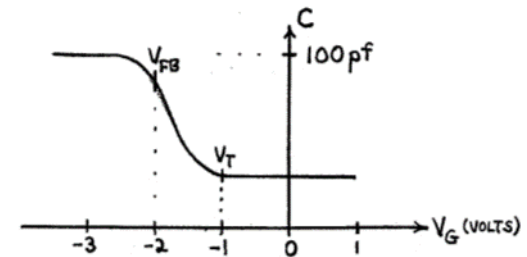
Topic: Nonideal MOS-Capacitors

Objective: Learning to interpret an experimental C-V characteristics

Based on the C-V characteristics, answer the following questions

5. If the material becomes a channel of a MOSFET, will this be NFET or PFET?
Ans. An N-MOSFET. MOSFET type is defined by the minority carriers (inversion)

6. Which voltage range would you use to determine the doping? Ans. -2V to -1V.

7. Which region will you check to determine the oxide thickness? Ans. Less than -2V.

8. Is this a small signal or a deep-depletion characteristics?
Ans. Small signal because capacitance at $V > V\_T$ is a constant. Deep depletion would show linear reduction in capacitance with voltage.

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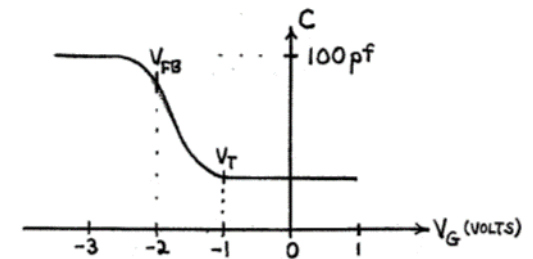
Topic: MOSFET

Objective: Calculate electrical parameters based on experimental data

$T = 300$ K

Oxide thickness: $x_0 = 2.2$ nm   Relative dielectric constant: $\kappa_{ox} = 4$

Power supply voltage: $V_{DD} = 1.2$ V   Series resistances: $R_S = R_D = 100\ \Omega - \mu m$

Actual channel length = 85 nm

From the so-called "on-current", $I_D\left(V_{SD} = V_{DD}, V_{DS} = V_{DD}\right)$, estimate the average velocity of electrons in the channel at the source end of the channel.

Solution:

$$\langle v(0)\rangle = \frac{I_{ON}}{WQ_n(0)}$$

$$Q_n(0) = C_{ox}\left(V_{GS} - I_D R_S - V_T\right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{x_o} = 1.6 \times 10^{-6}\ \ \text{F/cm}^2$$

$$Q_n(0) = \left(1.6 \times 10^{-6}\right)\left(1.2 - 1120 \times 10^{-6} \times 100 - 0.26\right) = 1.32 \times 10^{-6}$$

$$Q_n(0)/q \approx 8.3 \times 10^{12}\ \text{cm}^{-2}$$

$$\langle v(0)\rangle = \frac{I_{ON}}{WQ_n(0)} = \frac{1120 \times 10^{-6}}{10^{-4} \times 1.32 \times 10^{-6}} = 8.5 \times 10^7\ \text{cm/s}$$

$$\boxed{\langle v(0)\rangle = 8.5 \times 10^7\ \text{cm/s}}$$

Explain: Is this a long channel or a short channel transistor?
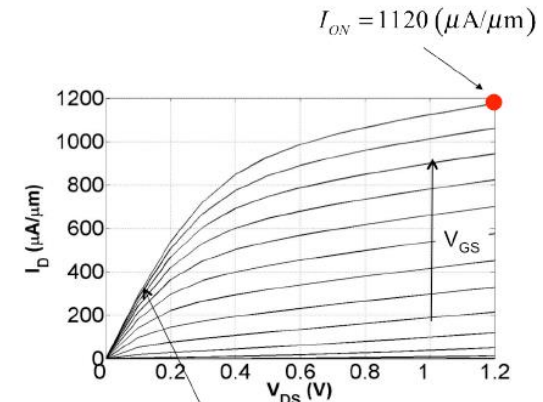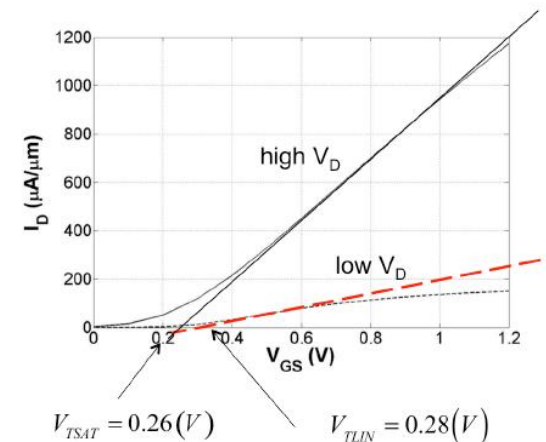
$I_{ON} = 1120\ (\mu A/\mu m)$

$R_{TOT} = \frac{V_{DS}}{I} = 340\ (\Omega - \mu m)$

high V_D

low V_D

$V_{TSAT} = 0.26\,(V)$ $V_{TLIN} = 0.28\,(V)$

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Warranty, product recall and other facts of life
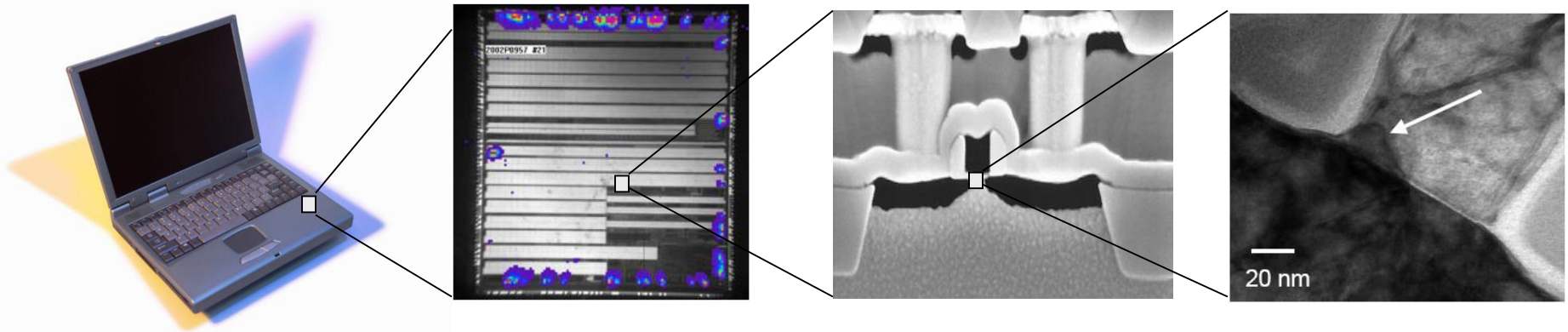
In this course, you are learning to analyze/design MOSFETs that go in an IC …

… because the ICs operate in incredibly harsh conditions, turning on and off trillions of time during its lifetime ….

… therefore the properties of the MOSFET keep changing. Eventually, S/D can be shorted, the gate oxide can break, etc ….

Measure of Flat-band shift from C-V Characteristics
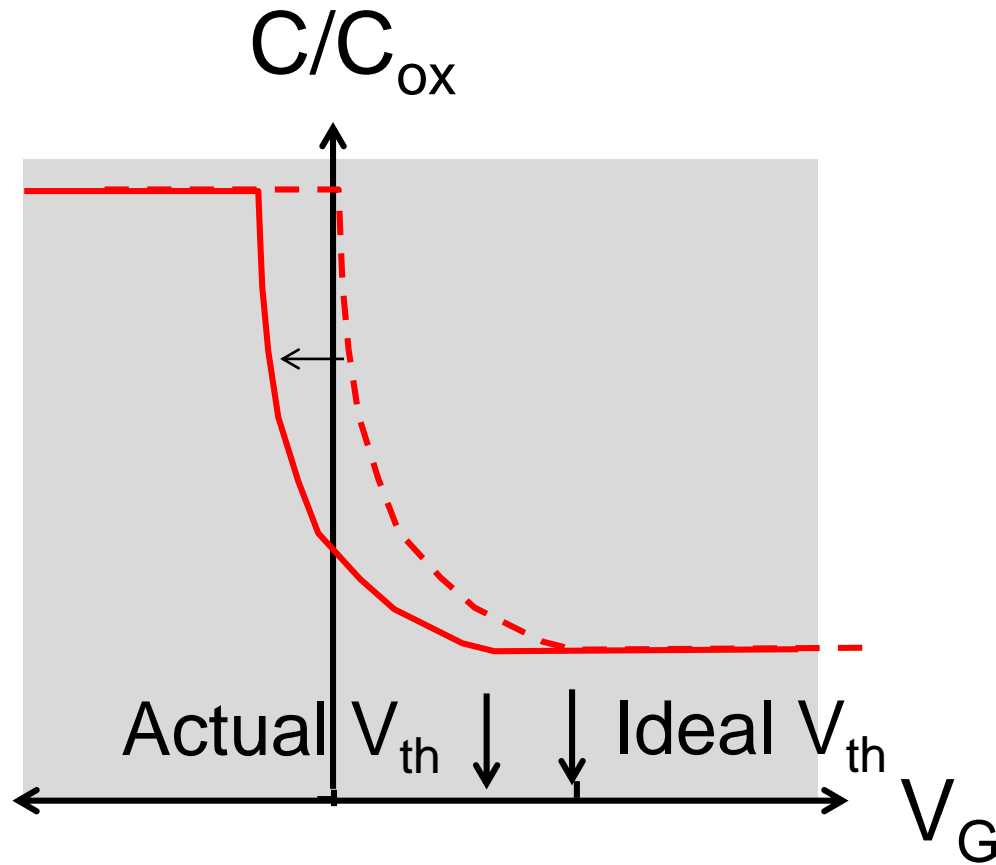
Idealized MOS Capacitor

Substrate (p)

y
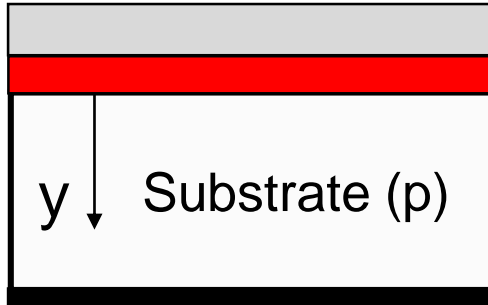
Recall that

$$Q_i = C_o(V_G - V_{T,ideal})$$

$$V_{T,ideal} = \phi_s - \left.\frac{Q_B}{C_o}\right|_{\phi_s = 2\phi_F}$$

Vacuum level

χ_i

χ_s

Φ_m

$Q_{ox}=0$

E_C

E_F

E_V

metal   insulator   p semiconductor

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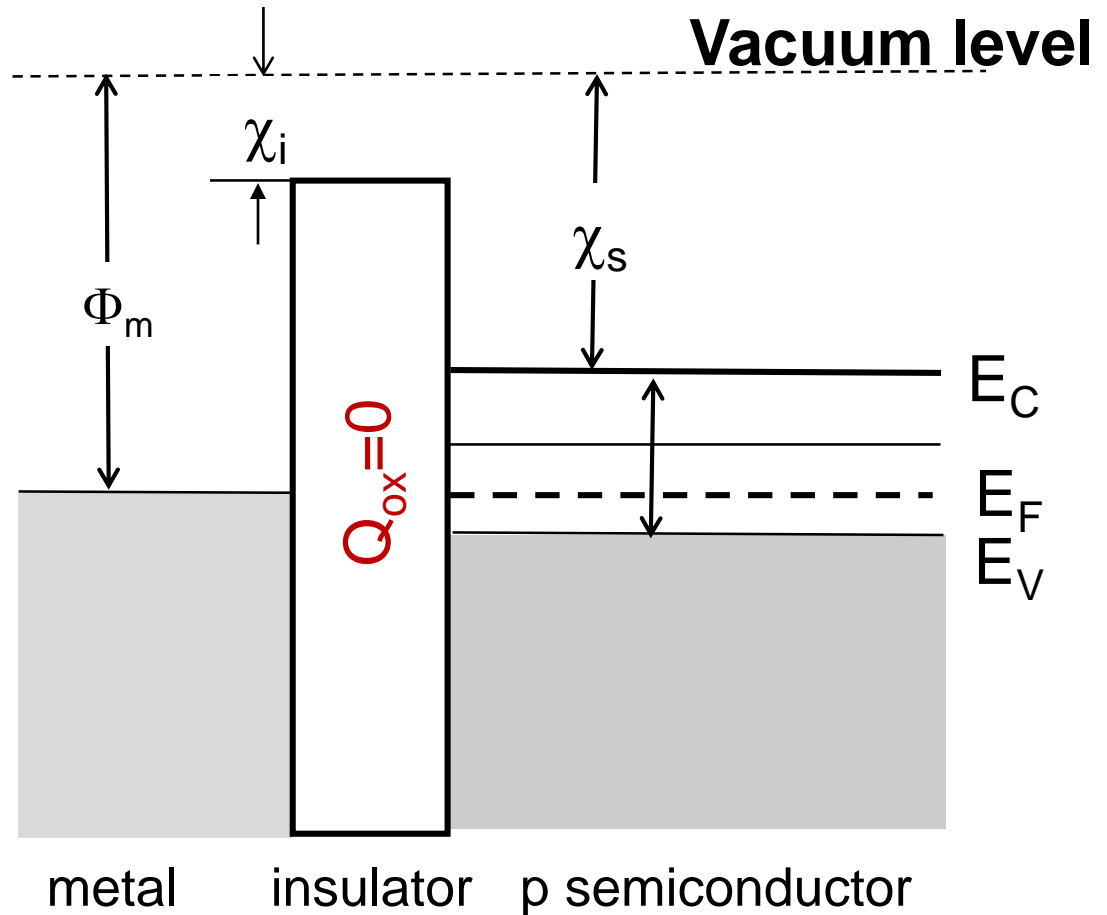
Distributed Trapped charge in the Oxide
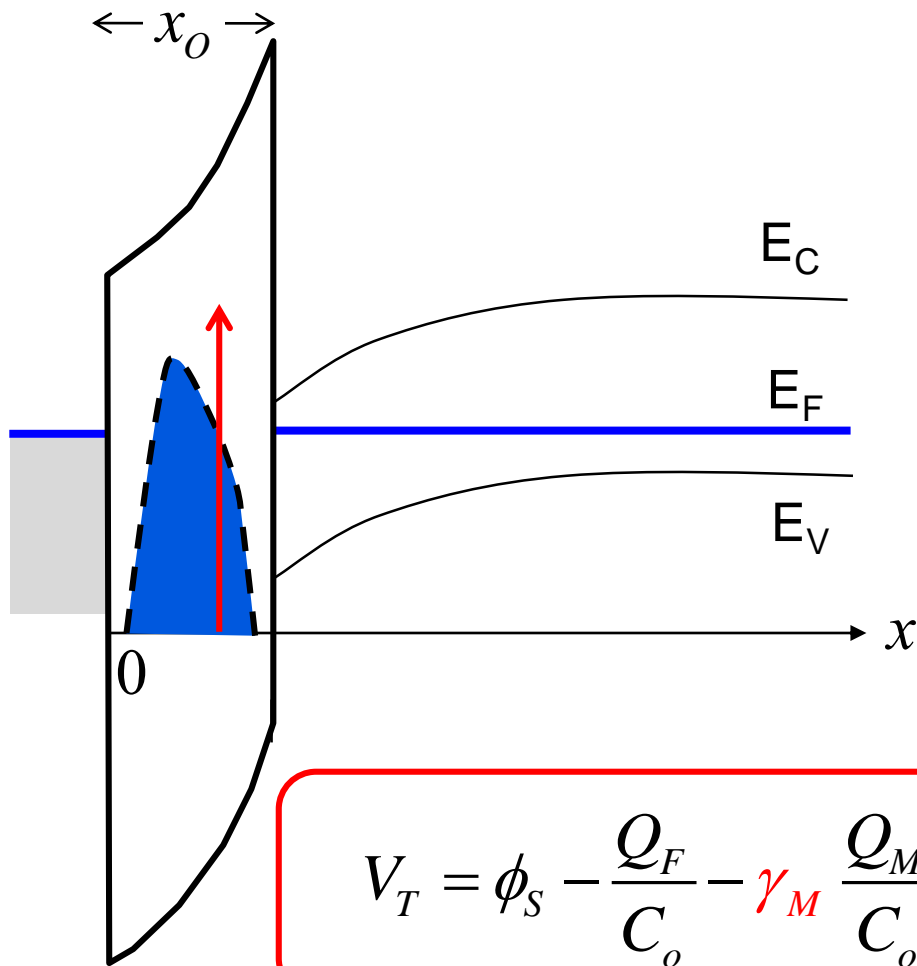
$$Q_M = \int_0^{X_O} \rho_{ox}(x)\,dx$$

$$\gamma_M \equiv \frac{x_M}{x_0} = \frac{\displaystyle\int_0^{x_0} x\,\rho_{ox}(x)\,dx}{\displaystyle x_0 \int_0^{x_0} \rho_{ox}(x)\,dx}$$

E_C

E_F

E_V

x

0

$\leftarrow x_O \rightarrow$

$$V_T = \phi_S - \frac{Q_F}{C_o} - \gamma_M \frac{Q_M}{C_o}$$

An Intuitive View

Ideal charge-free oxide

Bulk charge

$-\mathcal{E}$

$-\mathcal{E}$

Interface charge

$-\mathcal{E}$
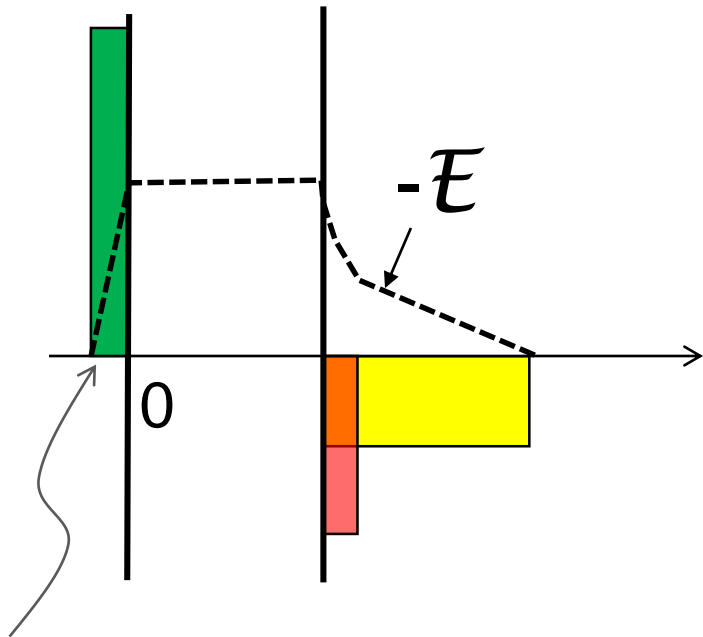
Reduced gate charge

0

0

0

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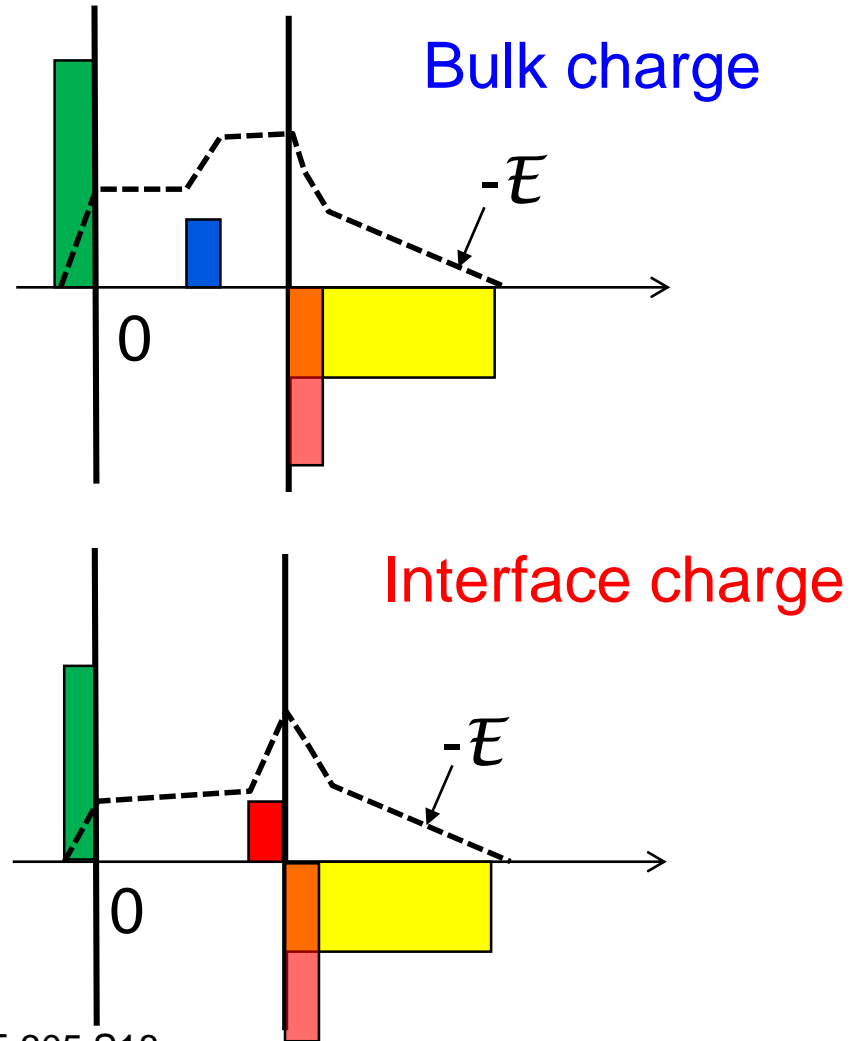
Gate Voltage and Oxide Charge

$$V_G = \Delta V_{ox} + \phi_s$$

$$-\frac{d^2 V_{ox}}{dx^2} = \frac{d\mathcal{E}_{ox}}{dx} = \frac{\rho_{ox}(x)}{K_o \varepsilon_0}$$

$$\int_{\mathcal{E}(x)}^{\mathcal{E}(x_0)} d\mathcal{E}_{ox} = \int_x^{x_0} \frac{\rho_{ox}(x')dx'}{K_o \varepsilon_0}$$

$$-\frac{dV_{ox}}{dx} = \mathcal{E}_{ox}(x) = \mathcal{E}_{ox}(x_0) - \int_x^{x_0} \frac{\rho_{ox}(x')dx'}{K_o \varepsilon_0}$$

$$\Delta V_{ox} = \frac{K_S}{K_o} x_0 \mathcal{E}_S(x_0) - \int_0^{x_0} dx \int_x^{x_0} \frac{\rho_{ox}(x')dx'}{K_o \varepsilon_0}$$

$$= \frac{K_S}{K_o} x_0 \mathcal{E}_S(x_0) - \int_0^{x_0} \frac{x\rho_{ox}(x)dx}{K_o \varepsilon_0}$$

-E

0
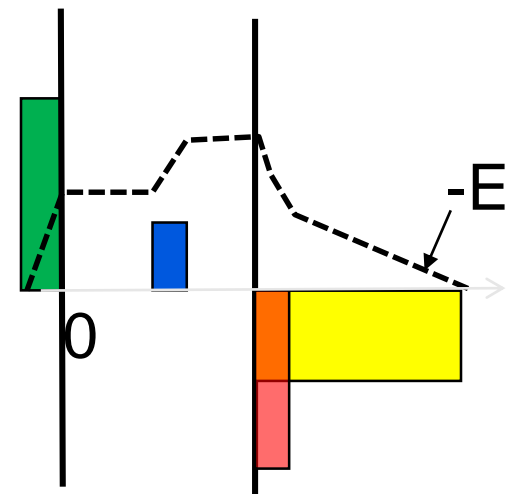
Gate Voltage and Oxide Charge

$$\Delta V_{ox} = \frac{K_S}{K_o} x_0 \mathcal{E}_S(x_0) - \int_0^{x_0} \frac{x \rho_{ox}(x)dx}{\left(\dfrac{K_o \varepsilon_0}{x_0}\right) x_0} \qquad = V_{T,ideal} - \frac{1}{C_o x_0} \int_0^{x_0} x \rho_{ox}(x)dx$$

$$= \frac{K_S}{K_o} x_0 \mathcal{E}_S(x_0) - \frac{1}{C_o x_0} \int_0^{x_0} x \rho_{ox}(x)dx \qquad = V_{T,ideal} - \frac{Q_M}{C_o} \gamma_M$$

$$V_{th} = \psi_s (= 2\phi_F) + \Delta V_{ox}$$

$$= \psi_s (= 2\phi_F) + \frac{\kappa_S}{\kappa_{ox}} x_0 \mathcal{E}_S(x_0) - \frac{1}{C_o x_0} \int_0^{x_0} x \rho_{ox}(x)dx$$

Interpretation for Bulk Charge

$$V_T = V_{T,ideal} - \frac{1}{C_o x_0} \int_0^{x_0} x \rho_{ox}(x)\delta(x-x_1)dx$$

$$= V_{T,ideal} - \frac{x_1}{x_0} \frac{Q_M(x_1)}{C_o}$$

C/C$_{ox}$

Ideal V$_T$

New V$_T$

V$_G$
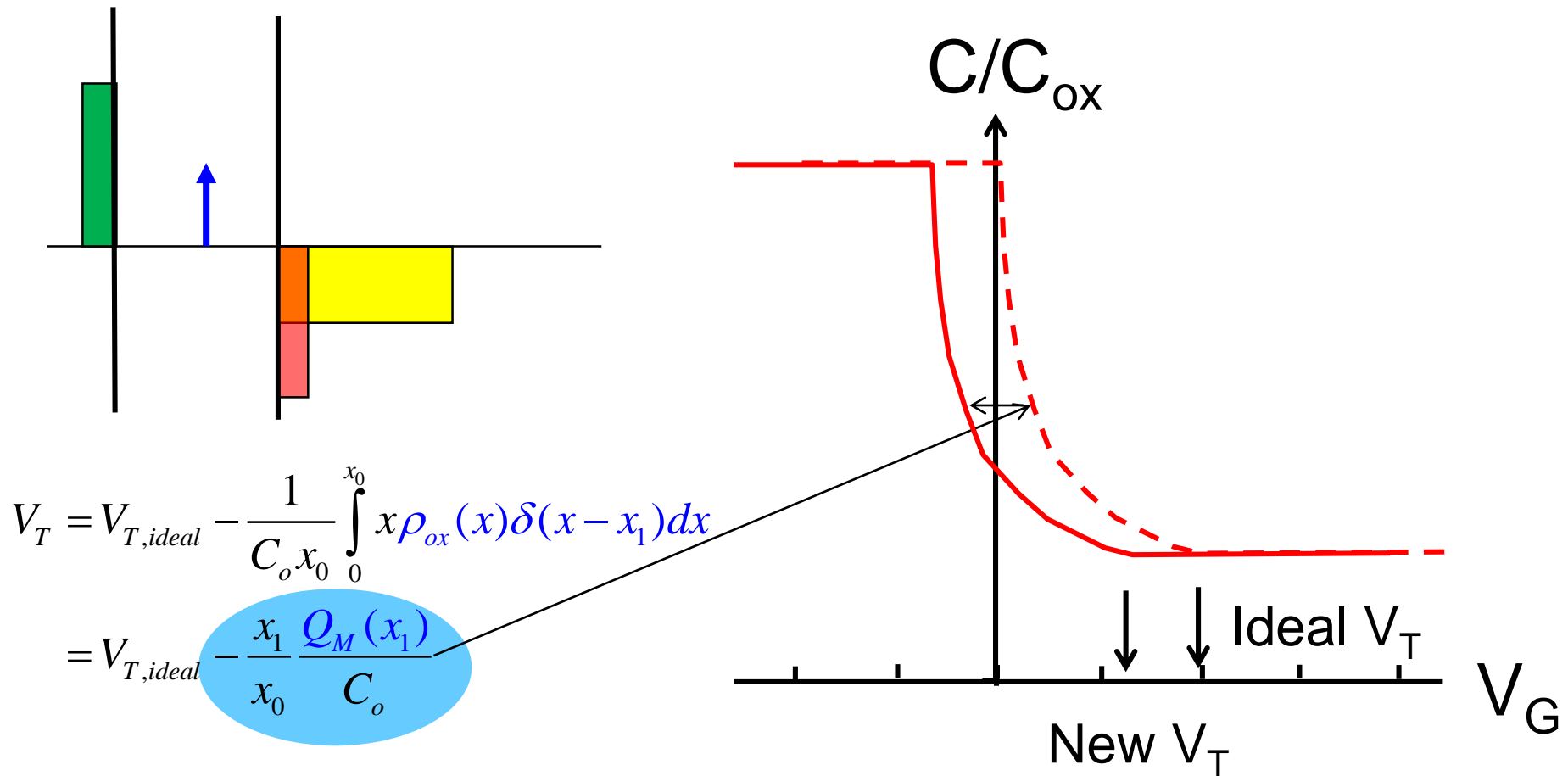
Interpretation for Interface Charge

$$V_T = V_{T,ideal} - \frac{1}{C_o x_0} \int_0^{x_0} x \rho_{ox}(x) \delta(x - x_o) dx$$

$$= V_{T,ideal} - \frac{Q_F}{C_o}$$

Ideal V_T

New V_T

C/C_{ox}

V_G
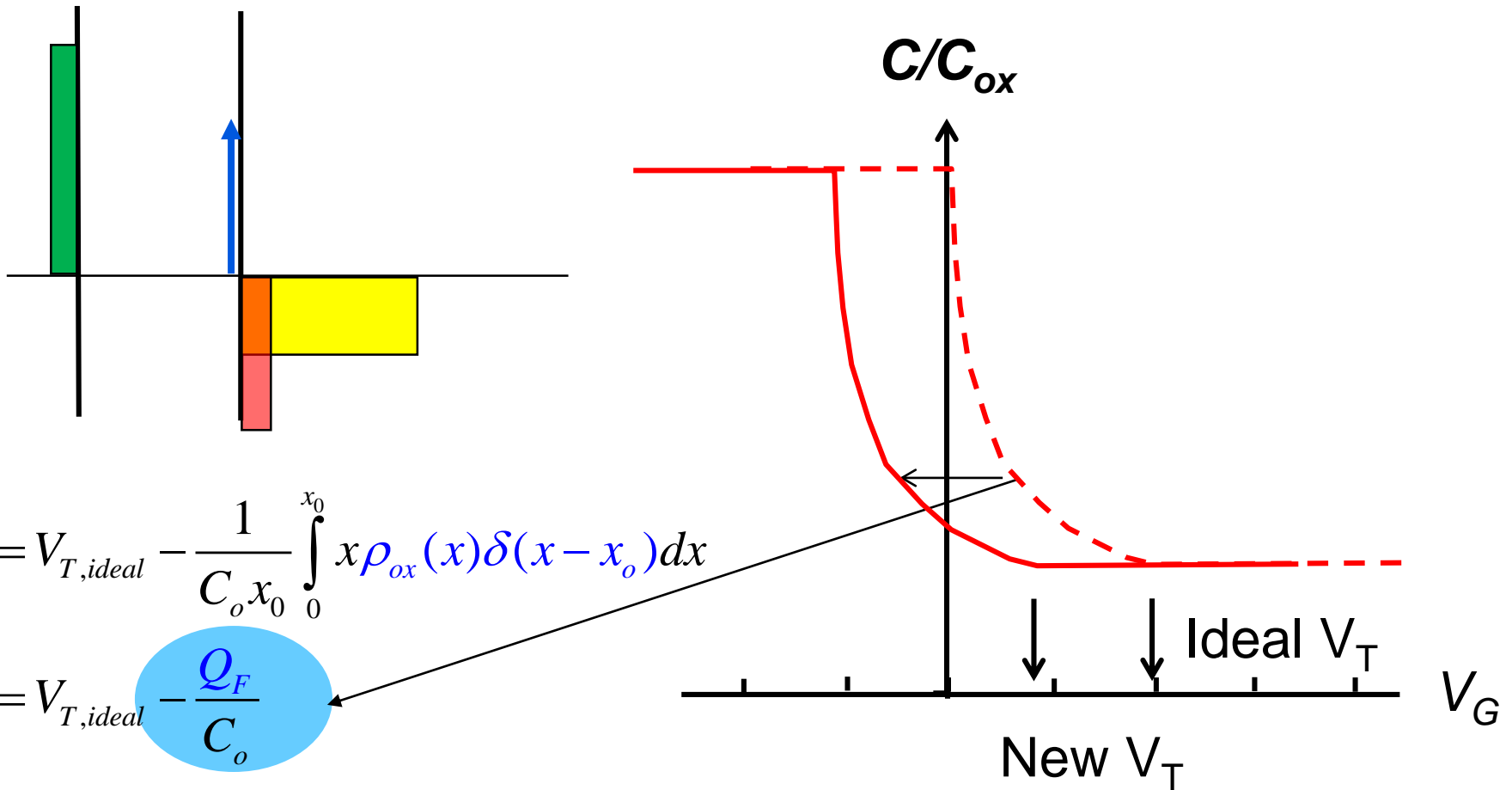
Time-dependent shift of Trapped Charge
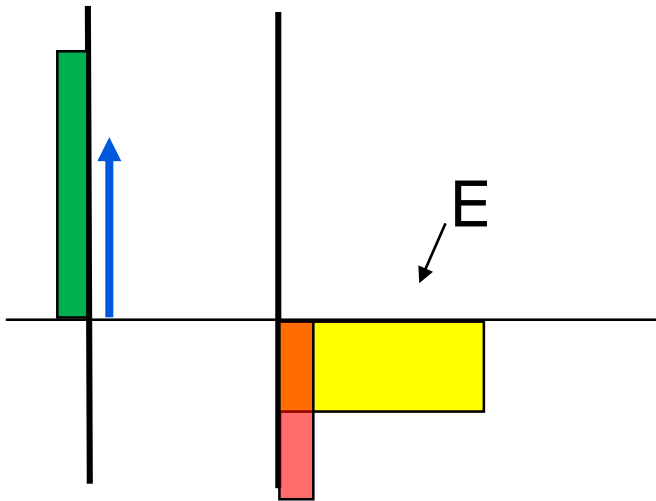
$$V_T = V_{T,ideal} - \frac{1}{C_o x_0} \int_0^{x_0} x Q_{ox}(x) \times \delta(x - x_1(t)) dx$$

$$= V_{T,ideal} - \frac{x_1(t)}{x_0} \times \frac{Q_{ox}(x)}{C_o}$$
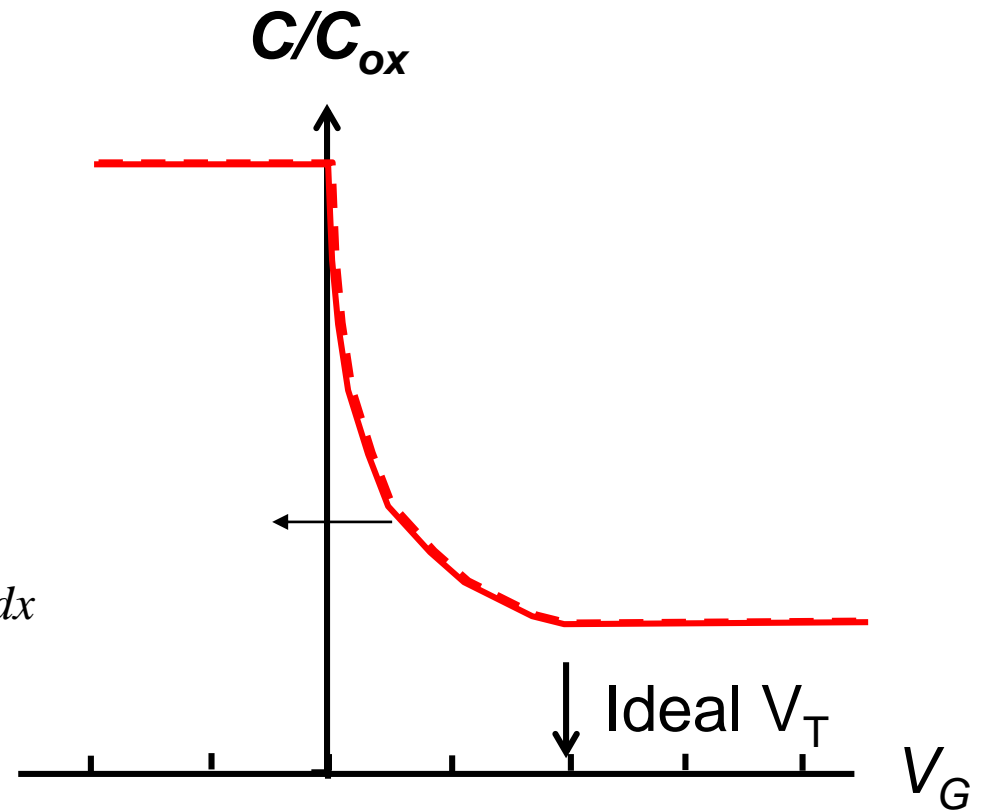
Sodium related bias temperature instability (BTI) issue

Dielectric Breakdown

Gate Current

Breakdown

ln (time)

$V_{G1} > V_{G2} > V_{G3}$ VDD

$\ln(-\ln(1-F))$

log(TBD)
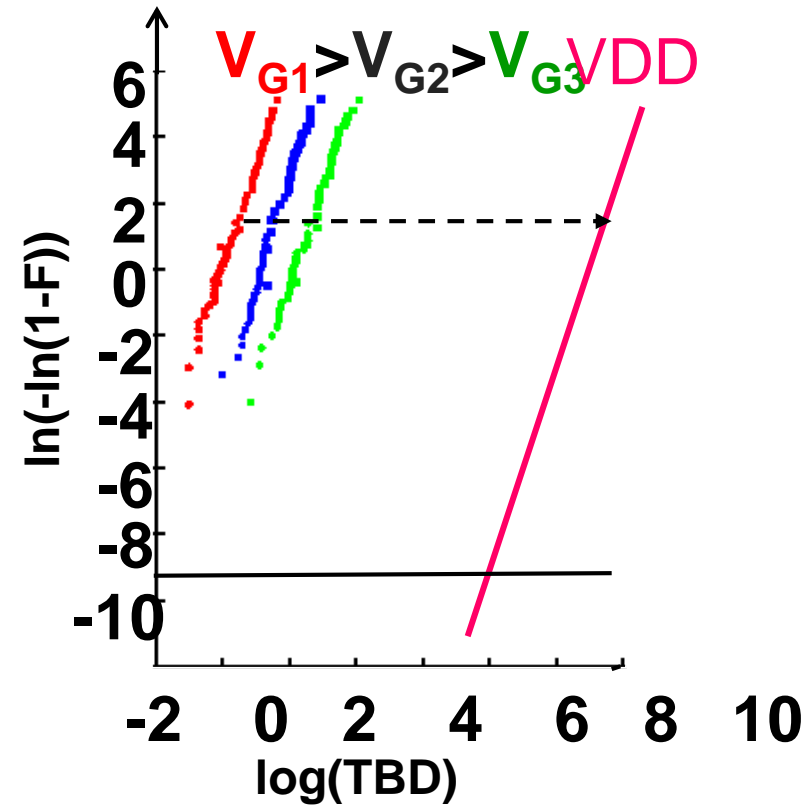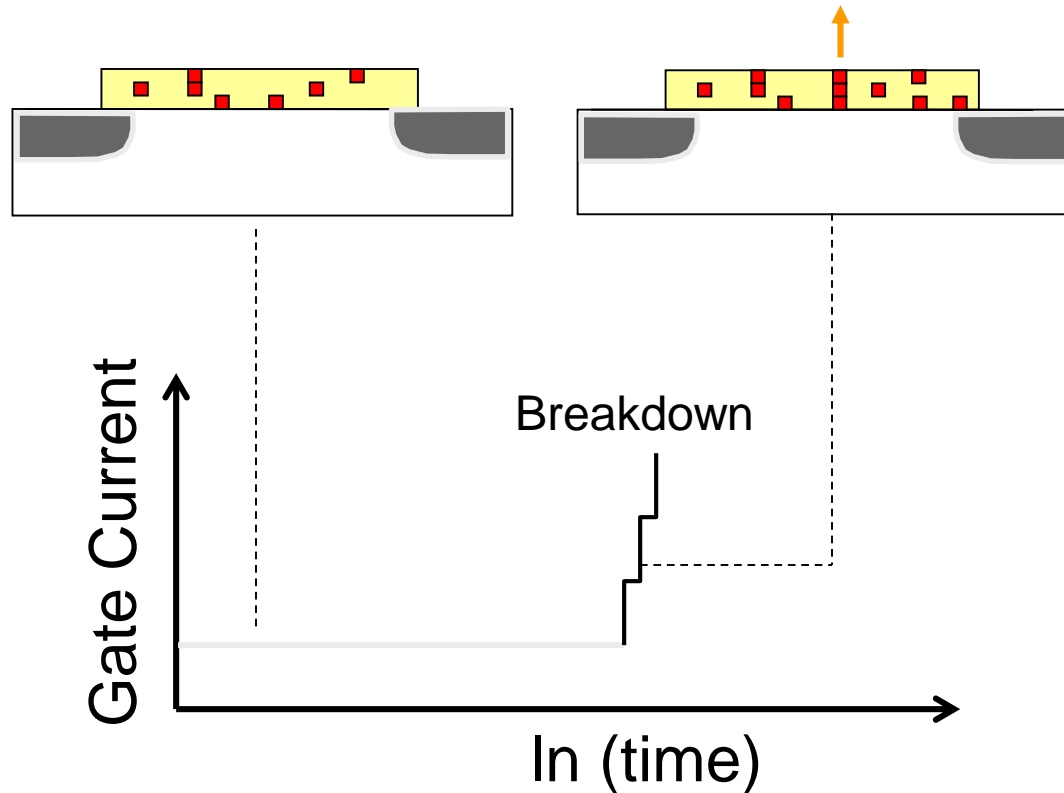
Radiation Induced Charge Buildup

(4) Radiation-induced interface traps within Si bandgap

Si

SiO$_2$

(3) Deep hole trapping near Si-SiO$_2$ interface

Gate

(1) Electron-hole pairs generated by ionizing radiation

(2) Hopping transport of holes through localized states in SiO$_2$ bulk

50 Mrad(Si) 8MeV elec

C/C$_{ox}$

Ideal V$_T$

Actual V$_T$

V_G
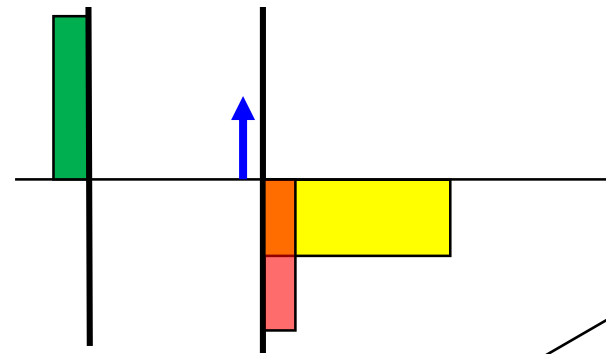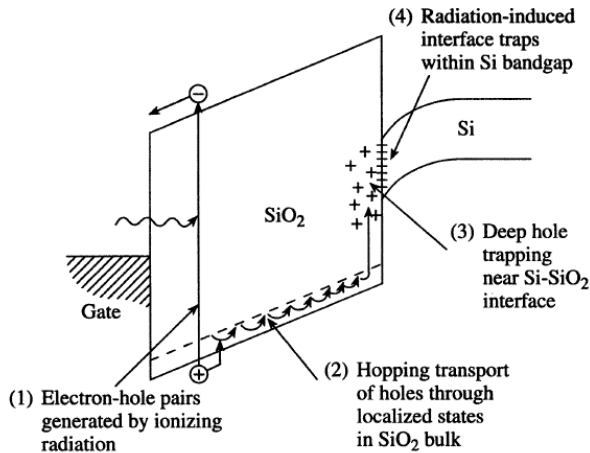
$$V_{th} = V_{th}^{*} - \frac{x_1}{x_0} \frac{Q_{ox}(x_1, t)}{C_{ox}}$$
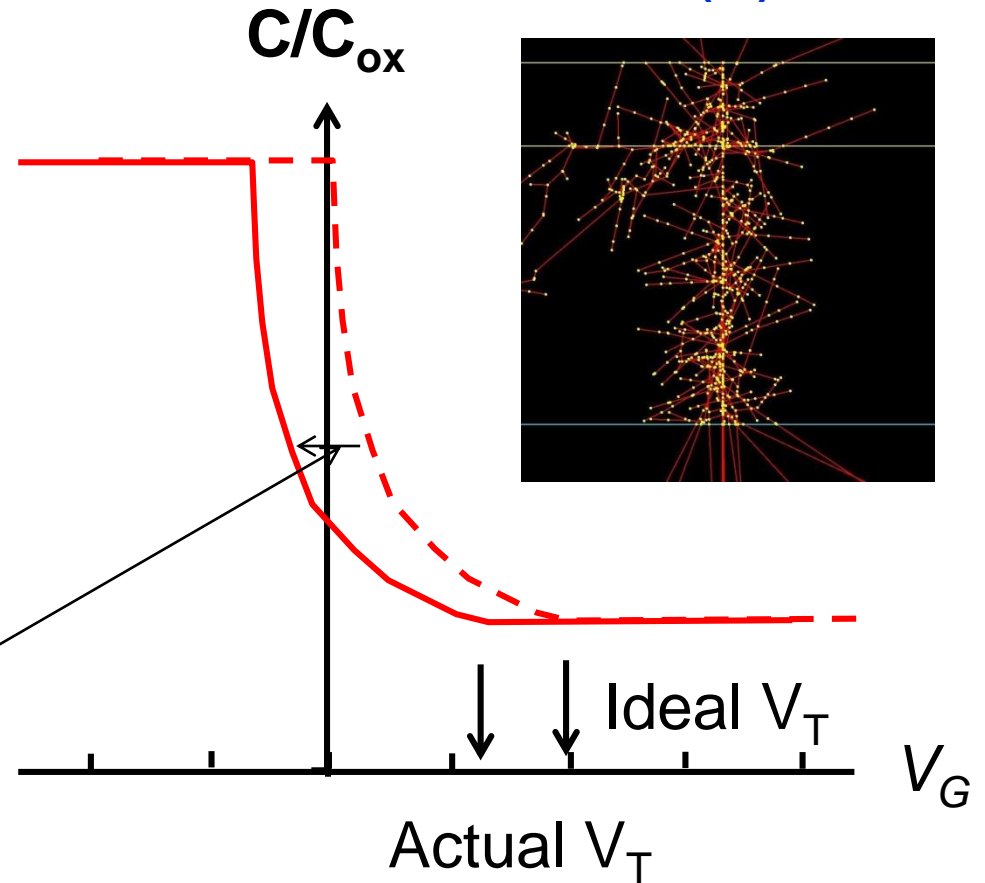
Bias Temperature Instability (Experiment)

M   O   S   M   O   S

(-) biases

(+) biases

ρ_{ion}

ρ_{ion}

0.1x

0.9x

0

x_o

0

x_o

X

X

$\Delta V_{FB} = -79$ V

1.0

0.9

0.8

0.7

0.6

$\frac{C}{C_o}$

Before bias temperature

After +12 V bias 100° C 70 min

After −30 V or 0 V bias 200° C 60 min

−140 −120 −100 −80 −60 −40 −20 0

V_G

Negative Bias Temperature Instability

before stress

after stress

I_D (mA)

V_D (volts)

Spec.

Warranty

% degradation

Stress Time (sec)

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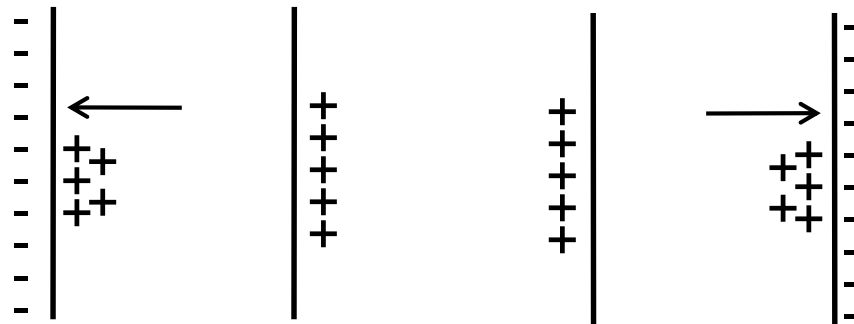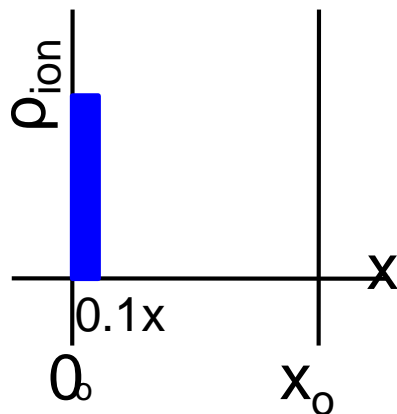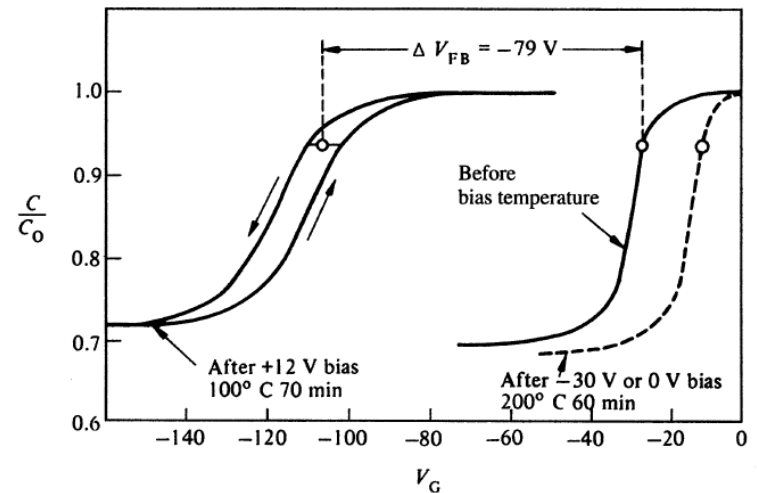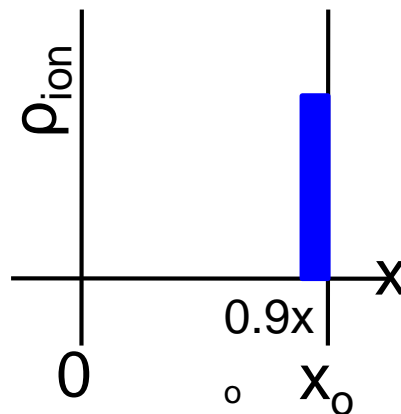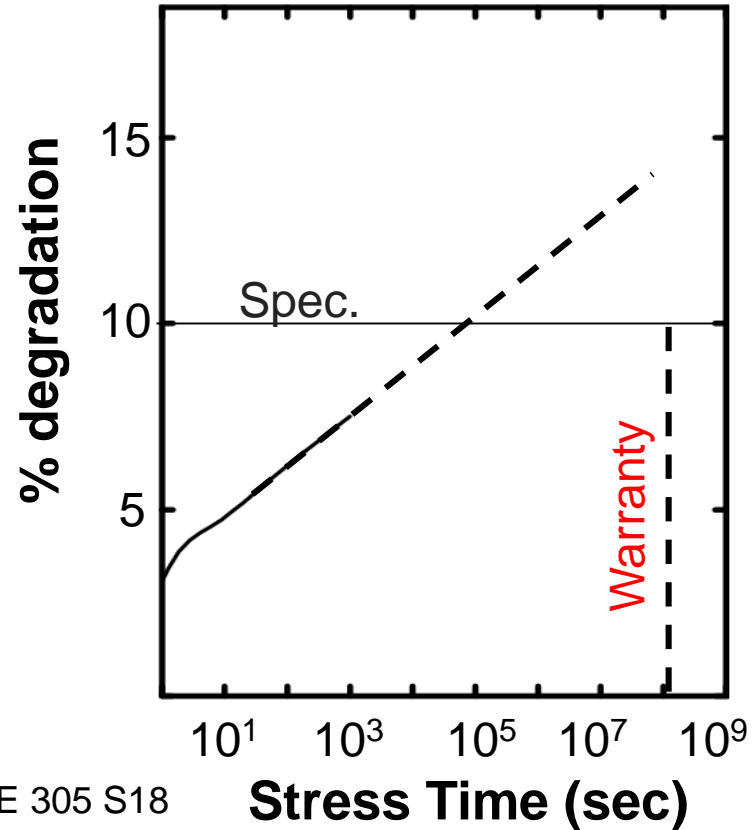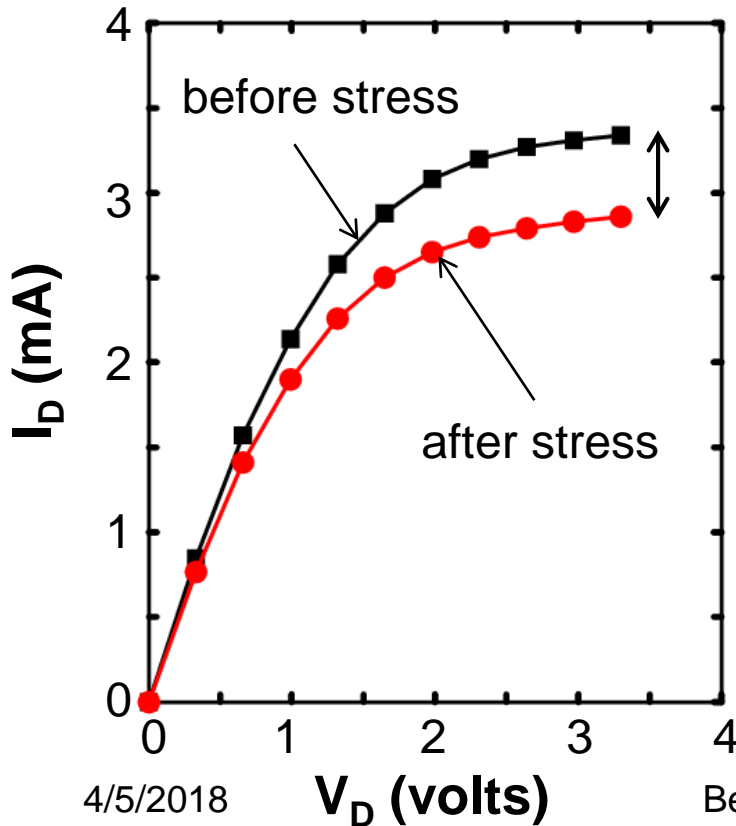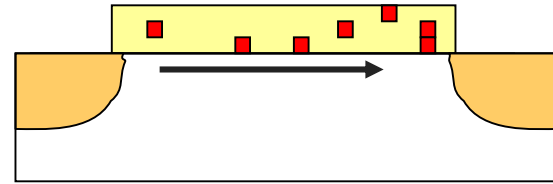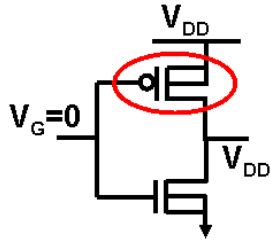
SiO and SiH Bonds

Google image

Gate Oxide (SiO$_2$), *amorphous*

Si-Channel, *crystalline*
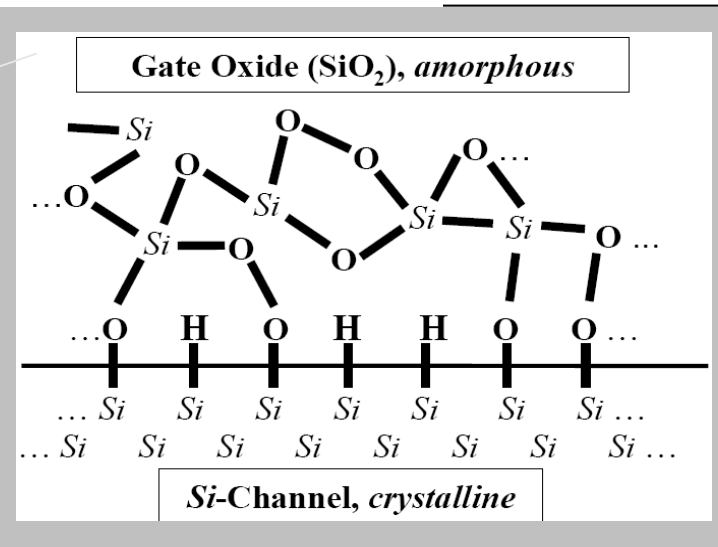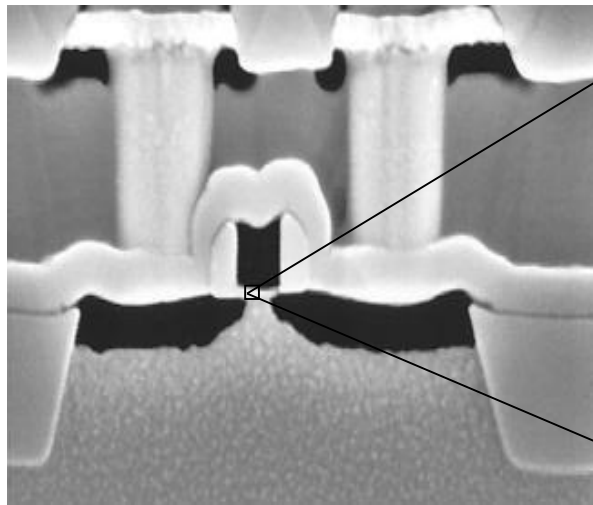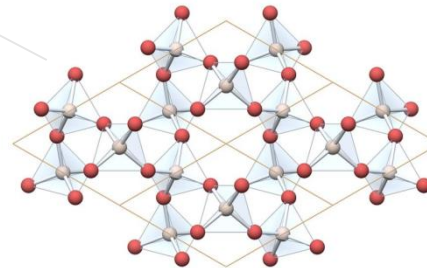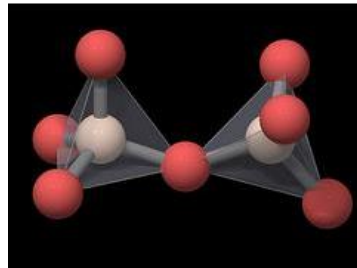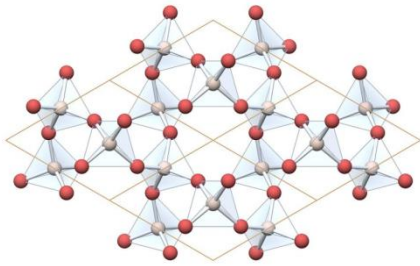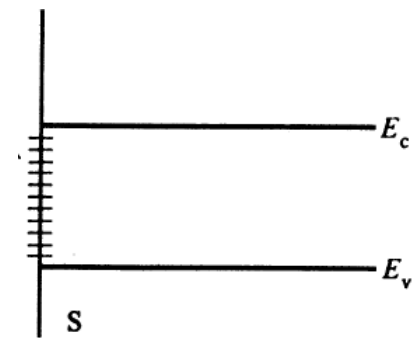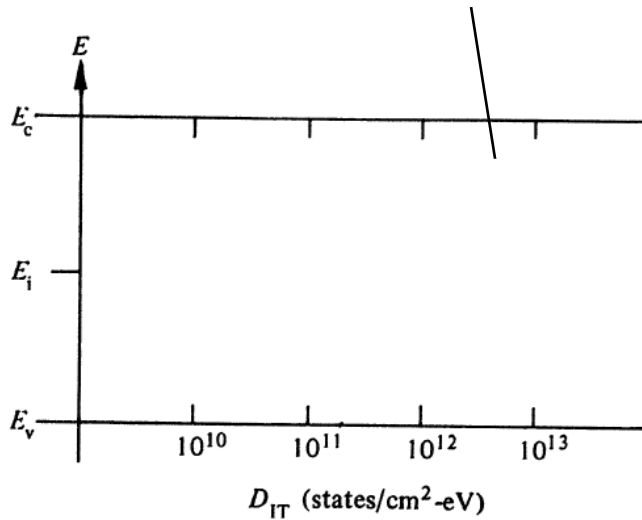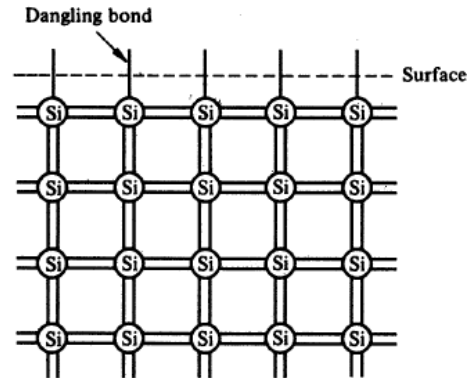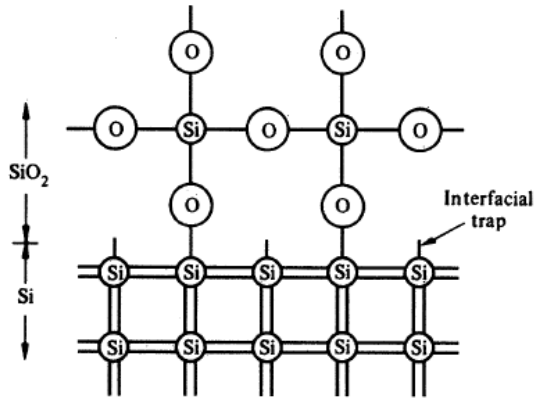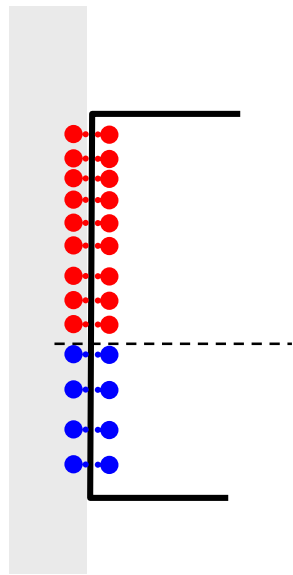
Interface States

'Annealing' of Interface States

Forming gas anneal
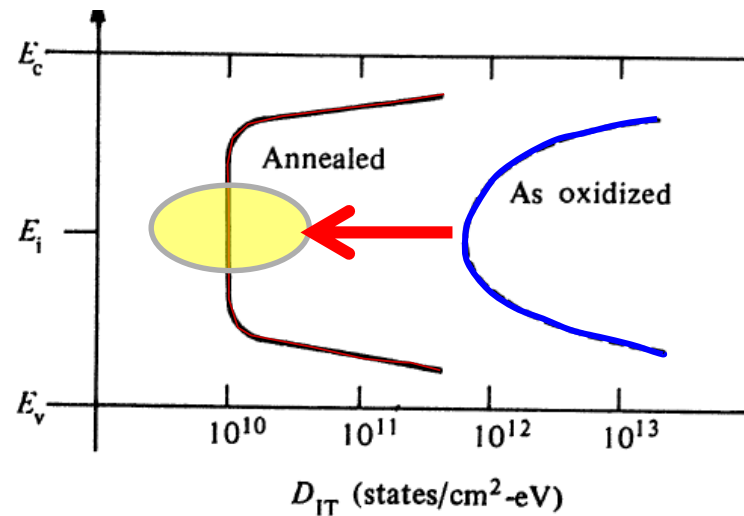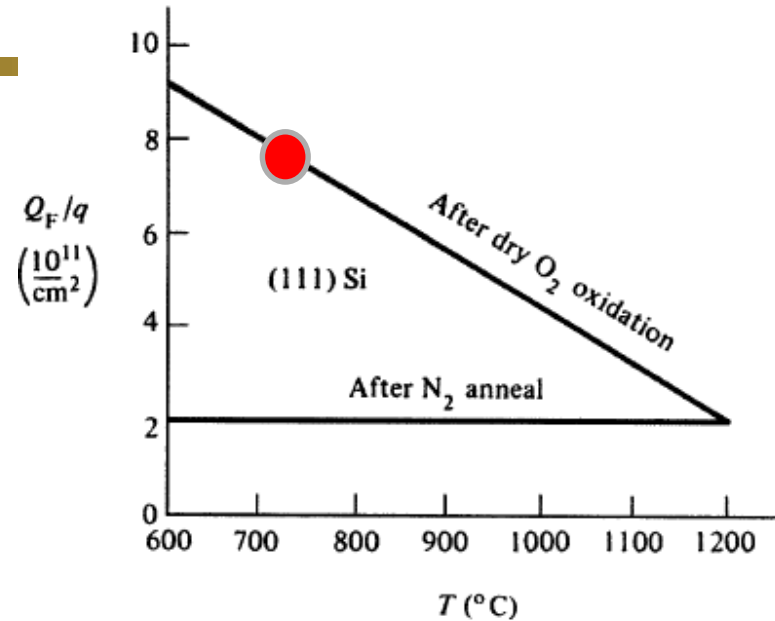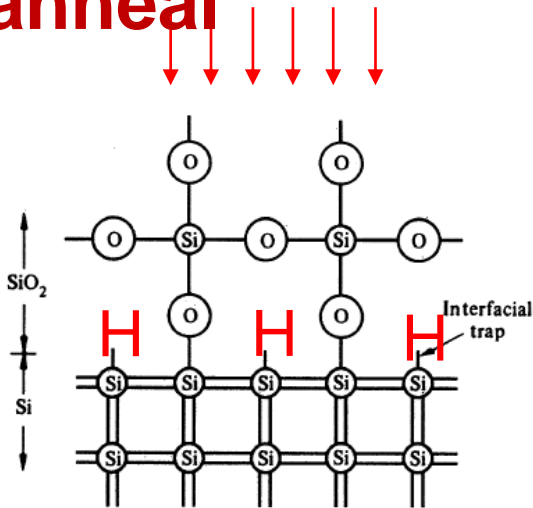
C-V Stretch Out

Forming gas anneal

33
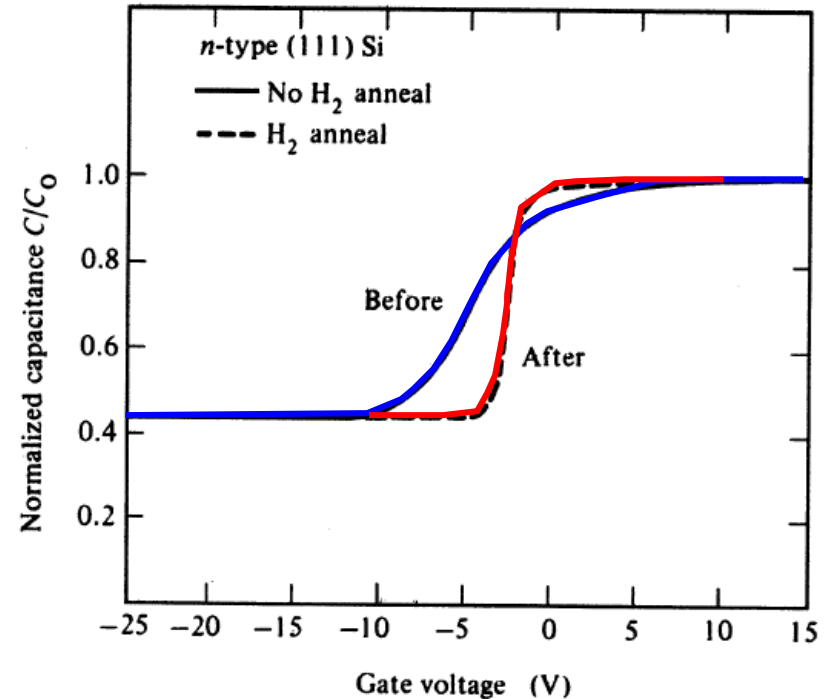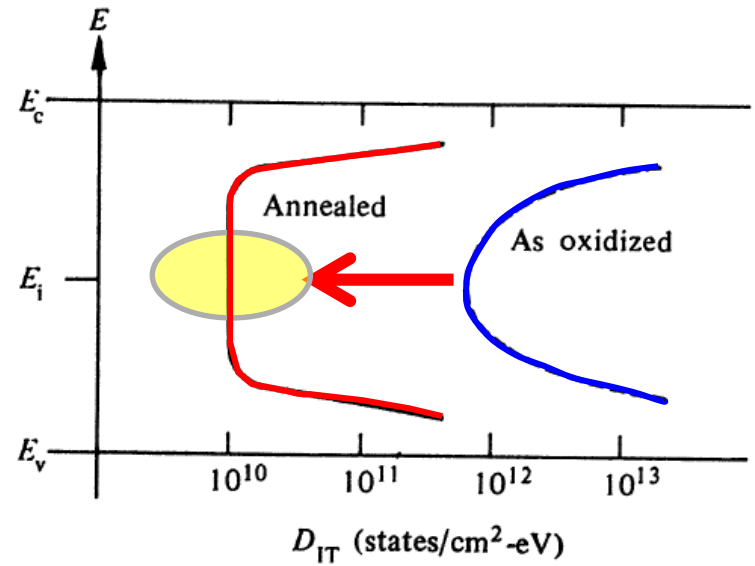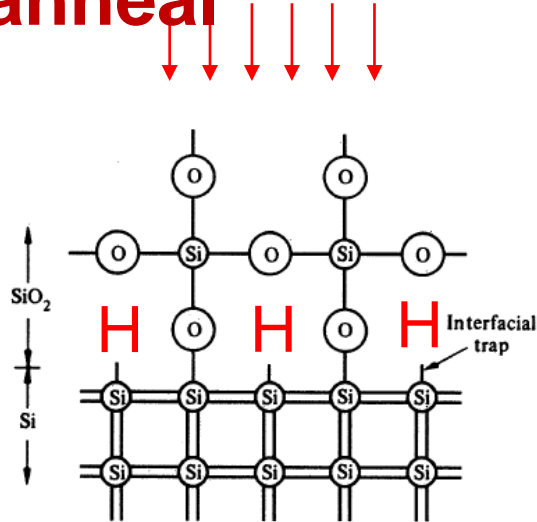
Nature of Donor and Acceptor Traps
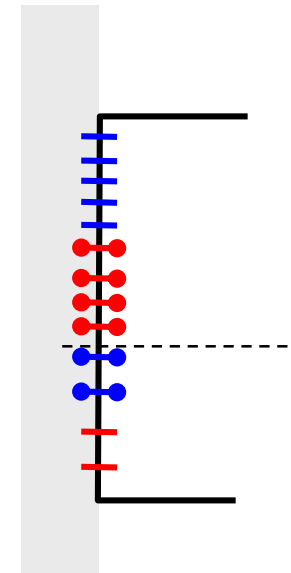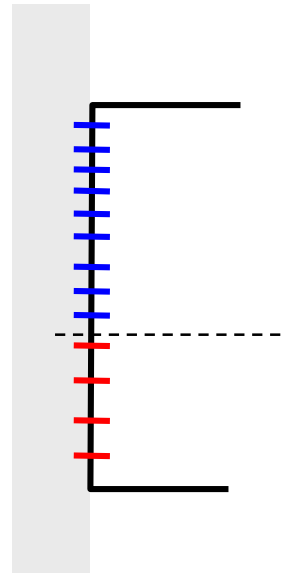
Donor level
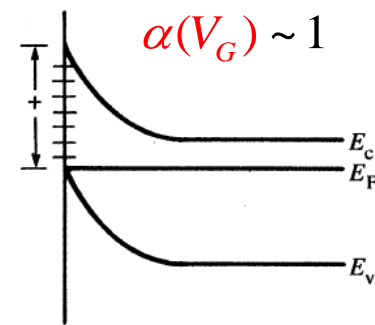Positive when empty
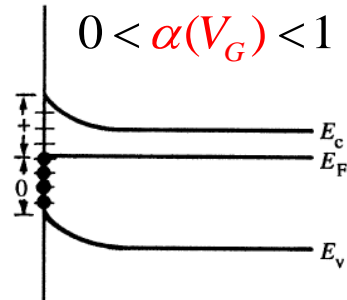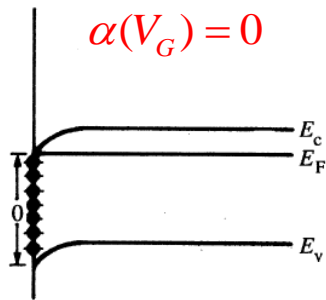Neutral when full

Acceptor level
Neutral when empty
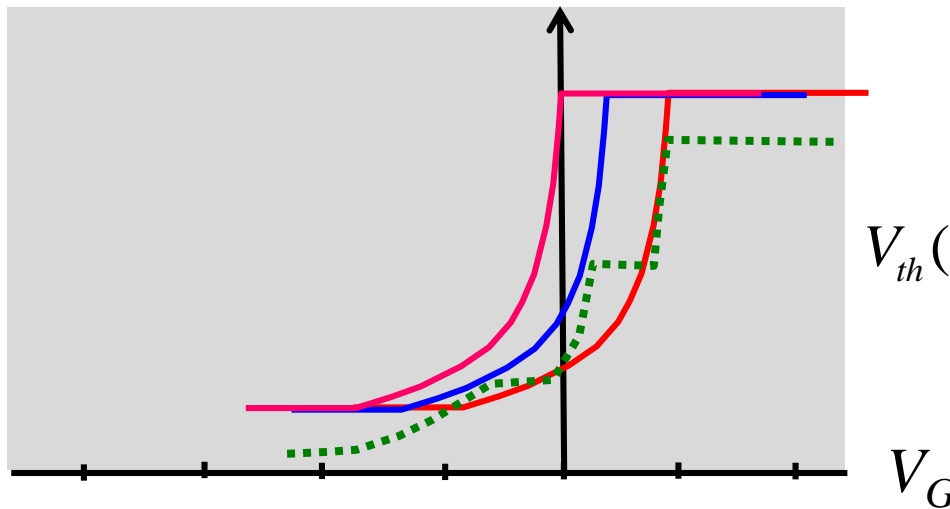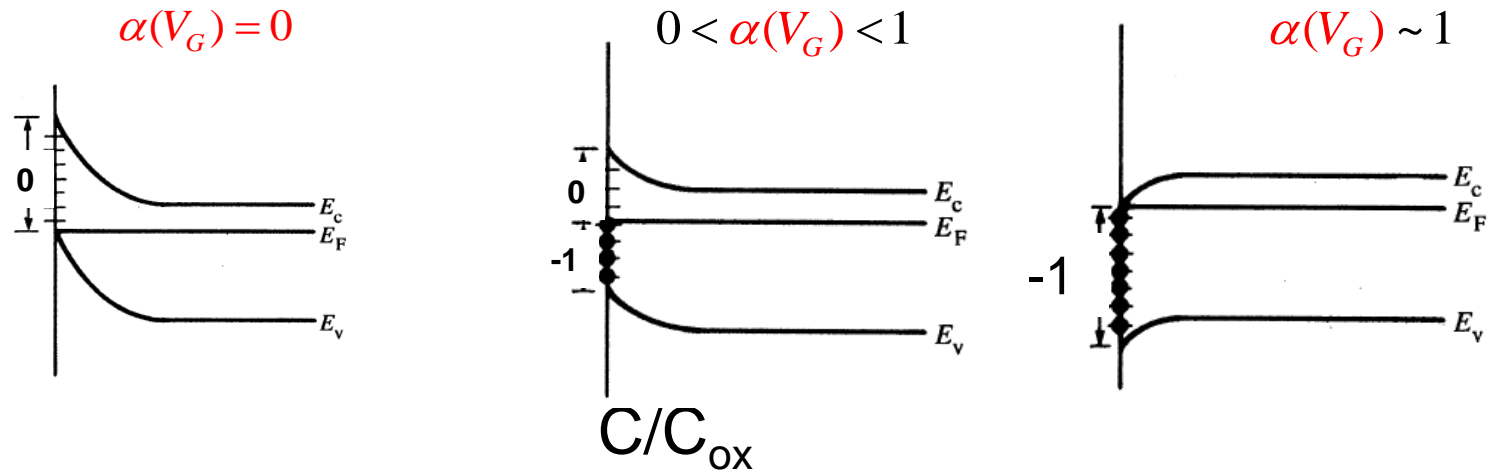Negative when full

Combination when both are present

Donor-like Interface States

$$V_{th} = V_{th}^* - \frac{1}{C_{ox} x_0} \int_0^{x_0} x \times \alpha(V_G) \times Q_{ox}(x)\delta(x - x_o)dx = V_{th}^* - \frac{\alpha(V_G)Q_{ox}(x_0)}{C_{ox}}$$

$\alpha(V_G) = 0$

$0 < \alpha(V_G) < 1$

$\alpha(V_G) \sim 1$

Bermel ECE 305 S18
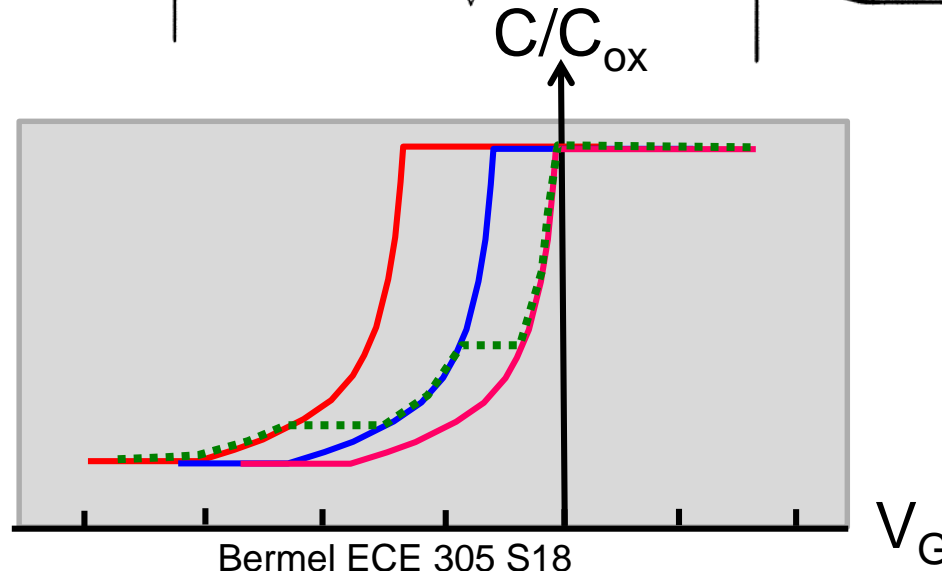
Acceptor-like Interface States

$\alpha(V_G) = 0$

$0 < \alpha(V_G) < 1$
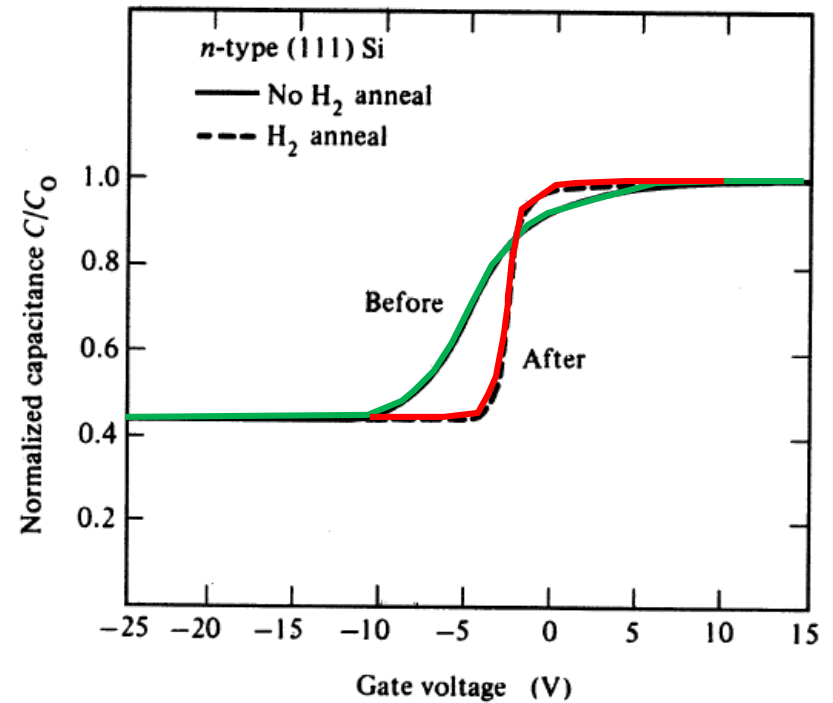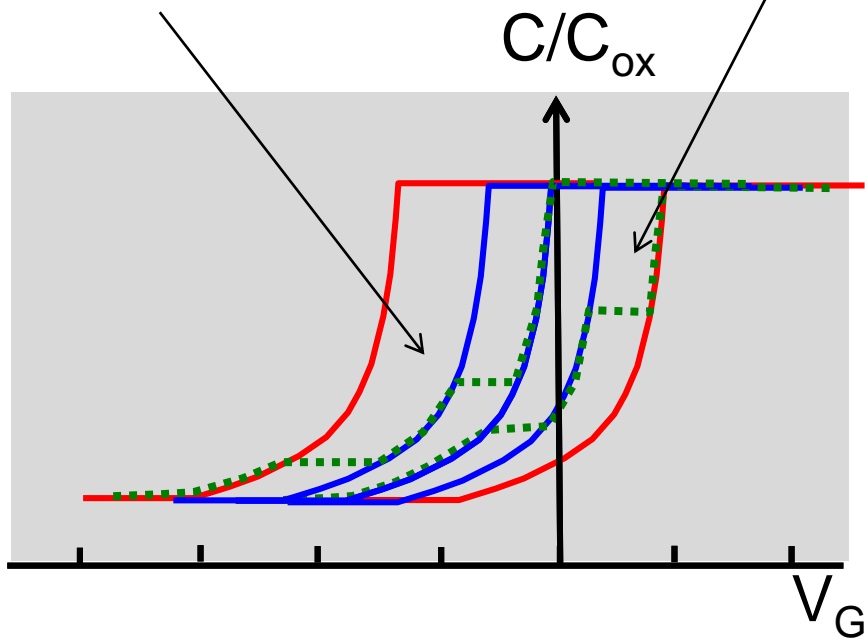
$\alpha(V_G) \sim 1$

C/C$_{ox}$

$$V_{th}(V_G) = V_{th}^* + \frac{\alpha(V_G)Q_{ox}(x_0)}{C_{ox}}$$
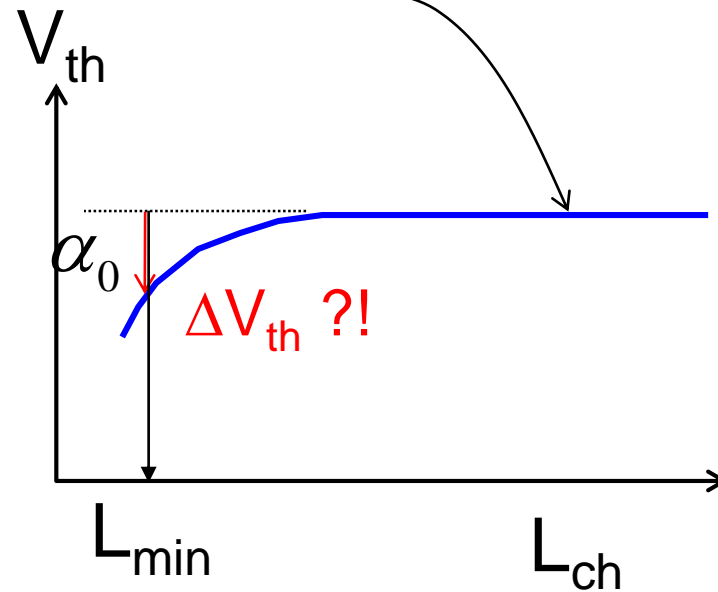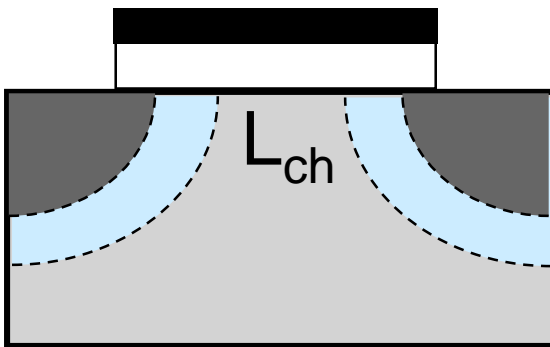
V_G

Acceptor and Donor Traps Combined

Donor-related
stretchout

Acceptor-related
stretchout

Short Channel Effect: V_{th} Roll-off

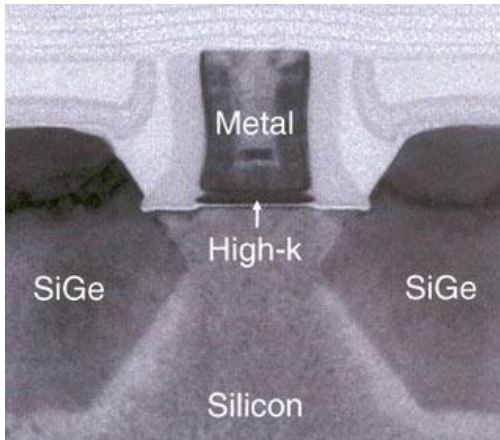$$V_{th} = 2\phi_F - \frac{Q_B}{C_{ox}} = 2\phi_F + \frac{qN_A W_T}{C_{ox}}$$

L_{ch}

V_{th}

α_0

ΔV_{th} ?!

L_{min} L_{ch}

How to reduce V_{th} roll-off ...

Shallow junction/geometry of transistors
laser annealing of junctions, FINFETs

Reduced substrate doping N_A
consider WT and junction breakdown

$$L_{\min} = \frac{qN_AW_T}{C_o} \frac{r_J}{\alpha_0} \left(\sqrt{1 + \frac{2W_T}{r_J}} - 1 \right)$$
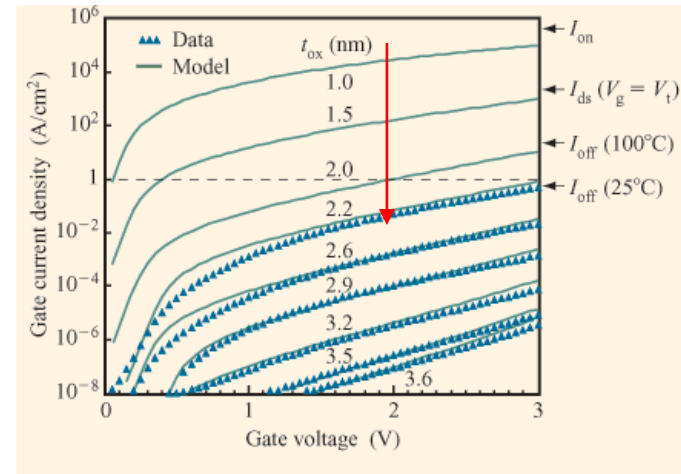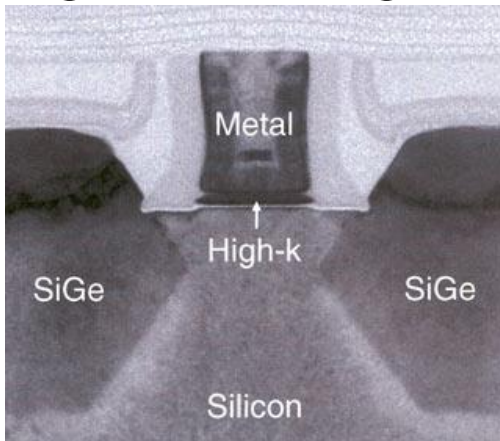
Thinner gate oxides
Consider tunneling current
Higher gate dielectric
Consider bulk traps

High-k/metal gate MOSFET

Advantages of High-k Dielectric
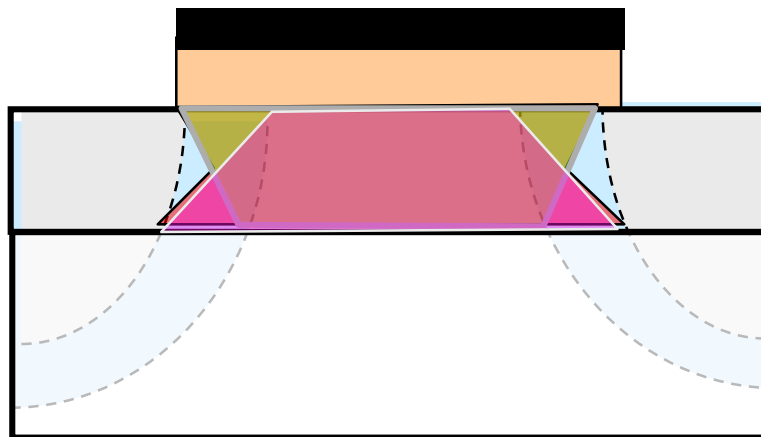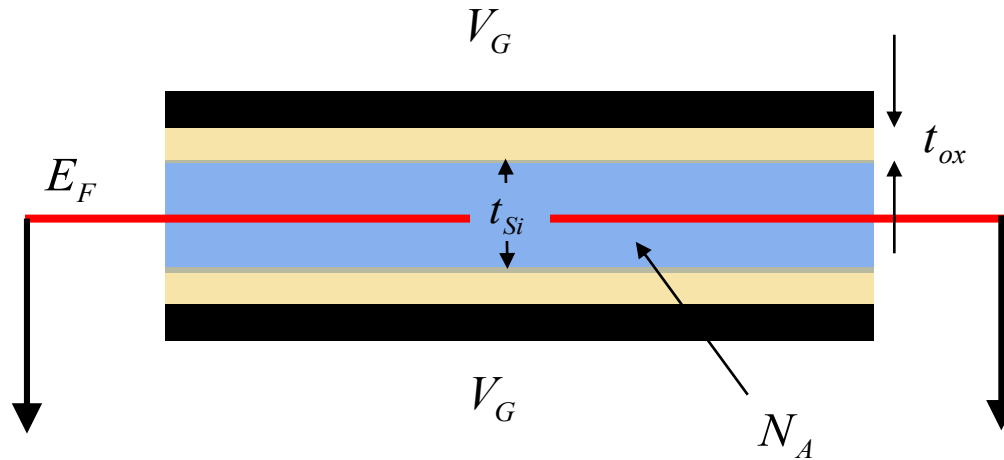
High-k/metal gate MOSFET ...

$$L_c = \frac{qN_AW_T}{\dfrac{\kappa_{ox}\varepsilon_0}{x_0}} \frac{r_J}{\alpha}\left(\sqrt{1+\frac{2W_T}{r_J}}-1\right)$$
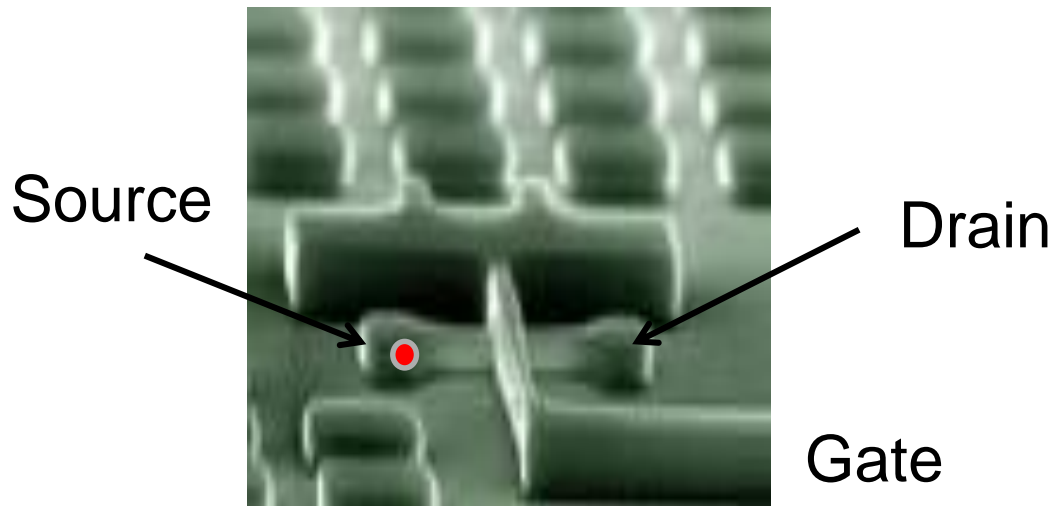
$$I_D = \frac{Z\mu C_o}{2L}(V_G - V_{T,ideal})^2$$

Thicker oxide (x_0) for same capacitance ...

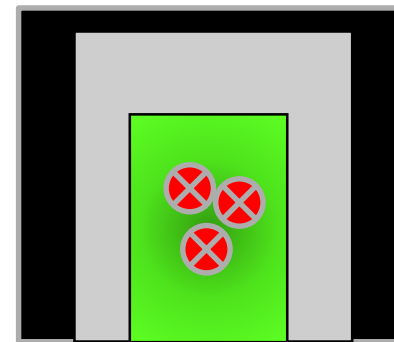... ensures the drive-current is not reduced , but tunneling current is suppressed.

Solution: Ultra-thin Body SOI

Example: FINFET, OmegaFET, X-FET

Source

Drain

Gate

Cross-section

Outline

1. Review from Tuesday

2. Velocity saturation in simplified theory

3. Major Failure Modes

   A. Bulk charge theory for small transistors

   B. Bias Temperature Instability

   C. Short Channel Effects

4. **Conclusion**

Conclusion

1) Ideal and non-ideal MOSFETs currents above threshold can be predicted using a simplified bulk-charge theory

2) There are a variety of failure modes that can degrade performance over time: particularly dielectric breakdown and negative-bias temperature instability

3) Short channel effects are a serious concern for MOSFET scaling, and novel approaches have been proposed to solve them. Fortunately, electrons travel from source to drain without scattering in very short channel transistors. A considerably simpler theory applies here.