ECE-305: Spring 2018
Exam 4 Review

Pierret, *Semiconductor Device Fundamentals* (SDF)
MOSCAPs and MOSFETs: Chapters 15-18

Professor Peter Bermel
Electrical and Computer Engineering
Purdue University, West Lafayette, IN USA
pbermel@purdue.edu

Key Principles in MOS devices

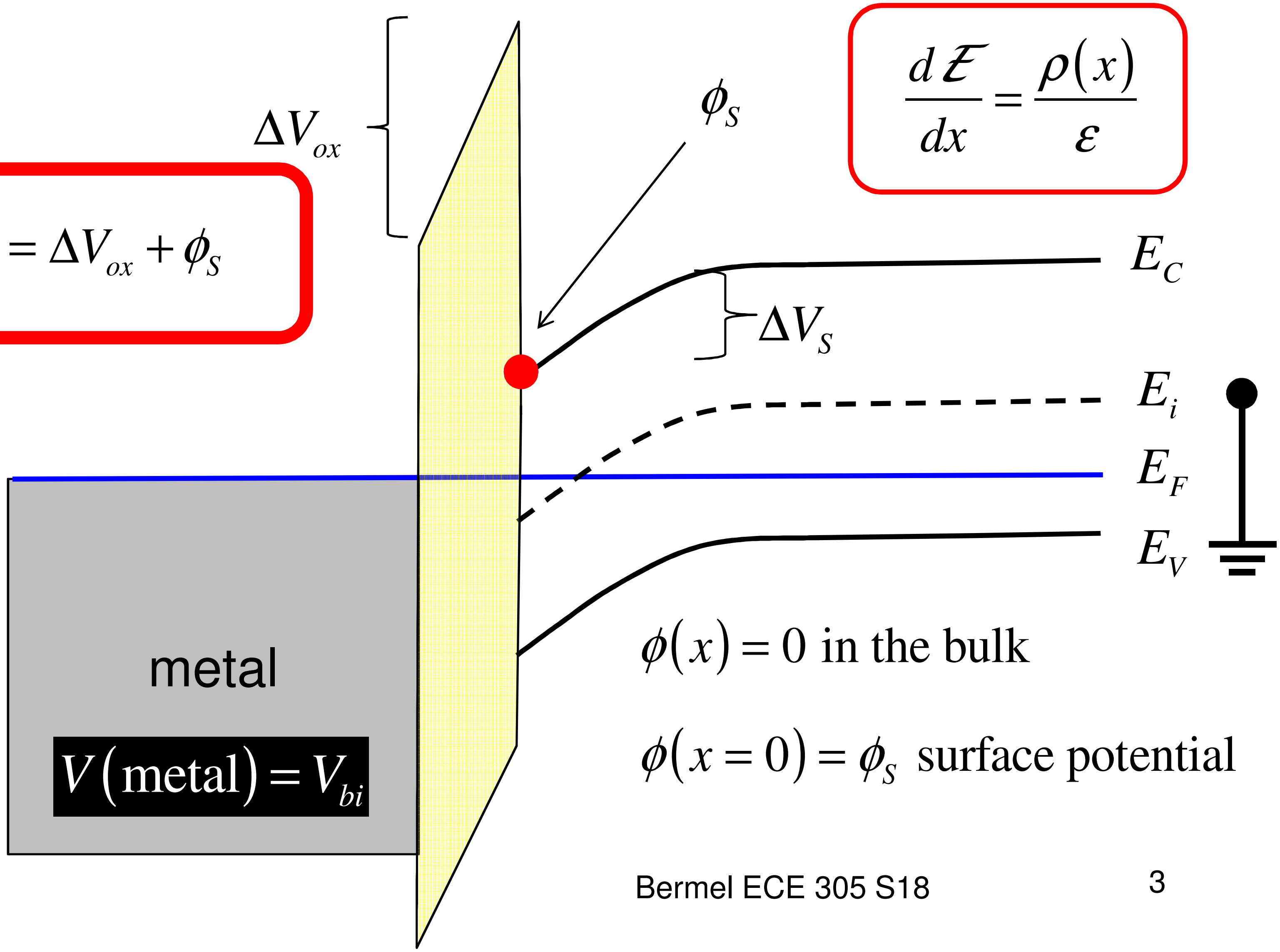
- MOS geometry & band bending
- MOS junction capacitance
- MOSFET geometry
- MOSFET transfer and output characteristics
- MOSFET square law and saturation
- MOSFET reliability and variability
- MOSFET new materials

equilibrium MOS band diagram

$$\frac{d\mathcal{E}}{dx} = \frac{\rho(x)}{\varepsilon}$$

$$V(\text{metal}) = \Delta V_{ox} + \phi_S$$

$$V_{bi} = -\phi_{ms}$$



$\phi(x) = 0$ in the bulk

$\phi(x=0) = \phi_S$ surface potential

band bending in p-type MOS

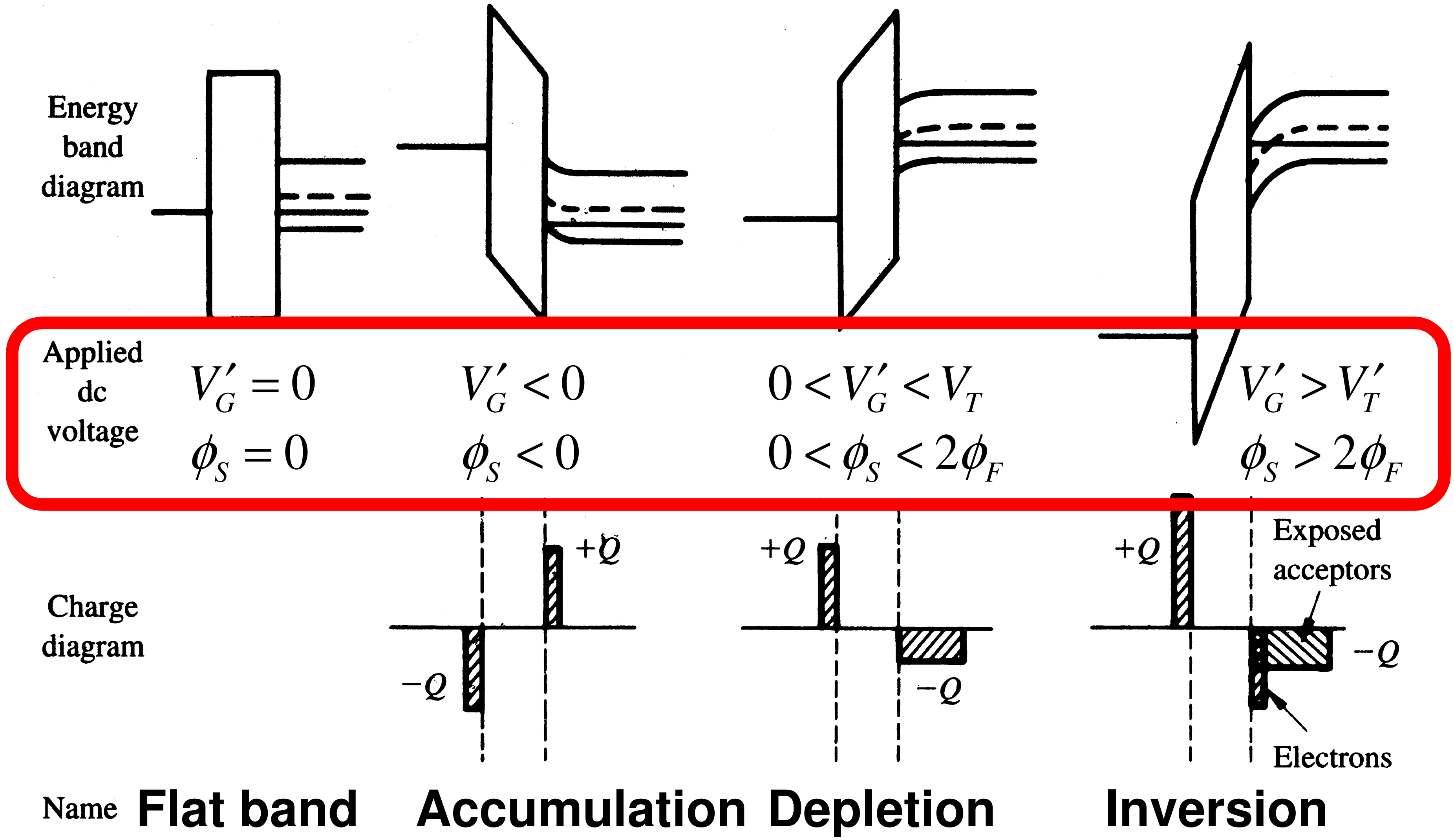
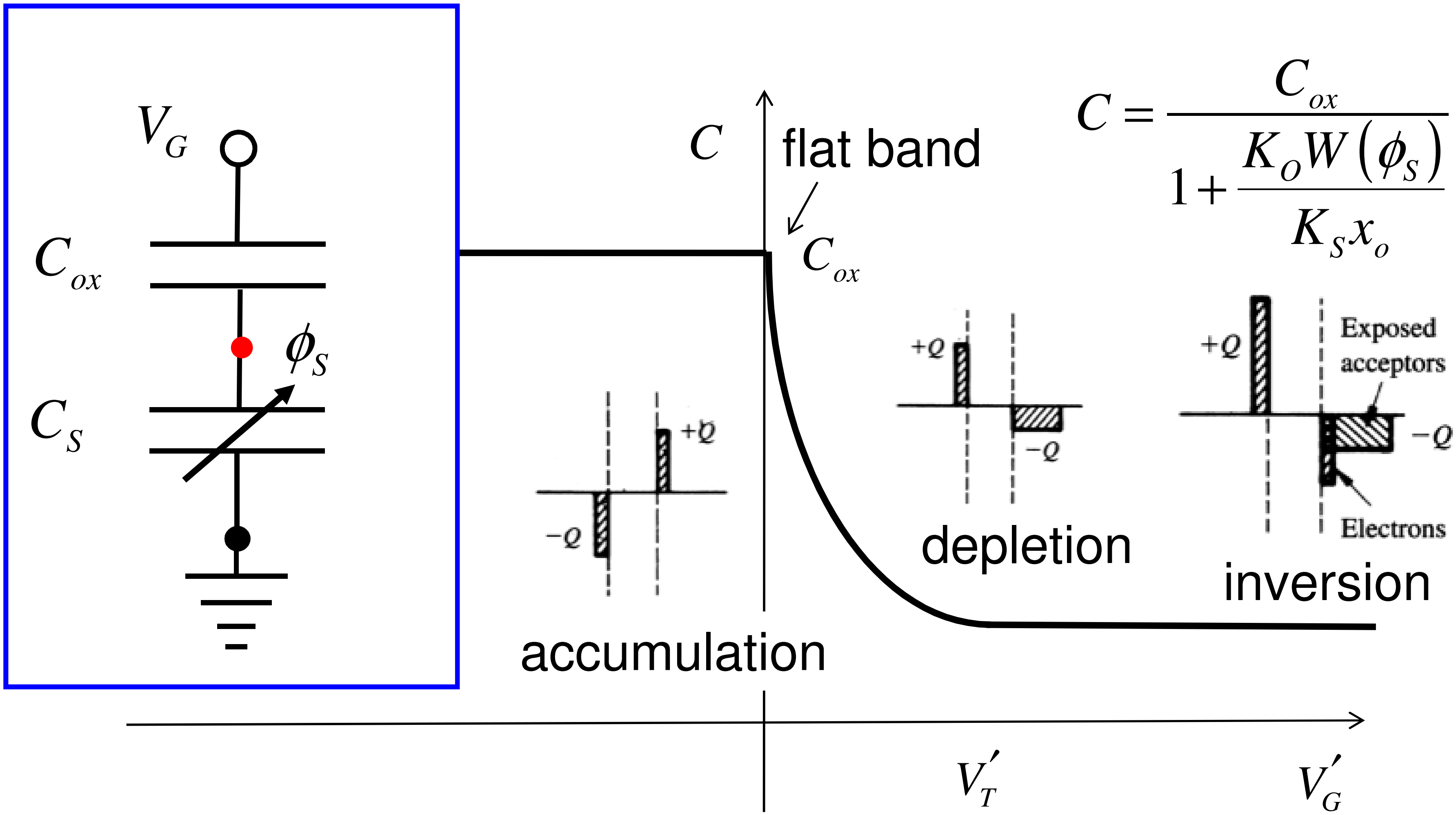


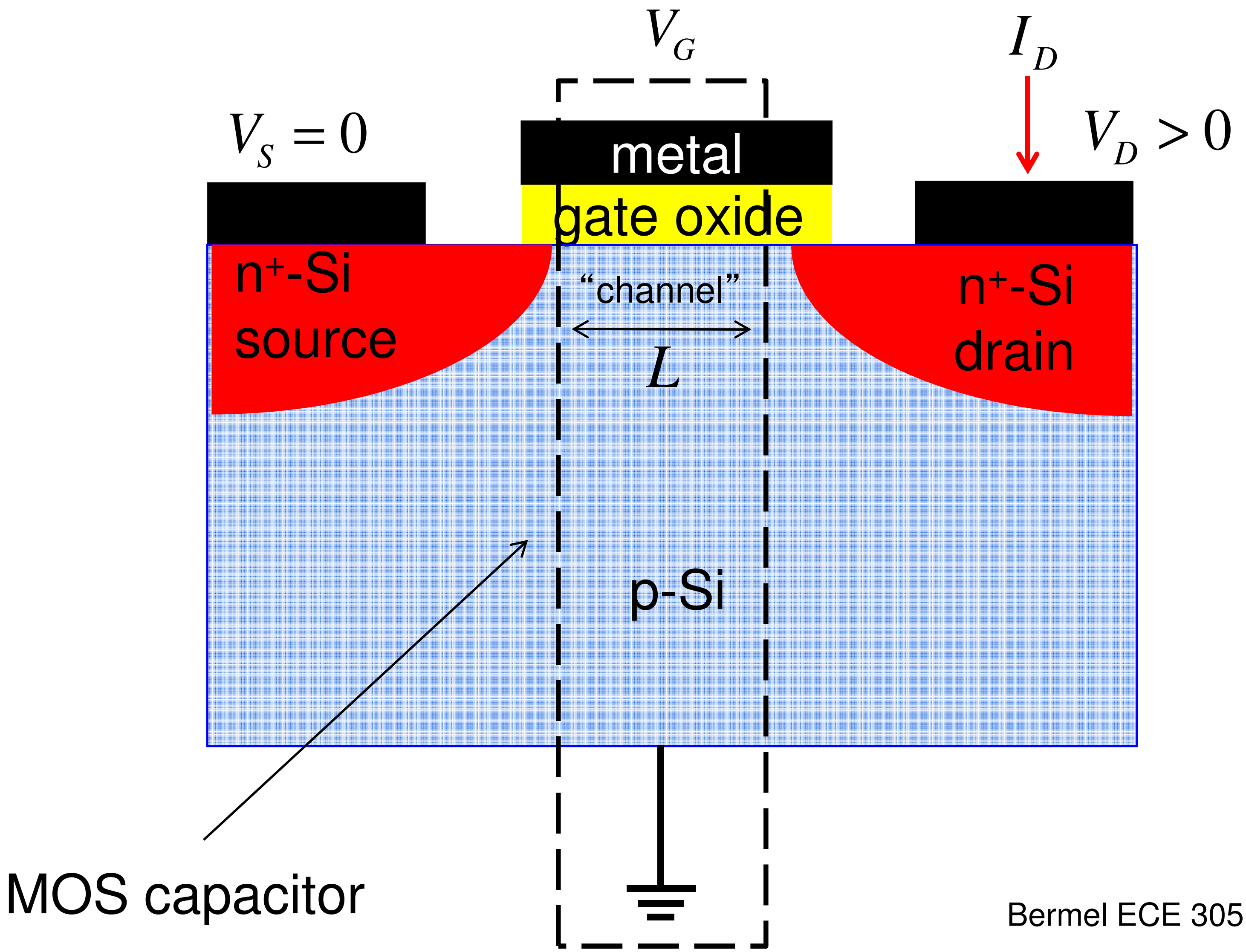
Fig. 16.6, Semiconductor Device Fundamentals, R.F. Pierret

s.s. gate capacitance vs. d.c. gate bias

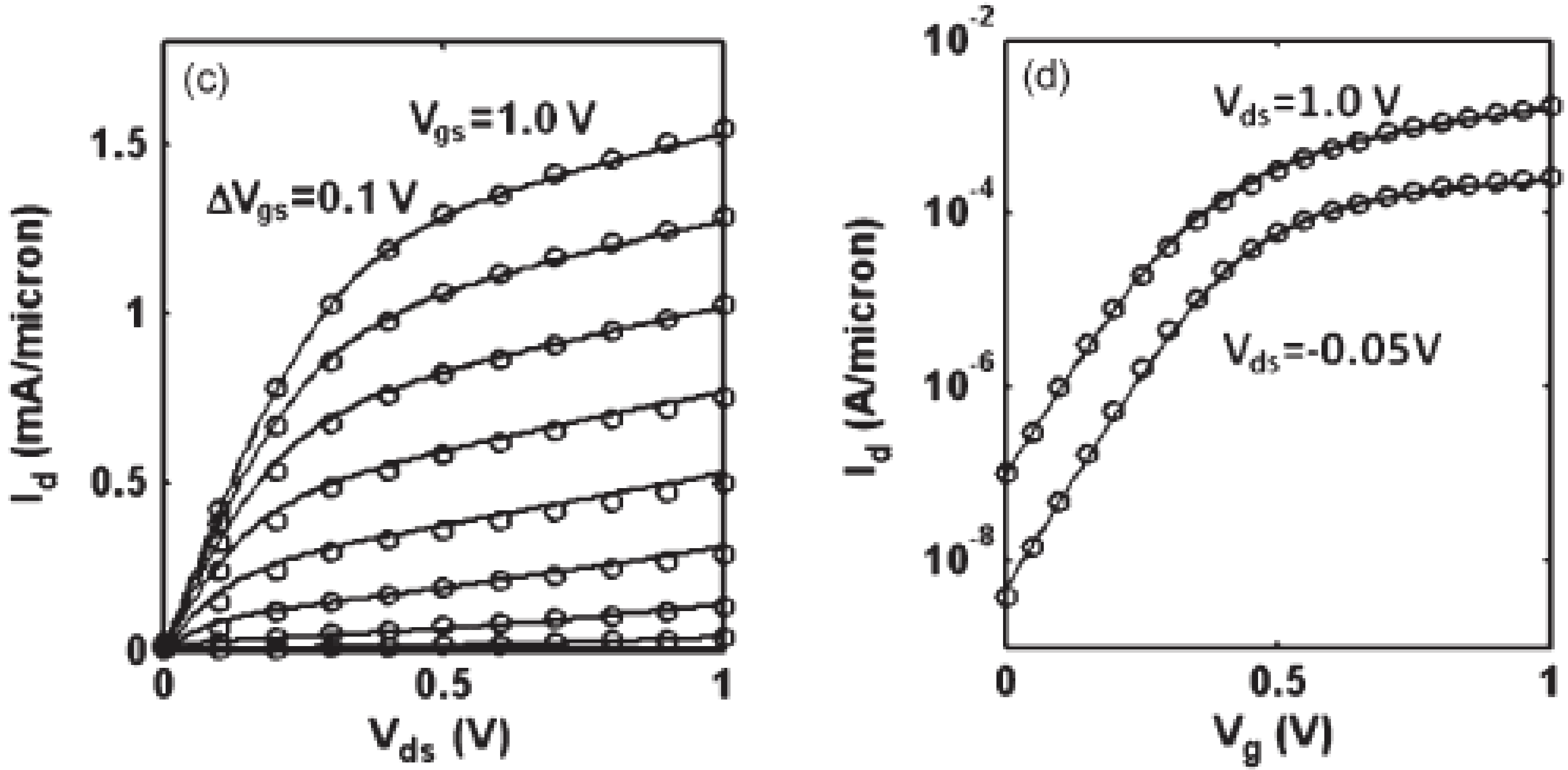


$$C = \frac{C_{ox}}{1 + \frac{K_O W(\phi_S)}{K_S x_o}}$$

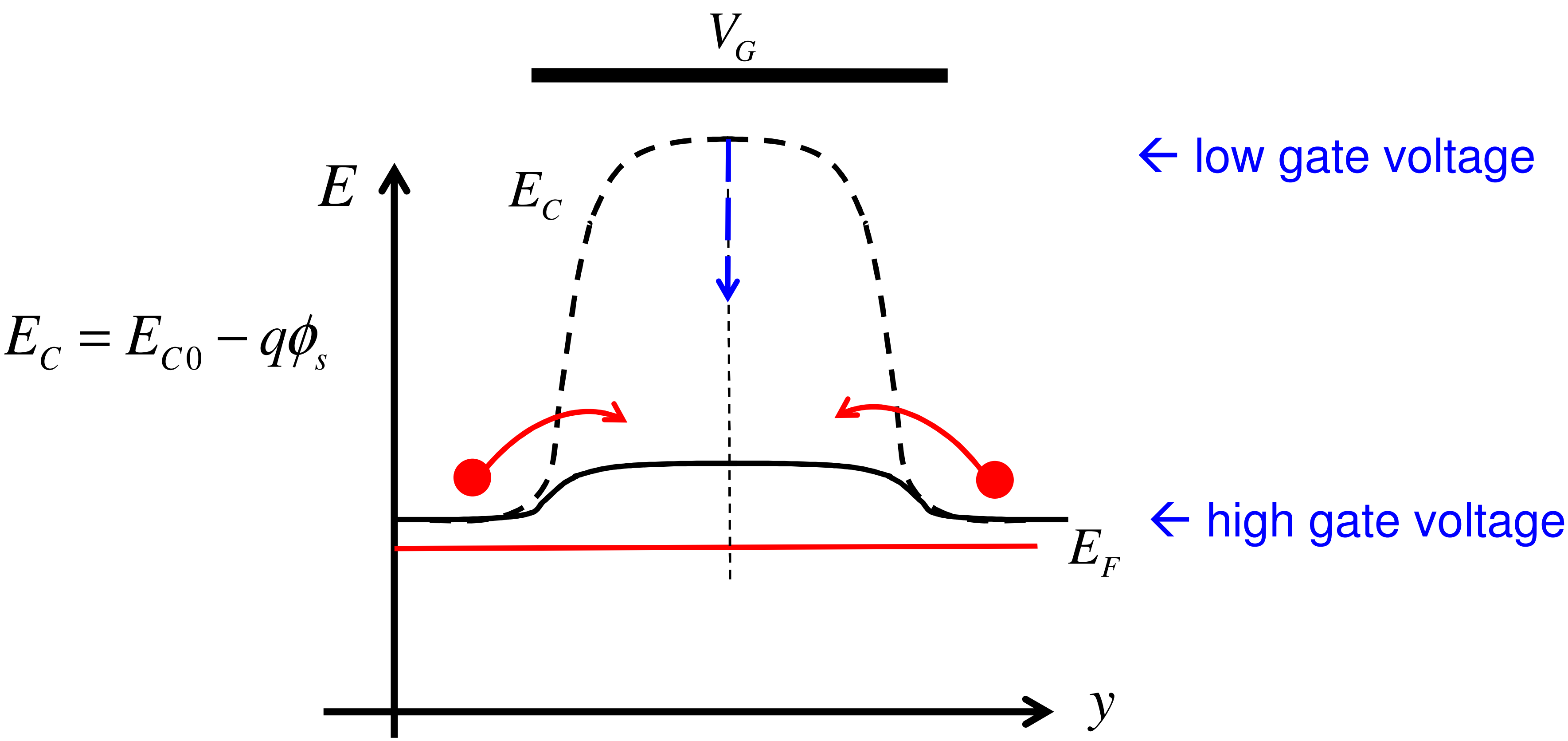
MOSFET Geometry



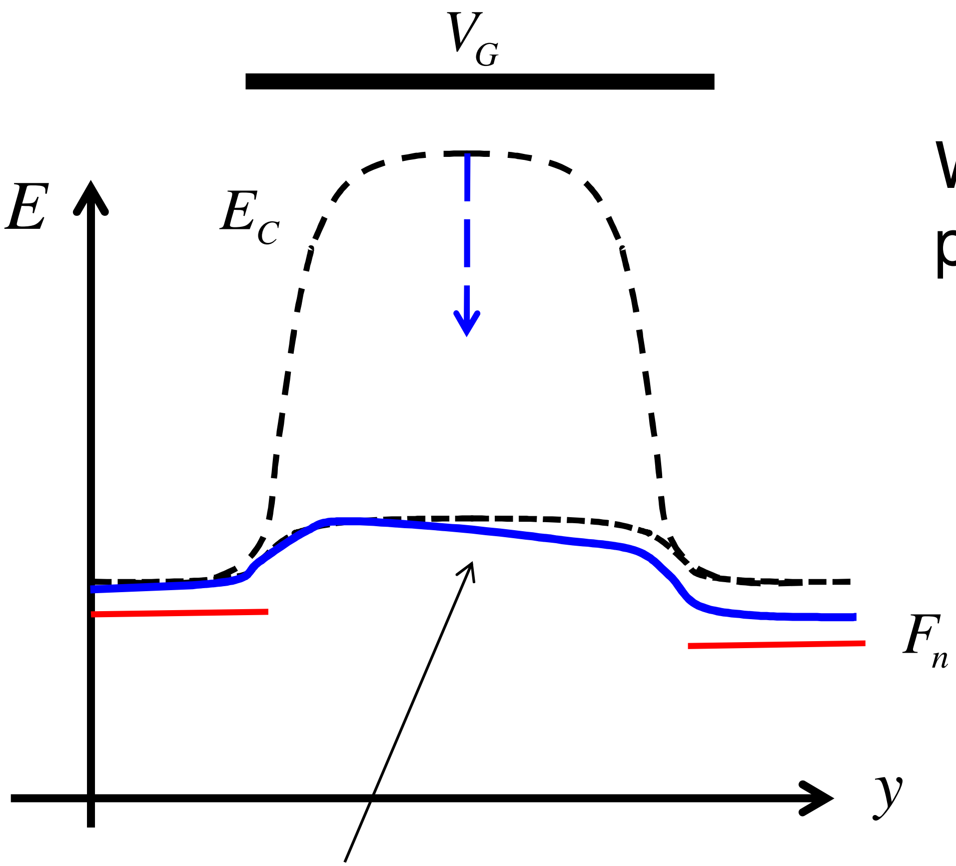
Example: 32 nm N-MOSFET technology



the MOSFET is a barrier controlled device: effects of gate voltage



the MOSFET is a barrier controlled device: effects of a small drain voltage



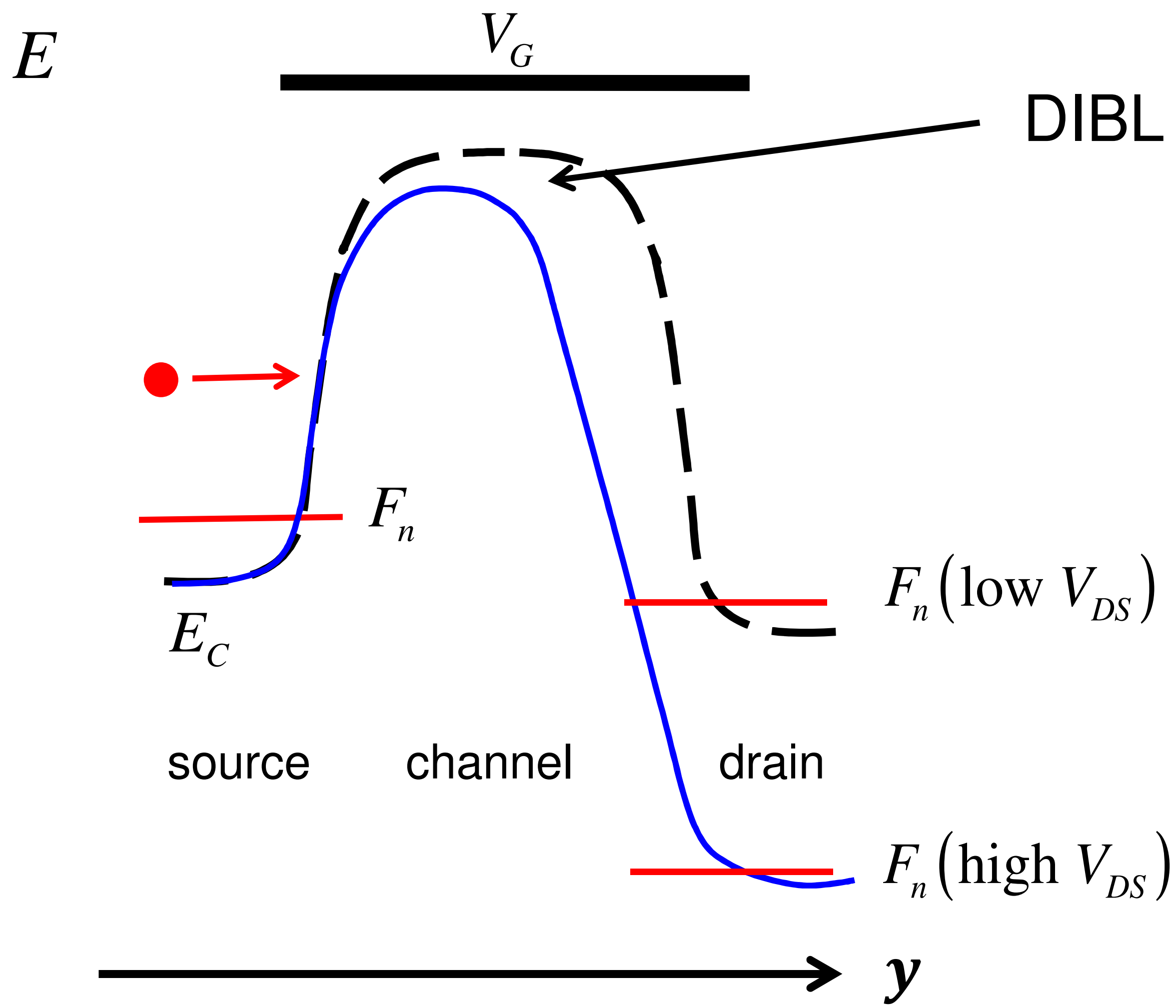
constant electric field
substantial electron density

What if we apply a small positive voltage to the drain?

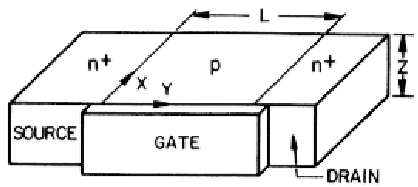
1) The Fermi level in the drain is lowered.

2) The conduction band is lowered too, but the electron density stays the same.

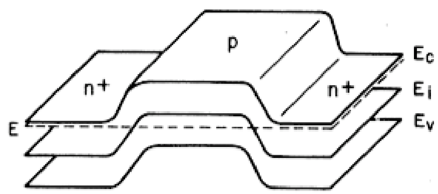
understanding DIBL



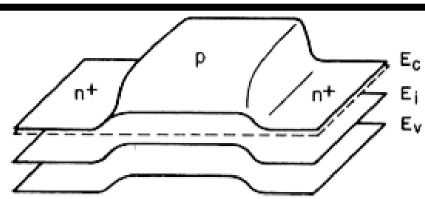
2D energy band diagram on n-MOSFET



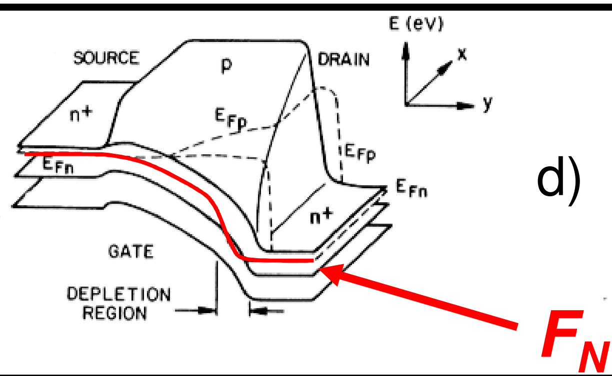
a) device



b) equilibrium (flat band)



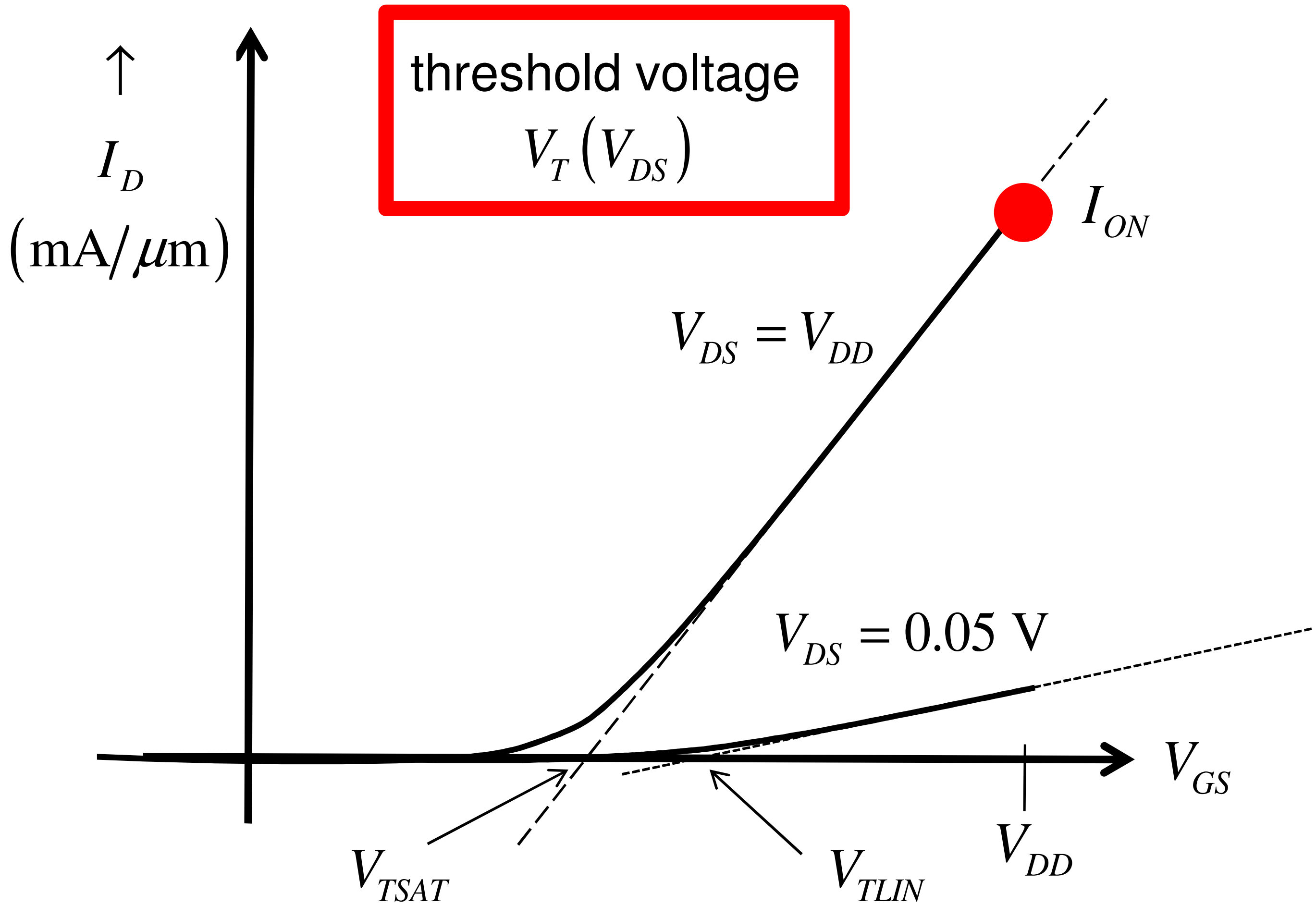
c) equilibrium ($\phi_S > 0$)



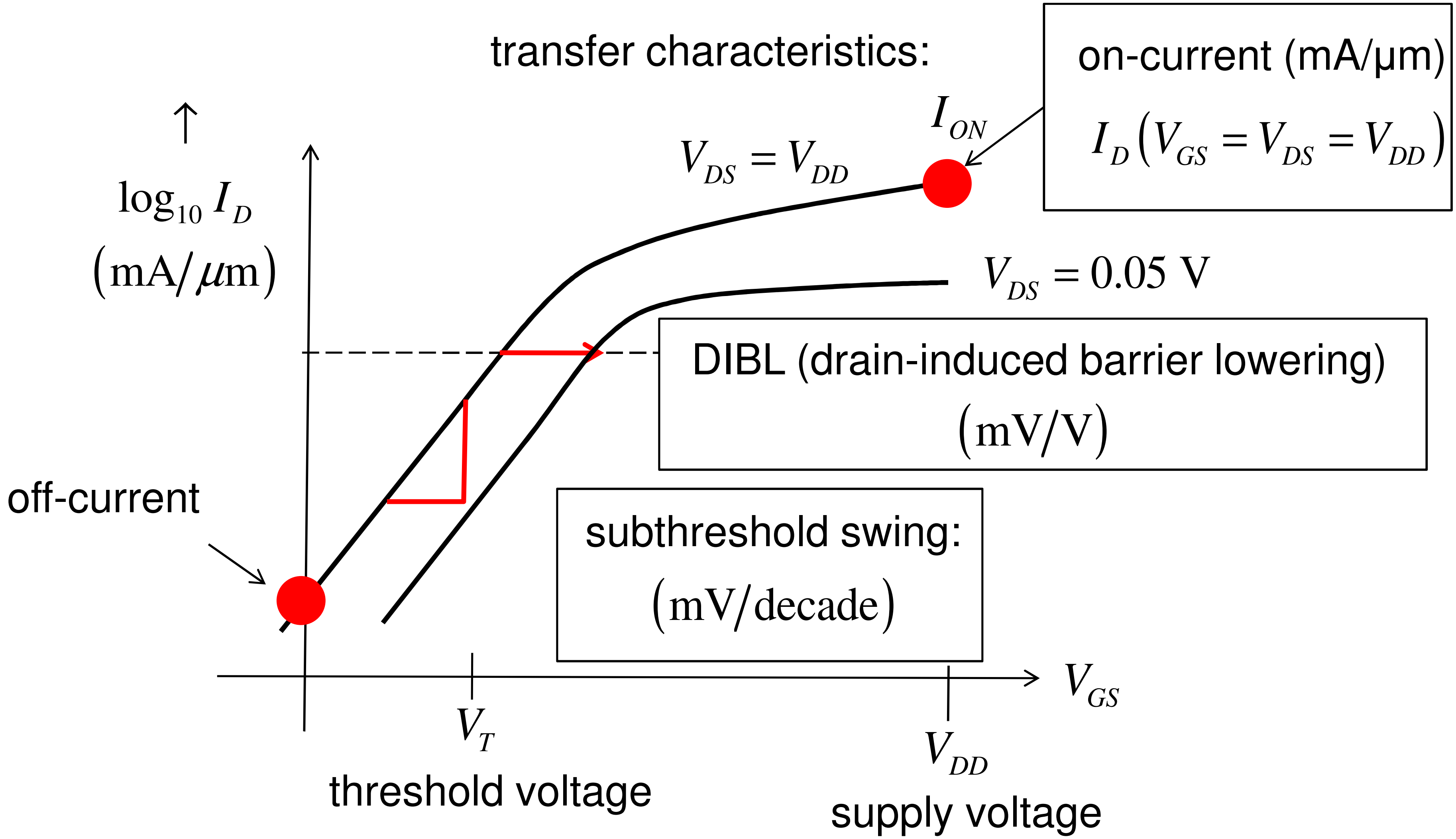
d) non-equilibrium with V_G and $V_D > 0$ applied

S.M. Sze, Physics of Semiconductor Devices, 1981 and Pao and Sah.

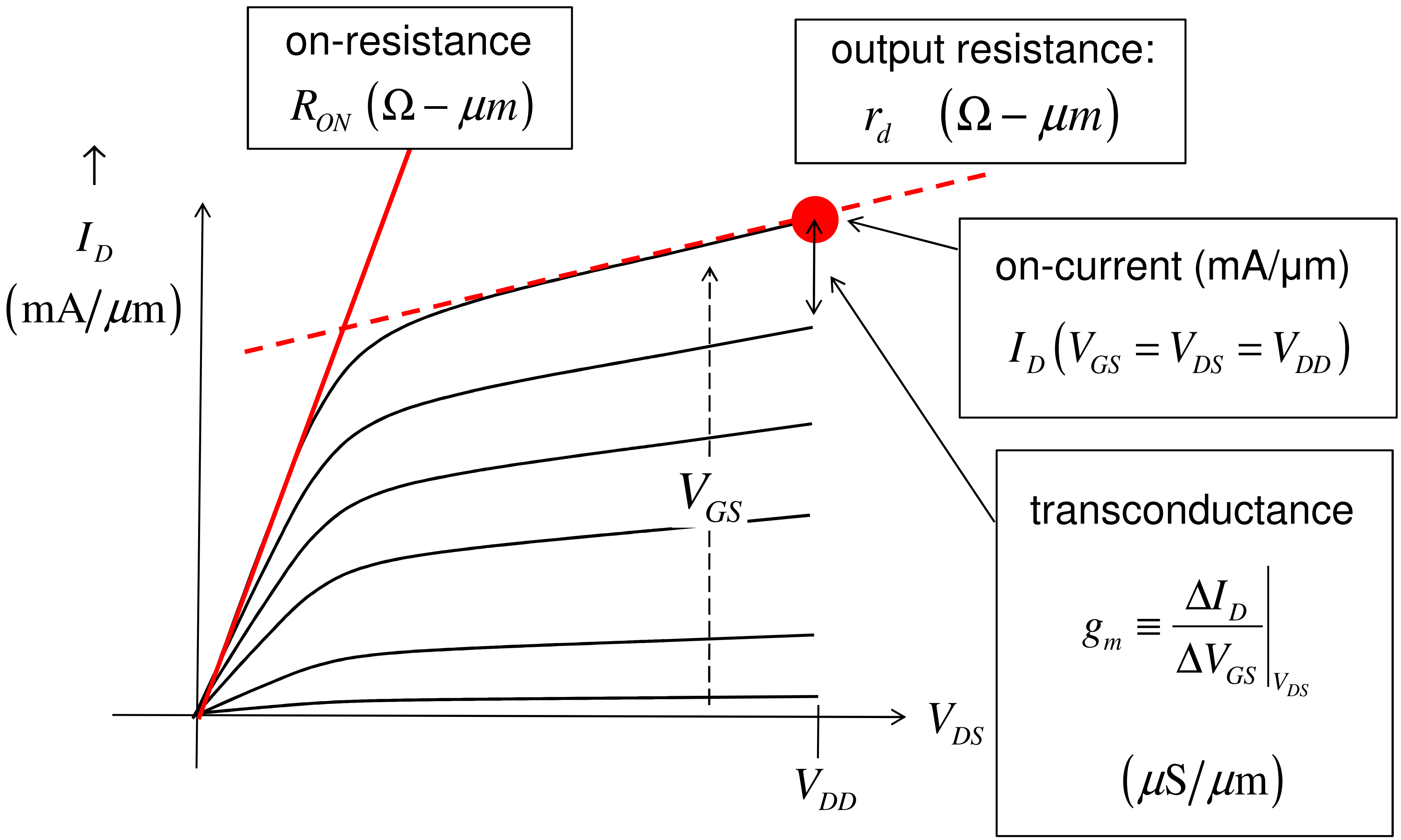
understanding DIBL



MOSFET device metrics



MOSFET device metrics



definition of body coefficient (*m*)

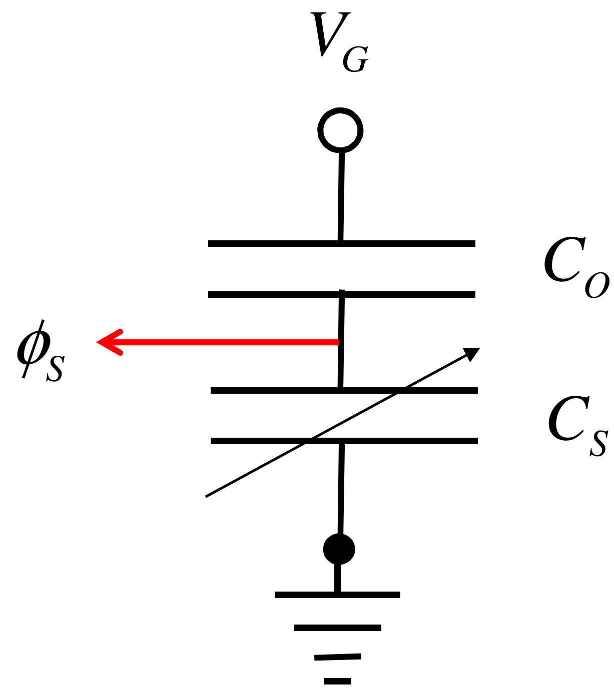
$$m \equiv \left(1 + C_S / C_O\right)$$

'Body Effect Coefficient'

$$m = \left(1 + K_S x_O / K_0 W_T\right)$$

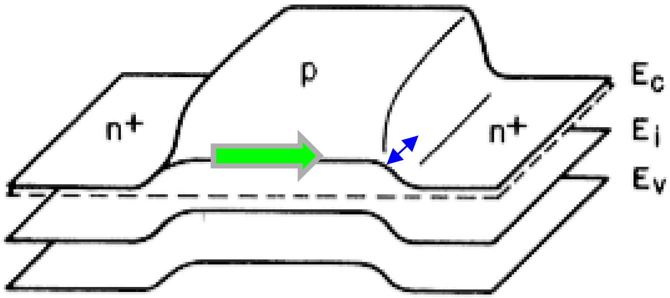
in practice:

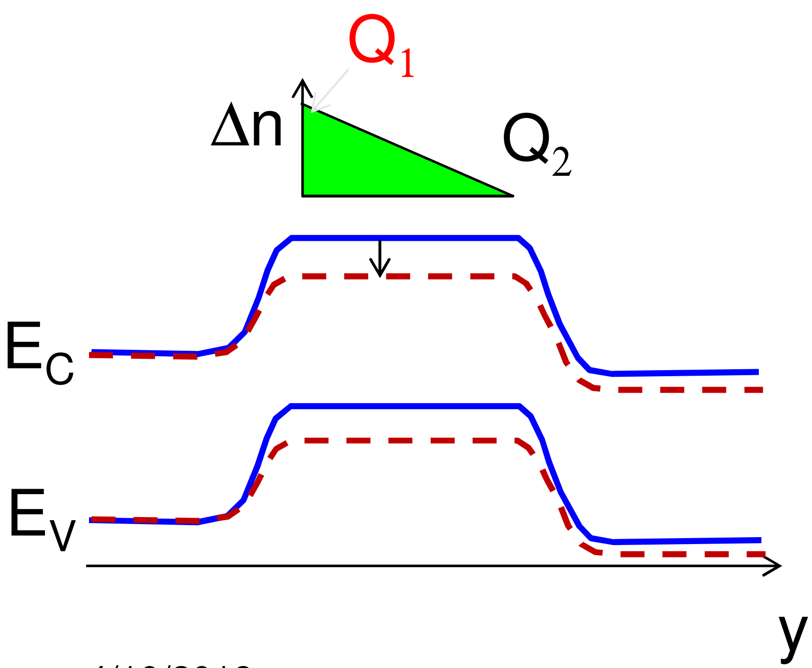
$$1.1 \le m \le 1.4$$

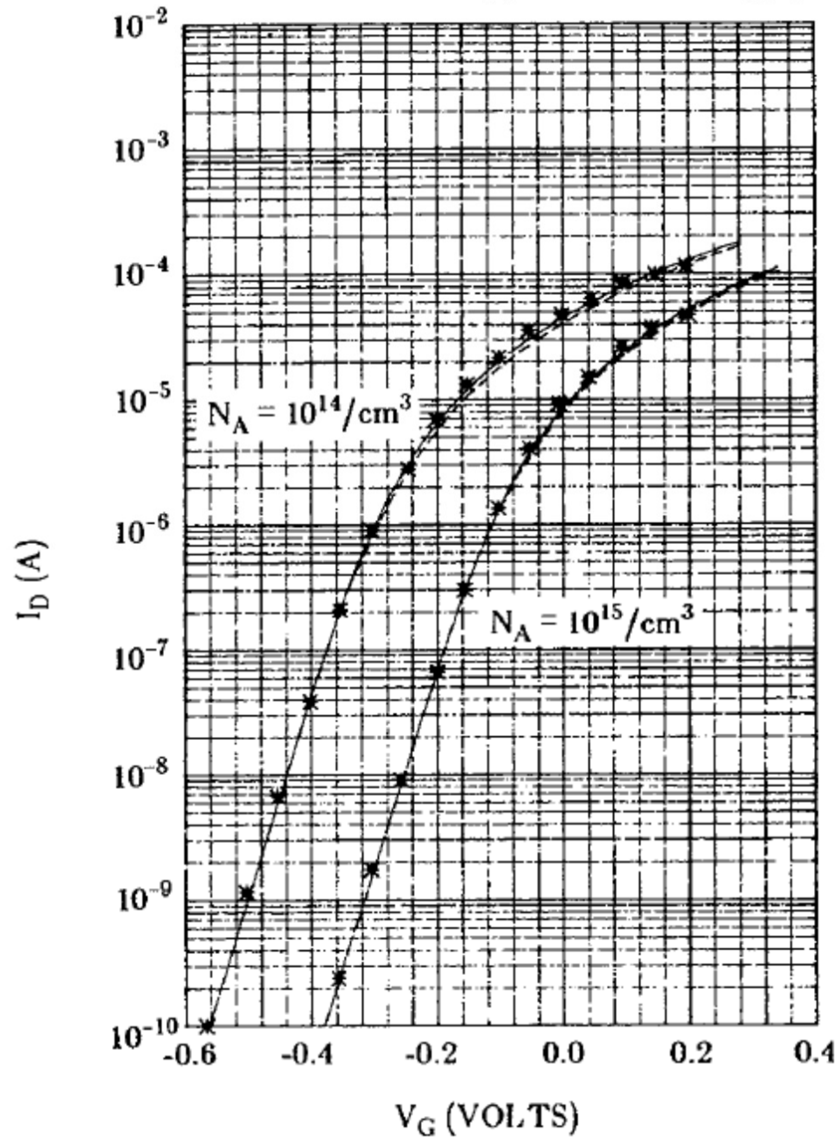


$$\phi_S = \frac{C_O}{C_O + C_S} V_G \equiv \frac{V_G}{m}$$

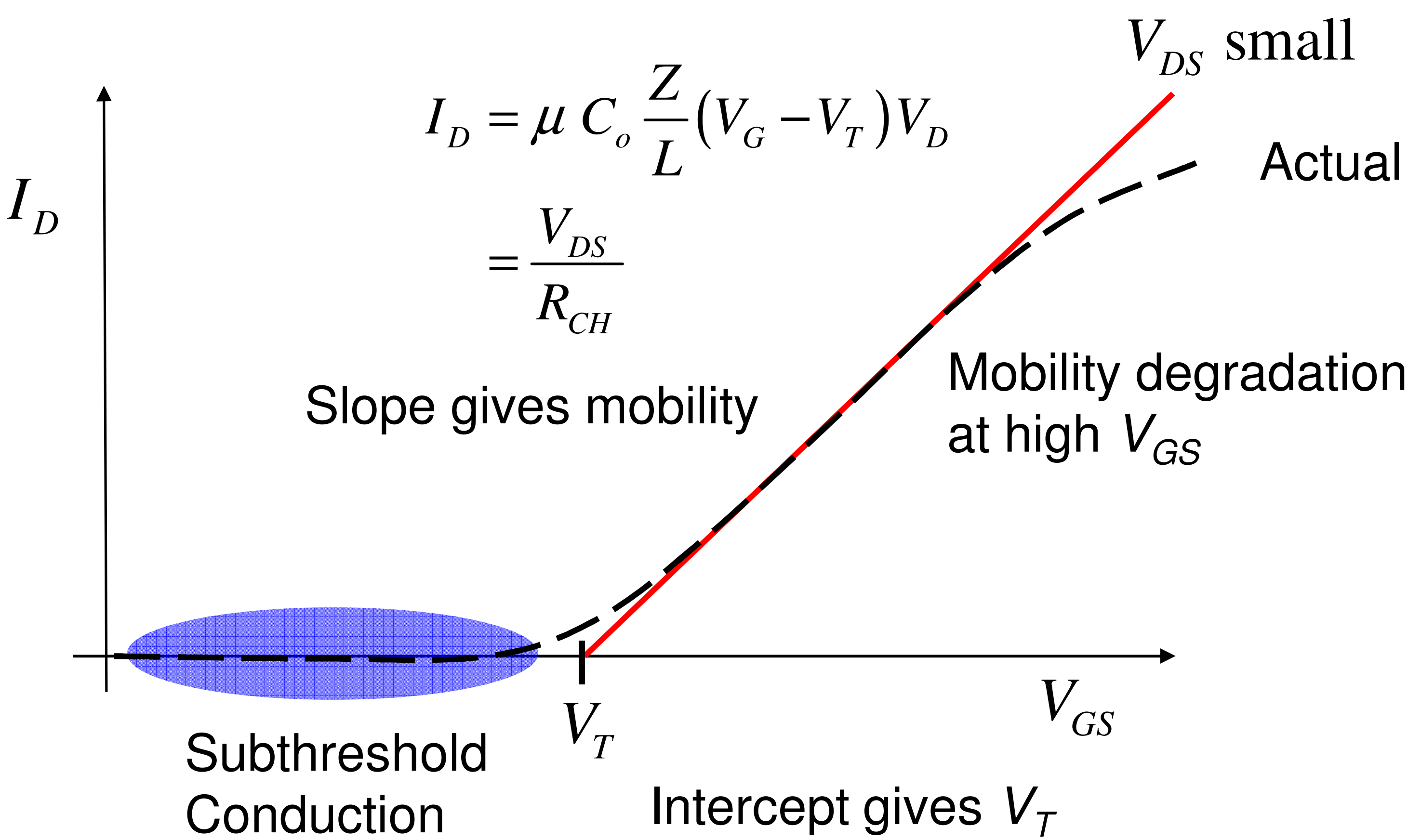
Subthreshold Region ($V_G < V_{th}$)







Linear Region (Low V_{DS})



Post-Threshold MOS Current ($V_G > V_{th}$)

$$I_D = -\frac{W}{L_{ch}} \mu_{eff} \int_0^{V_{DS}} Q_i(V)\, dV$$

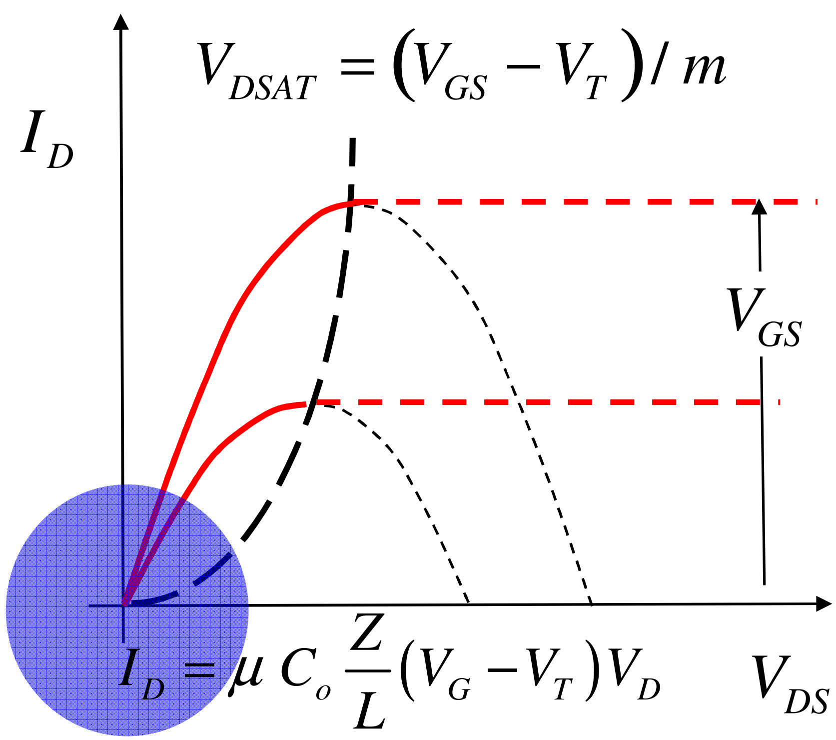
1) Square Law $\quad Q_i(V) = -C_G \left[V_G - V_T - V \right]$

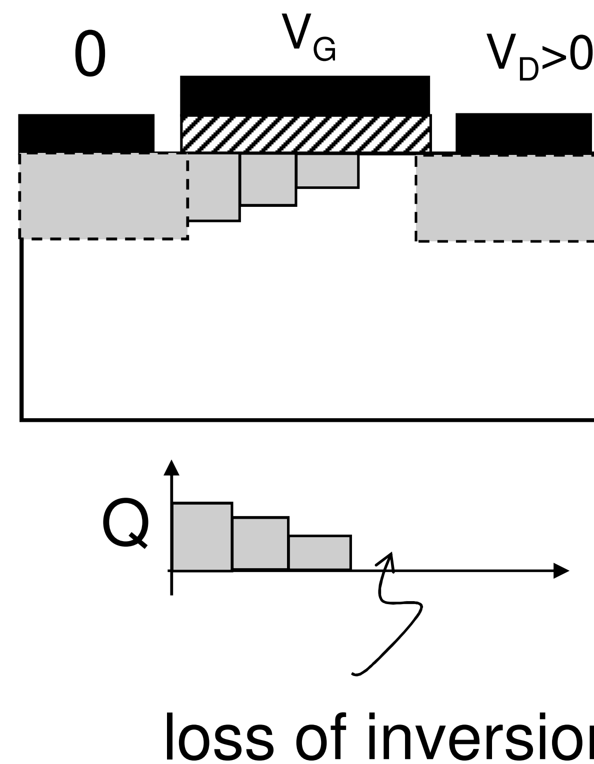
2) Simplified Bulk Charge $\quad Q_i(V) = -C_G \left[V_G - V_T - mV \right]$

Why does the curve roll over?

$$I_D = \frac{W\mu C_o}{2mL}\left(V_G - V_T\right)^2$$

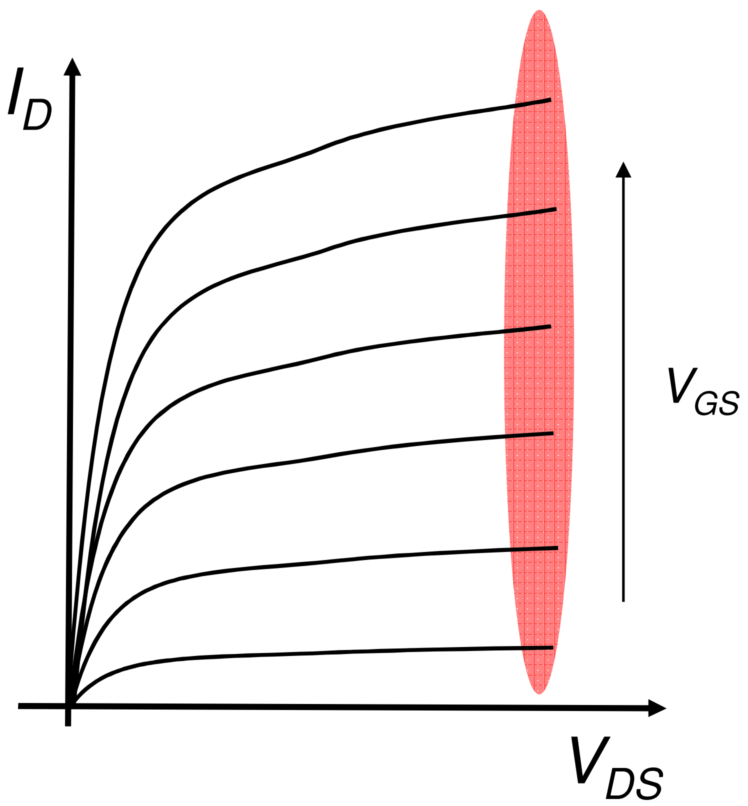
$$Q_i \approx -C_o\left(V_G - V_T - mV\right)$$





I_D and $(V_{GS} - V_T)$: In practice

……



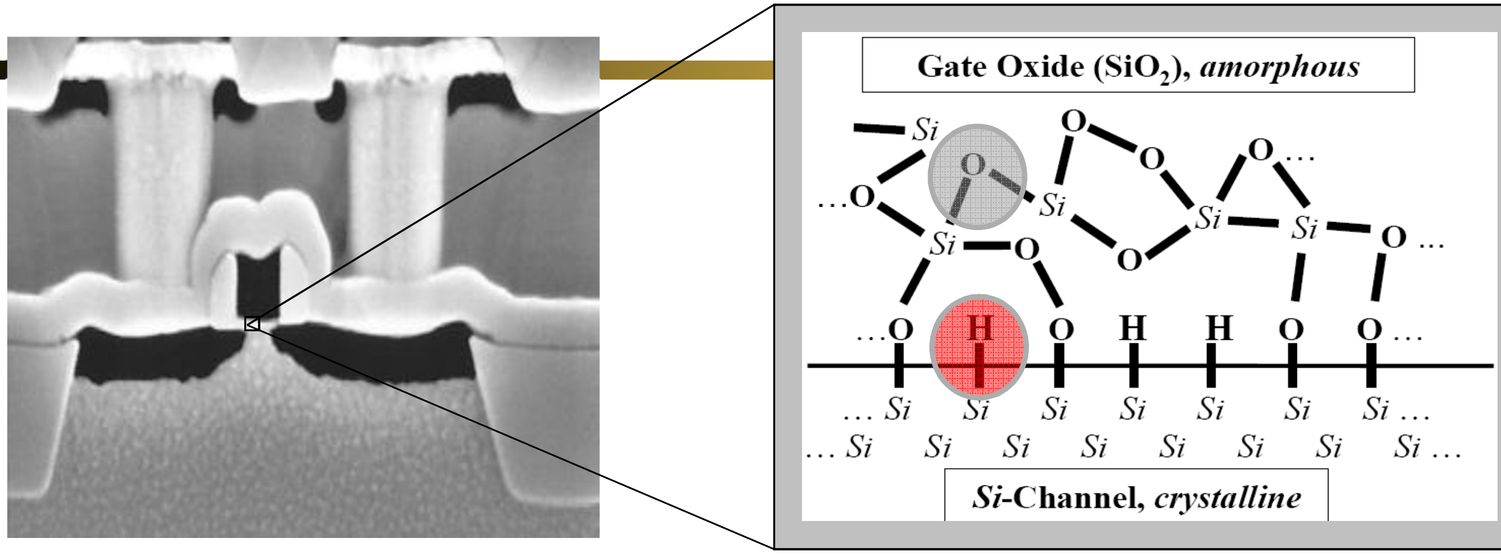
$$I_D(V_D = V_{DD}) \sim (V_G - V_T)^\alpha$$

$$1 < \alpha < 2$$

Complete velocity saturation

Long channel

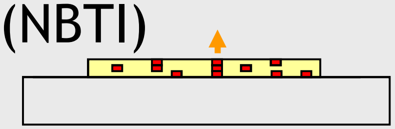
Failure mechanisms



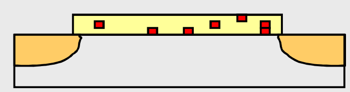
Broken Si-H bonds

Negative Bias Temperature Instability (NBTI)

Hot carrier degradation (HCI)



Broken Si-O bonds

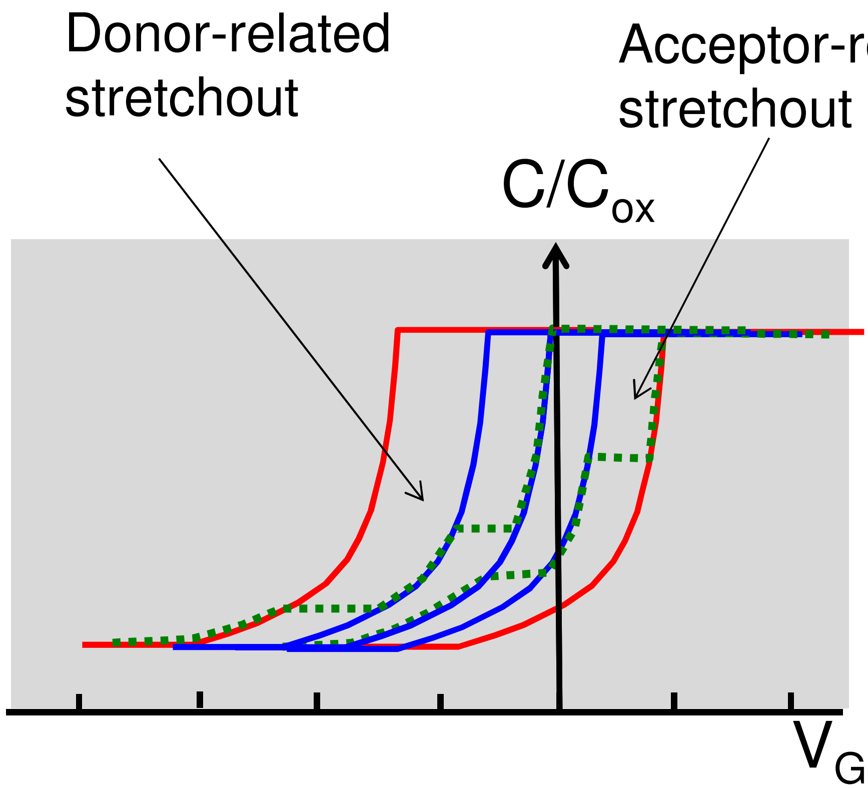


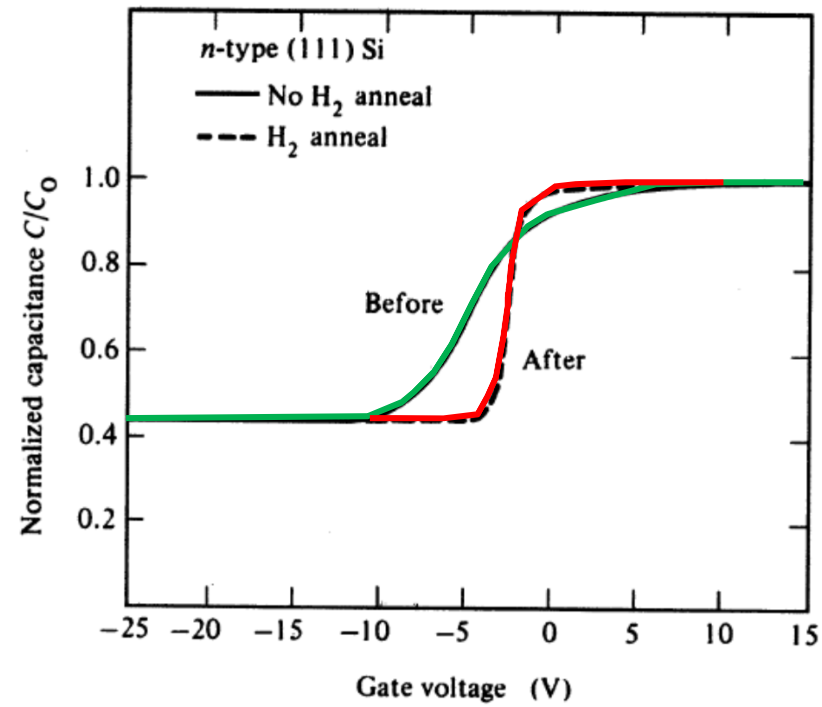
Gate dielectric Breakdown (TDDB)

Electrostatic Discharge (ESD)

Radiation induced Gate Rupture (RBD)

Threshold shifts



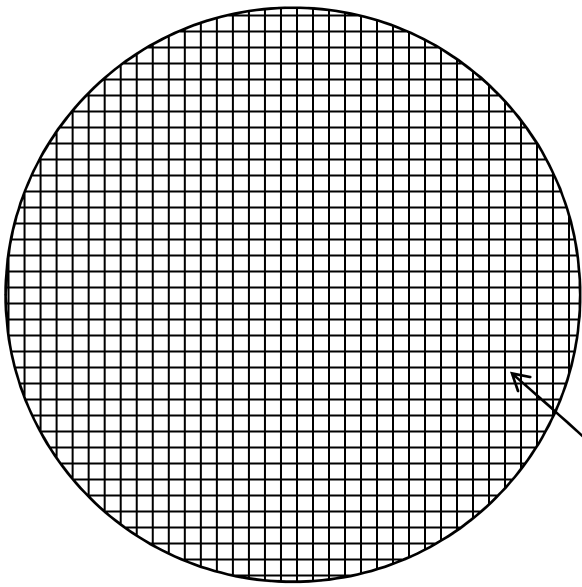


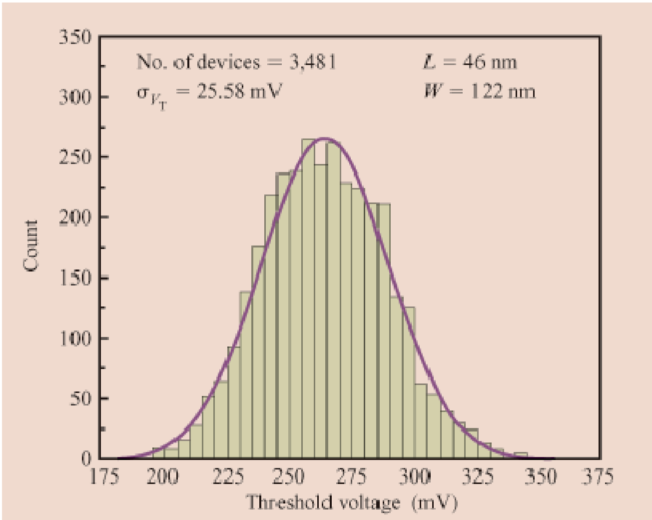
$$V_T = V_{T,ideal} - \frac{x_1}{x_o}\frac{Q_M}{C_o}$$

Variability in Threshold Voltage

$$V_{th} = 2\phi_F - \frac{Q_B}{C_{ox}} = 2\phi_F + \frac{qN_A W_T}{C_{ox}}$$

$$\sigma_{V_T} = 3.19 \times 10^{-8} \left(\frac{t_{ox} N_A^{0.4}}{\sqrt{L_{eff} W_{eff}}} [V] \right),$$



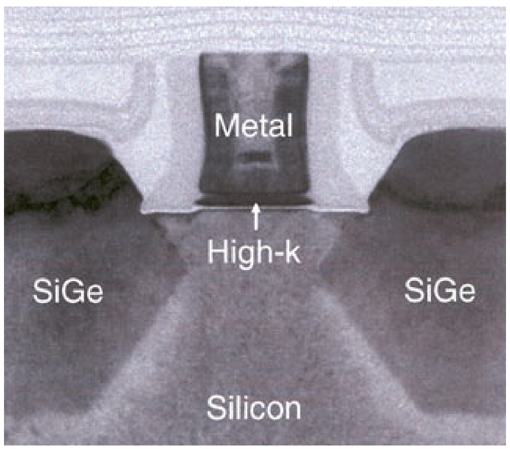


If every transistor has different V_{th} and therefore different current, circuit design becomes difficult

$$I_D = \frac{Z\mu C_o}{2L}(V_G - V_{T,ideal})^2$$

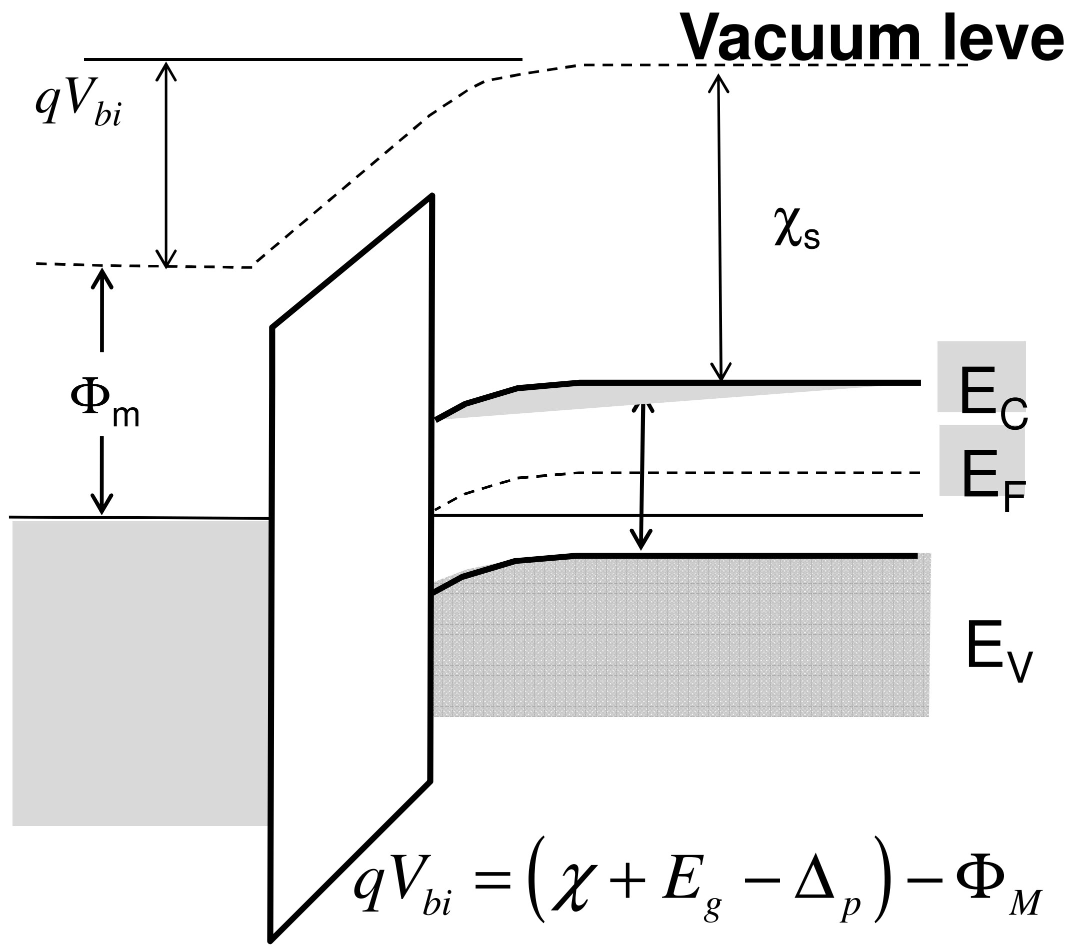
V_{th} control by Metal Work-function

High-k/metal gate MOSFET



$$Q_i = C_o (V_G - V_T)$$

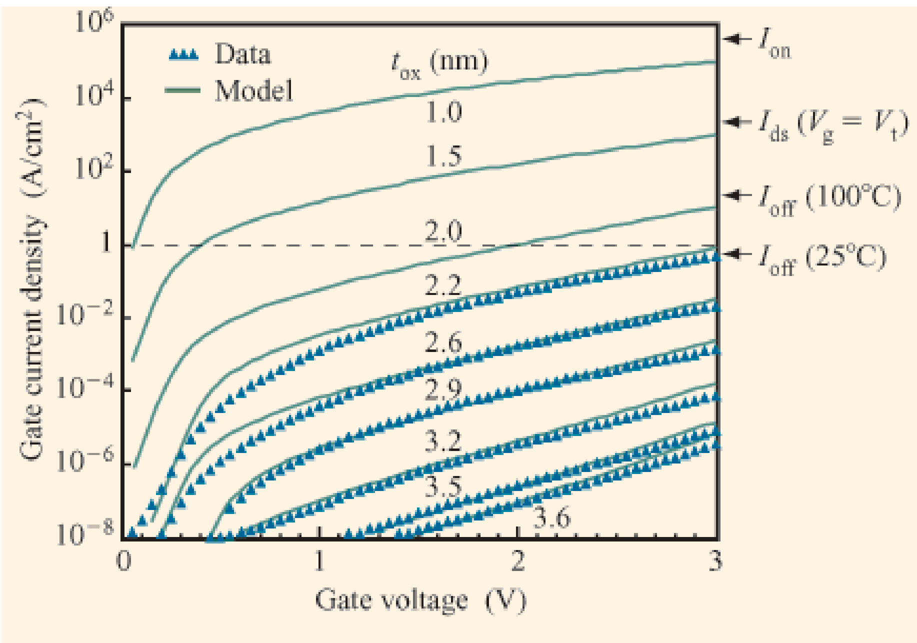
$$V_T = -V_{FB} + \left(\phi_s - \frac{Q_B}{C_o} \right)$$

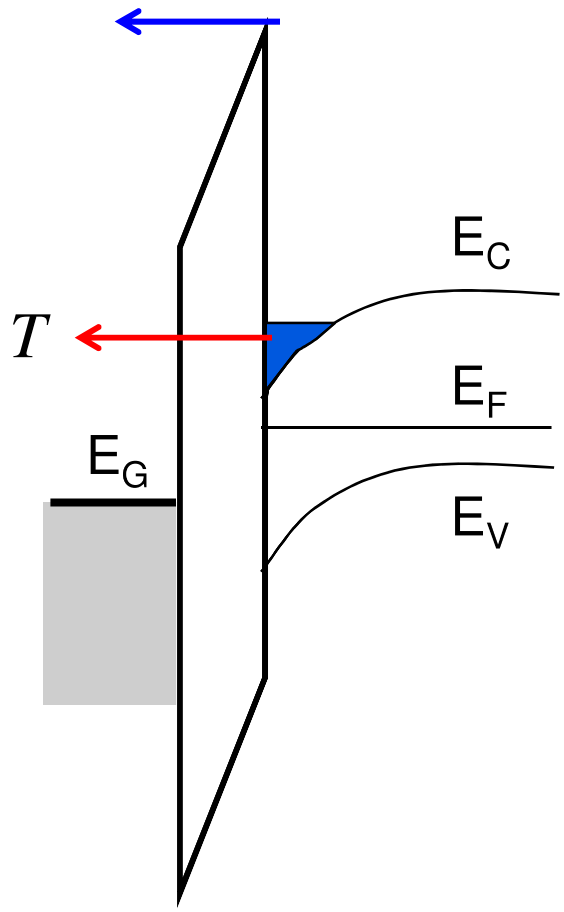


$$qV_{bi} = \left(\chi + E_g - \Delta_p \right) - \Phi_M$$
$$= qV_{FB}$$

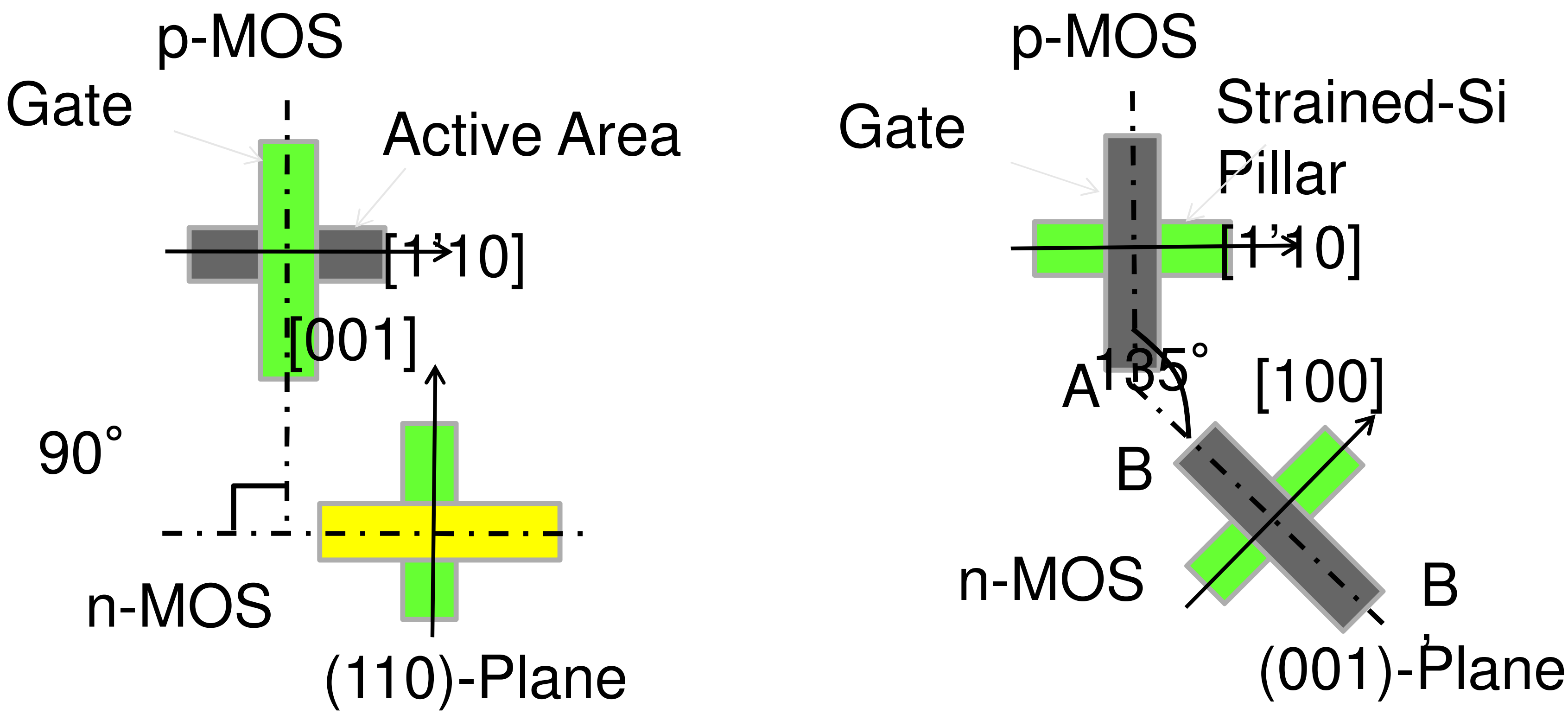
Tunneling Current

$$J_T = \left[Q_i(V_G) - \frac{n_i^2}{N_A} e^{-qV_G\beta} \right] \upsilon_{th} \langle T(E) \rangle$$



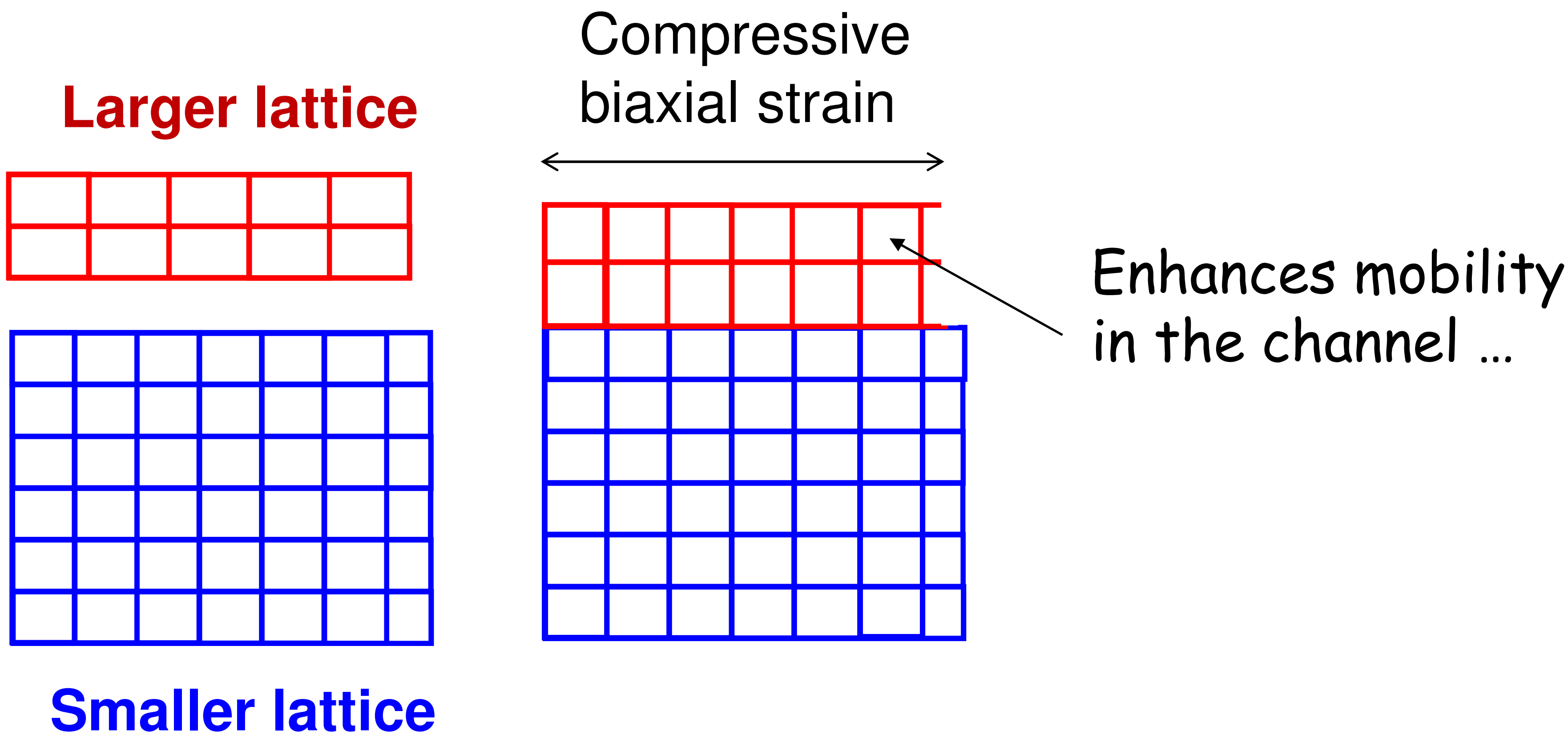


Ge for PMOS, Si for NMOS

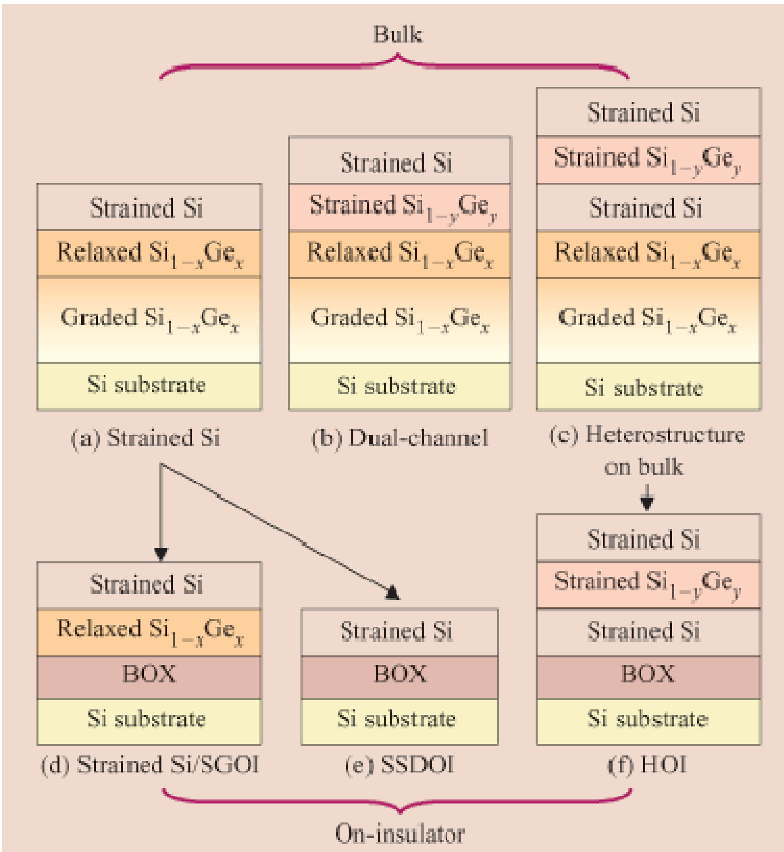


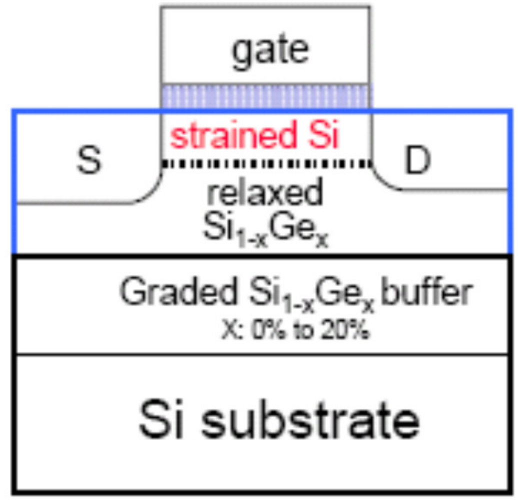
Takagi, TED 52, p.367, 2005

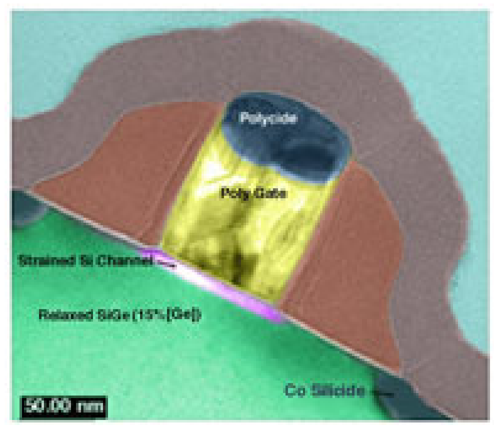
Basics of Strain ..



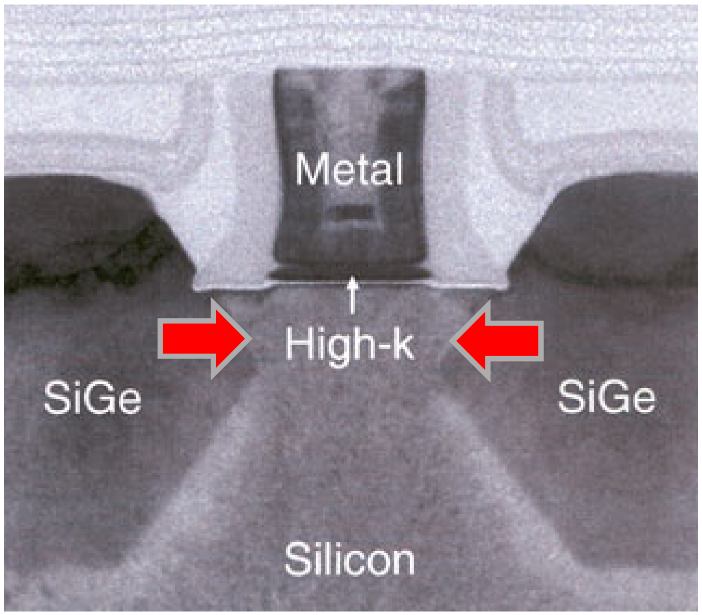
Biaxial Strain to Enhance Mobility



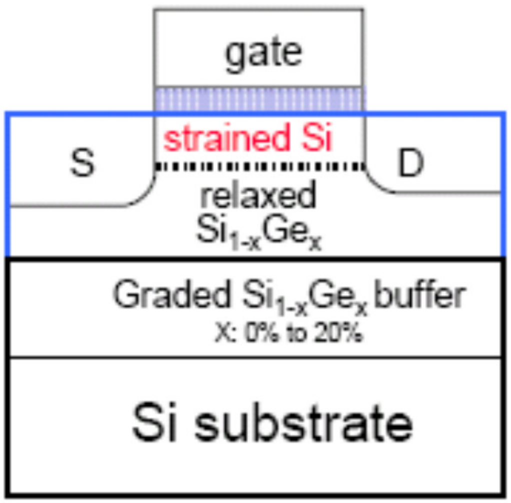


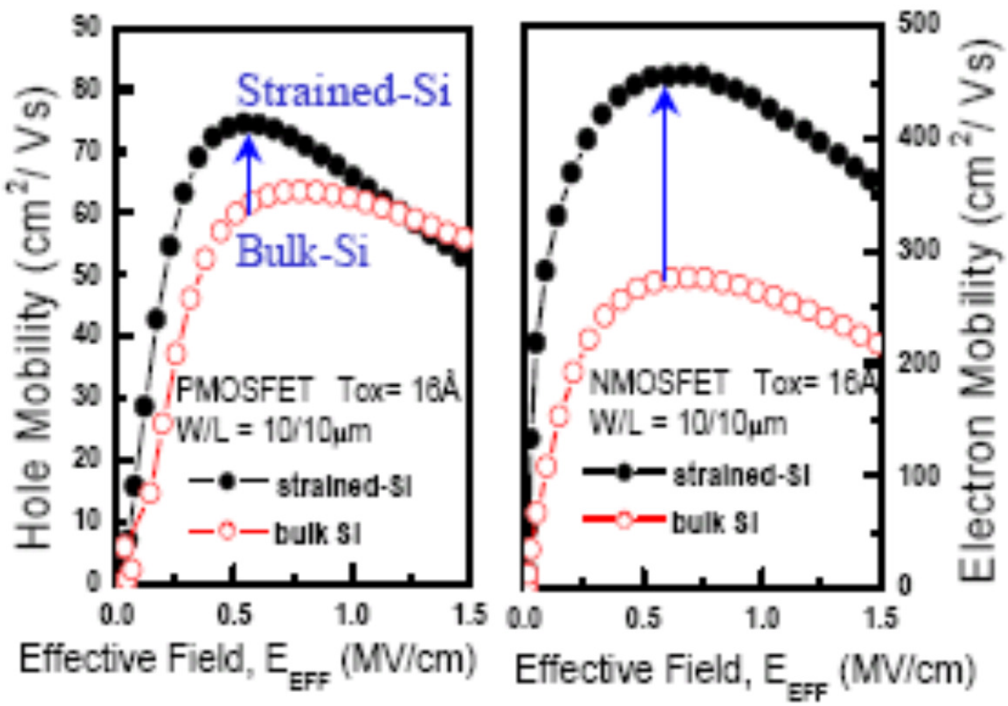


Uniaxial Compressive Strain to Enhance Mobility



Biaxial Strain to Enhance Mobility



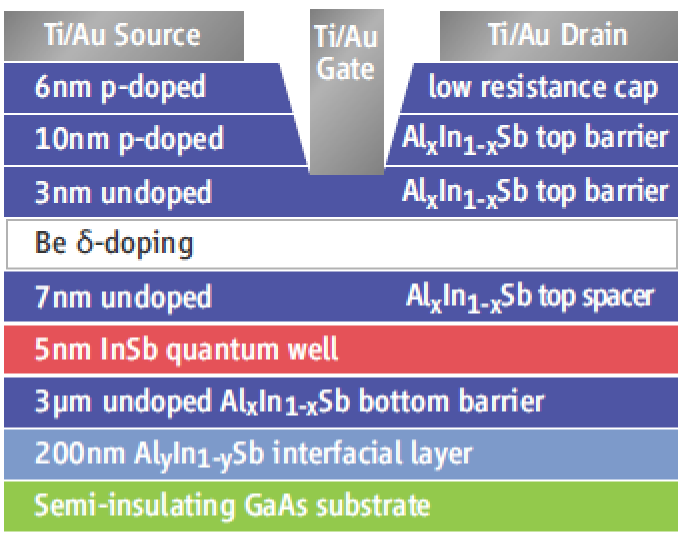


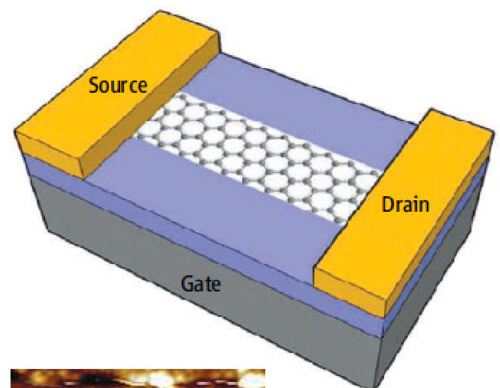
Adapted from Chang et. al, IEDM 2005

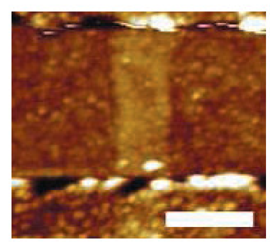
New Channel Materials for improved mobility

	Speed of Charges in Different Materials ($cm^2/V\cdot s$)				
Charges	Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
Electrons*	300	7000	10,000	15,000	30,000
Holes*	450	400	200	460	1250

*Electron carrier mobilities measured in transistor channels with electron concentration of $1x10^{12}$ cm^{-2}. Hole mobilities in bulk.

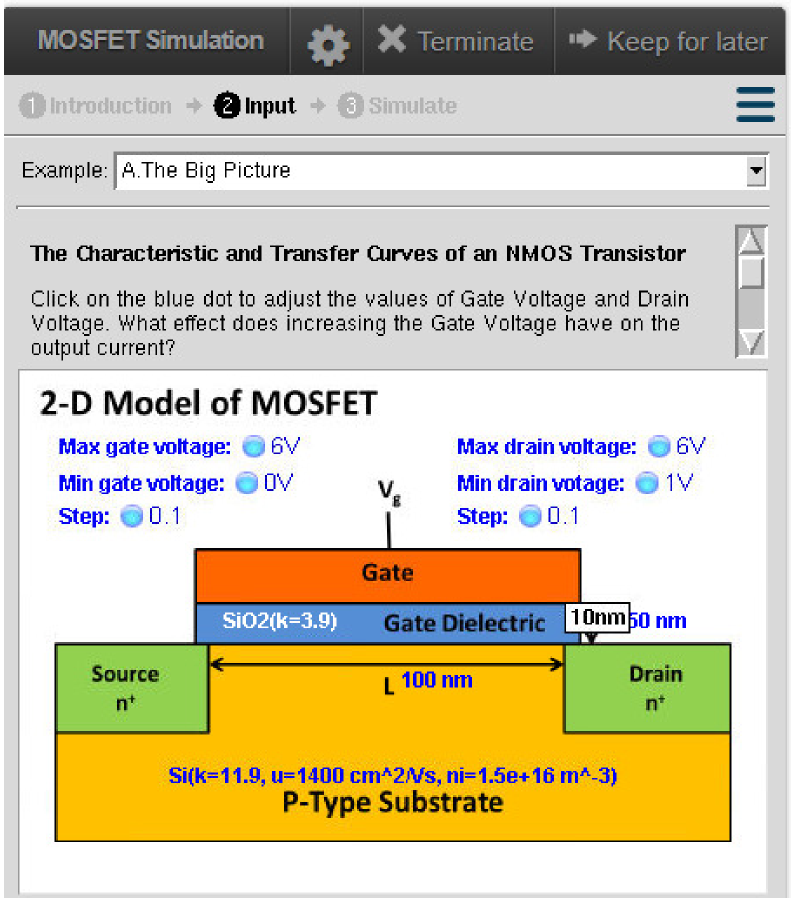






New kid. Transistors made from graphene nanoribbons could be blinding fast. But can they perform on an industrial scale?

Putting it all together

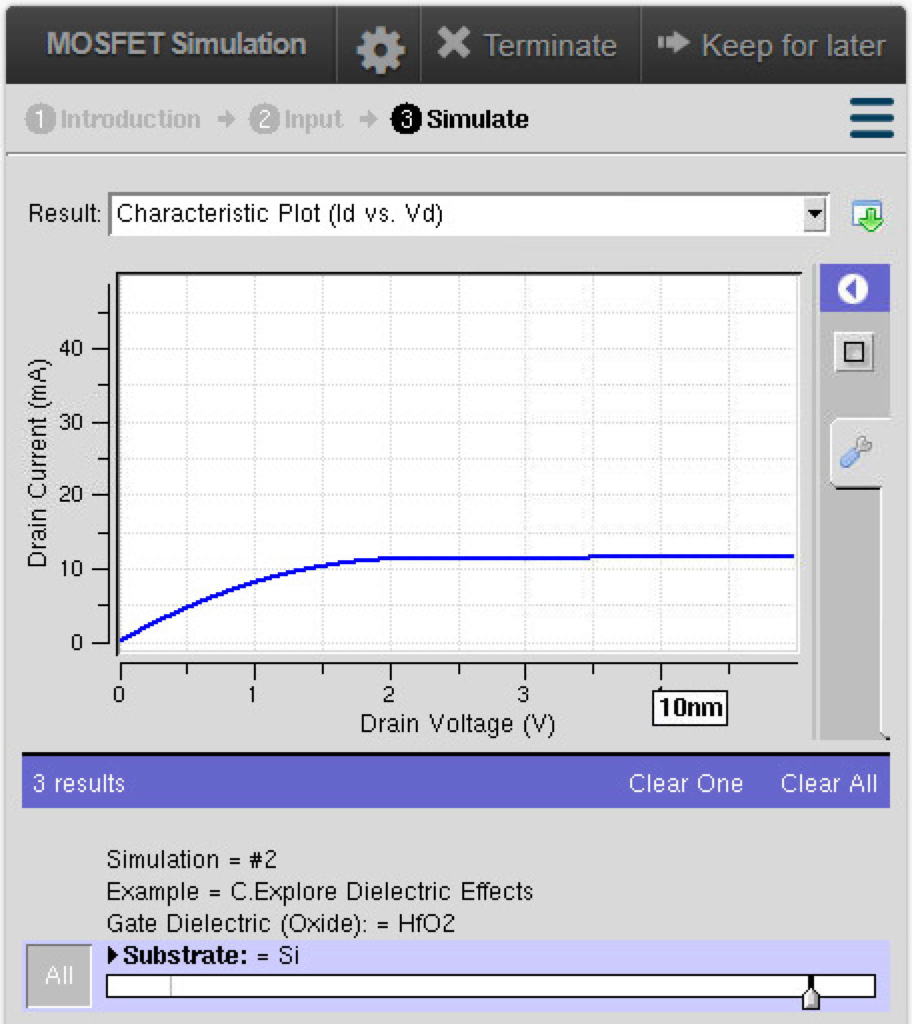


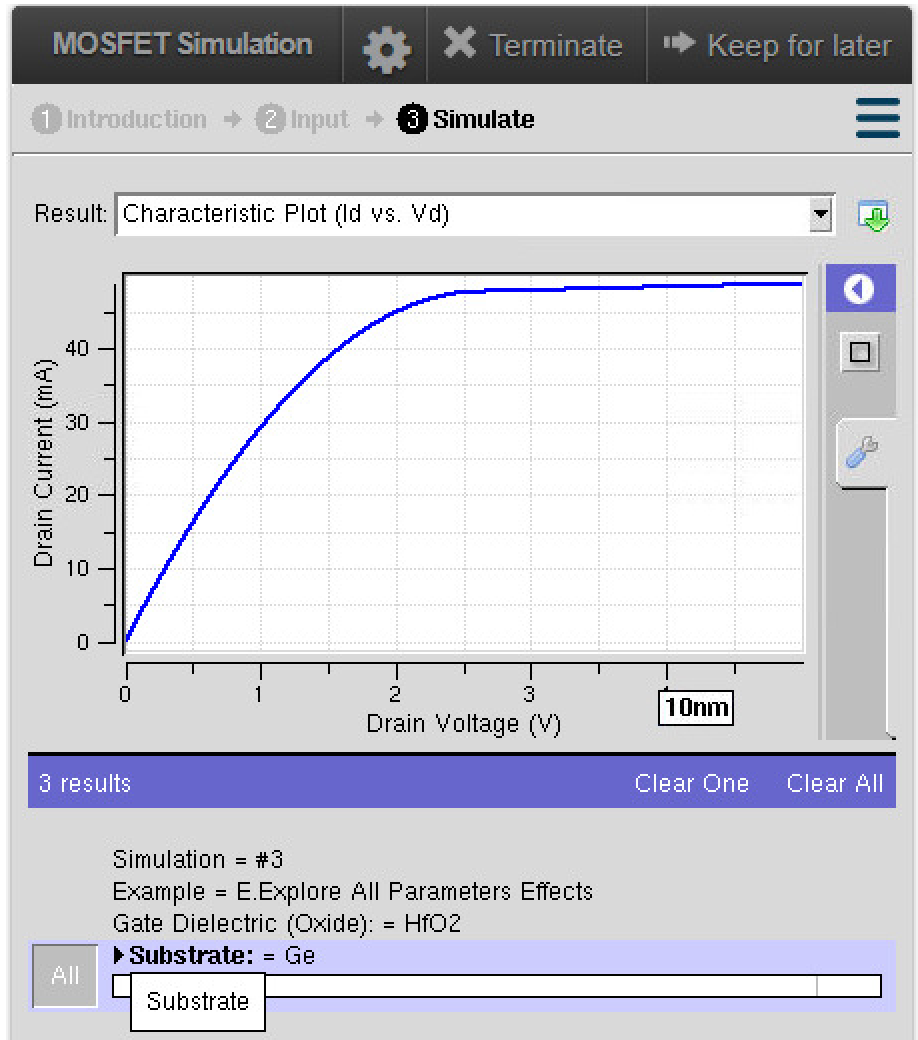
MOSFET Simulation Tools:

https://nanohub.org/tools/mosfet

https://nanohub.org/tools/mosfetsat

Comparing Ge with Si





summary

- The MOS capacitor is the foundation for MOS field effect transistors (MOSFETs), characterized by many device metrics
- MOSFETs differs from MOSCAPs in that the field from the S/D contacts now causes current flow – can be understood via band diagrams
- Two regimes: diffusion-dominated subthreshold and drift-dominated super-threshold, define the key I_D-V_D-V_G characteristics of a MOSFET
- Short channels and variability are serious concerns for MOSFET scaling, but strained lattices can help address this issue → effective channel lengths below 15 nm

New equations on equation sheet

MOS capacitors:

$$W = \sqrt{\frac{2K_s\epsilon_o\phi_s}{qN_A}}\ \text{cm} \qquad \mathcal{E}_s = \sqrt{\frac{2qN_A\phi_s}{K_s\epsilon_o}}\ \frac{\text{V}}{\text{cm}}$$

$$Q_B = -qN_AW(\phi_s) = -\sqrt{2qK_s\epsilon_oN_A\phi_s}\ \frac{\text{C}}{\text{cm}^2}$$

$$V_G = V_{FB} + \phi_s + \Delta\phi_{ox} = V_{FB} + \phi_s - \frac{Q_s(\phi_s)}{C_{ox}}$$

$$C_{ox} = K_o\epsilon_o/x_o \qquad V_{FB} = \Phi_{ms}/q - Q_F/C_{ox}$$

$$C = C_{ox}/\left[1 + \frac{K_oW(\phi_s)}{K_sx_o}\right]$$

$$V_T = -Q_B(2\phi_F)/C_{ox} + 2\phi_F \qquad Q_n = -C_{ox}(V_G - V_T)$$

New equations on equation sheet

MOSFETs:

$$I_D = -WQ_n(y=0)\langle v_y(y=0)\rangle$$

$$I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T)V_{DS}$$

$$I_D = WC_{ox}v_{sat}(V_{GS} - V_T)$$

Square Law (for $V_{GS} \geq V_T$):

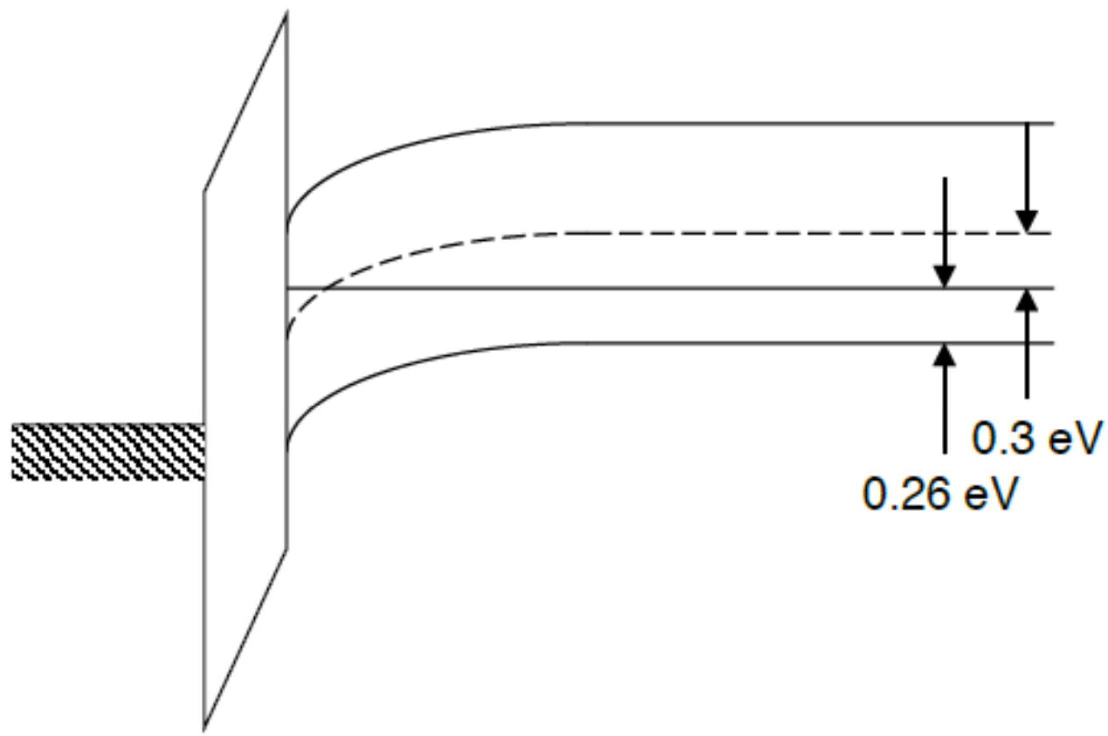
$$I_D = \begin{cases} \frac{W}{L}\mu_n C_{ox}[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2], & 0 \leq V_{DS} \leq V_{GS} - V_T \\ \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_T)^2, & V_{DS} \geq V_{GS} - V_T \end{cases}$$

Review Questions

1) Why is the small signal conductance and diffusion capacitance absent for MOS capacitors?
2) What is the expression for inversion capacitance? Why isn't there inversion capacitance in a diode?
3) What is the difference between flatband voltage vs. threshold voltage?
4) When would you use deep depletion formula vs. small signal formula?
5) Explain why there is a difference between low frequency response vs. high-frequency response for a MOS-C, but there is no such distinction for MOSFET.

Example Free Response Question

5. An MOS capacitor is biased at the threshold of inversion, as shown in the band diagram below. You may assume that no inversion layer charge is present, and that the structure is "ideal" as defined in class. (The sketch is not drawn exactly to scale. Do not attempt to answer the questions below by "measuring" the diagram.)



Example Free Response Question

a. What is the surface potential?

Example Free Response Question

b. What is the substrate doping?

Example Free Response Question

c. What is the semiconductor depletion width?

Example Free Response Question 2

A silicon p-type MOS capacitor is maintained in the dark at room temperature. Substrate doping is 10^{17} cm^{-3} and the oxide thickness is 20 nm. Assuming it is ‘ideal’, calculate the threshold voltage.