Week 13 Quiz Answers
ECE 606: Solid State Devices
Mark Lundstrom
Purdue University, Spring 2013

Quiz 1:
Answer the **four multiple choice questions** below by choosing the **one, best answer**.

1) What is the "flatband voltage" of an MOS capacitor?
   a) The surface potential of an MOS capacitor for $V_G = 0$.
   b) The voltage drop across the oxide for $V_G = 0$.
   c) Another term for $2\phi_F$.
   d) The voltage that must be applied to the gate in order to make the band bending in the semiconductor zero.
   e) The voltage that must be applied to the gate in order to make the semiconductor intrinsic at the surface.

2) What effect does a metal-semiconductor work function difference have on a $C(V)$ characteristic for an MOS capacitor?
   a) It increases the oxide capacitance.
   b) It decreases the oxide capacitance.
   c) It increases the inversion capacitance.
   d) It decreases the inversion capacitance.
   e) It translates the $C(V_G)$ vs. V_G characteristic to the left or right on the voltage axis.

3) Assume that there is charge, $\rho_m(x)$, distributed within the oxide. Charge at what location in the oxide has the biggest effect on the threshold voltage?
   a) At the top of the oxide, adjacent to the metal gate.
   b) At the bottom of the oxide, next to the Si substrate.
   c) At the center of the gate oxide.
   d) Charge in the oxide has the same effect wherever it is located.
   e) Charge in the oxide has no effect on the threshold voltage – no matter where it is located.

4) What causes the "bias temperature instability"?
   a) An increase in the magnitude of the charge in the oxide with increasing bias and temperature.
   b) An decrease in the magnitude of the charge in the oxide with increasing bias and temperature
   c) A change in the centroid of the charge distributed within the oxide cause by the application of a bias at an elevated temperature.
   d) A change in the second moment of the charge distributed within the oxide...
   e) A shift in threshold voltage caused by the break of silicon and oxygen bonds caused by the application of a bias at an elevated temperature.

Continued on next page

Quiz 2:

1) What is the purpose of a "forming gas anneal"?
   a) To anneal the defects produced by ion implantation.
   b) To tie up dangling bonds at the Si : SiO_2 interface with oxygen.
   c) To tie up dangling bonds at the Si : SiO_2 interface with hydrogen.
   d) To promote surface reconstruction to reduce dangling bonds on a Si surface.
   e) To densify the SiO_2 and increase its breakdown voltage.

2) If the transition from depletion to inversion in an MOS CV characteristic is "stretched out", what does it indicate?
   a) A high concentration of mobile ions in the oxide.
   b) A high concentration of fixed charge at the oxide-Si interface.
   c) A large metal-semiconductor workfunction difference.
   d) A high concentration of dangling bonds that change charge state with gate bias.
   e) It translates the $C(V_G)$ vs. V_G characteristic to the left or right on the voltage axis.

3) What is a "donor like" surface state?
   a) A surface state that is neutral when filled.
   b) A surface state that is neutral when empty.
   c) A surface state that dopes the semiconductor surface n-type.
   d) A surface state cause by the presence of a phosphorus or arsenic atoms on the surface.
   e) A surface state located in energy very near the conduction band.

4) How do donor like and acceptor like surface states affect an MOS CV characteristic?
   a) Donor like states stretch out the CV characteristic in voltage, but acceptor like states do not.
   b) Acceptor like states stretch out the CV characteristic in voltage, but donor like states do not.
   c) Both donor like and acceptor like surface states stretch out the CV characteristic, but in different voltage ranges.
   d) Donor like states decrease the flat band capacitance
   e) Acceptor like states decrease the flat band capacitance.

Continued on next page

Quiz 3:

1) What is threshold voltage "roll-off"?
   a) A reduction in the magnitude of the threshold voltage as the channel length decreases.
   b) An effect caused by two-dimensional MOS electrostatics.
   c) A reduction of gate control over the channel potential.
   d) All of the above.
   e) None of the above.

2) Why do transistor designers increase the substrate doping of a bulk MOSFET every technology generation?
   a) To increase the threshold voltage.
   b) To increase reliability.
   c) To reduce threshold voltage roll-off.
   d) To increase the oxide capacitance..
   e) To lower the metal-semiconductor work function difference..

3) What is the primary motivation for replacing planar MOSFETs with FinFETs?
   a) To lower series resistance.
   b) To reduce parasitic capacitance.
   c) To lower the noise figure.
   d) To improve gate control over the channel and reduce threshold voltage roll off.
   e) To decrease the subtreshold swing below 60 mV/decade.

4) Why are MOSFETs intentionally strained?
   a) To reduce threshold voltage variations.
   b) To lower the surface state density.
   c) To decrease series resistance.
   d) To increase the channel mobility and, therefore, the drain current.
   e) To adjust the gate workfunction.