23. CHARACTERIZATION OF DEFECTS RESPONSIBLE FOR TDDB

23.1 Review/Background:

In the last few chapters, we have discussed the time dependent dielectric breakdown (TDDB) in CMOS devices. The physics behind TDDB was explained based on the Anode Hole Injection (AHI) model. According to this model, the electrons tunneling from the cathode impact ionize at the anode and generate hot holes. A fraction of these hot holes get injected back into the gate oxide and trapped in the oxide. The electrons tunneling through the oxide can recombine with these holes, i.e., electrons jump into empty seats on the lower energy levels. The energy released through this process breaks bonds. These newly created defect levels would allow additional electrons to tunnel through the oxide by a trap-assisted tunneling process.

In order to characterize this theoretical model, it is important to understand measurement techniques to monitor how defects are formed as a function of stress time. In this lecture, various measurement techniques that are commonly used are explained: 1) Capacitance-Voltage (CV) method, 2) Stressed Induced Leakage Current (SILC) method, 3) Low Voltage Stressed Induced Leakage Current (LV-SILC) method, and 4) Quantum Yield (QY) experiments.

23.2 Capacitance-Voltage (CV) Method

The capacitance-voltage (CV) method makes use of the fact that electrons can remain trapped in a fraction of the defect energy levels, leading to bulk oxide charges. First, a reduced gate voltage compared to the stress phase is applied. Second, the substrate contact is pushed up a bit to inject hot electrons to the oxide as shown in Fig. 23.1. When injected electrons fill up the defect levels, the defect levels are charged. The
charged density is proportional to the defect density, and a threshold voltage shift of the device can be measured to check how many defects are generated.

\[ V_{TH} = V_{TH} + \Phi_{MS} - \frac{Q_{IT}(\Phi_S)}{C_0} \]  

[lecture 7]

This method is suitable for gate oxides that are thicker than 10 nm. This is a simple measurement technique, but its low-sensitivity is the disadvantage. The smallest change in defect density that can be measured using the CV method is in the order of $10^{11}$ per $\text{cm}^2$.

23.3 **Stress Induced Leakage Current (SILC)**

The increase of oxide leakage current after high-field stress is defined as SICL. SILC measurement is specifically suitable for the oxide thickness ($T_{OX}$) in the range between 1.5 nm and 6 nm. This method can measure defect densities on the order of $10^8$/cm$^2$, which might correspond to a single trap being generated. The measurement is performed by lowering the gate voltage ($V_G$) at the stress bias ($V_{STS}$) to a measurement bias ($V_{MEAS}$) as depicted in Fig. 23.2(a), and the gate current can be monitored as shown in Fig. 23.2(b).
The defect levels in the oxide band gap provide additional leakage paths for the electrons, and it results in larger leakage currents. Since this trap-induced additional leakage current is small, it would be hard to identify in high gate voltage \( (V_G) \). Interestingly, the increase in leakage current will become visible at lower gate voltages when the direct tunneling current is smaller than the trap assisted tunneling current as shown in Fig. 23.2(b). This is the reason why SILC measurement has to be carried out at \( V_{MEAS} < V_{STS} \).

Fig. 23.2(b) shows that the slope of the SILC vs. \( V_G \) is almost half the slope of the direct current vs. \( V_G \) in a log plot. This is an important signature of SILC, and to understand this, analytical expressions for various gate-tunneling components shown in Fig. 23.3 are derived. The direct tunneling current \( J_{DIR} \) is given by

\[
J_{DIR} = AP_{DIR}(f_C(1-f_A) - f_A(1-f_C)) 
\]

\[
\approx AP_{DIR}(f_C - f_A)  \tag{23.1} 
\]

where \( P_{DIR} \) is the direct tunneling probability, and \( A \) is a constant. \( f_C \) is the Fermi function at the cathode, and \( f_A \) is the Fermi function at the anode. \( P_{DIR} \) can be obtained from the WKB approximation as

\[
P_{DIR} = e^{-\int_0^{R_{ox}} K(x)dx} \tag{23.2} 
\]

Following a similar argument, \( J_1 \), which is the tunneling current component from the cathode into the trap, can be expressed to
\[ J_1 = c \sigma N_{OT} P_1 [f_c (1 - f_T) - f_T (1 - f_c)] \quad 23.3 \]

A similar expression can be written for \( J_2 \), which is the tunneling current component from the trap to the anode.

\[ J_2 = c \sigma N_{OT} P_2 (f_T - f_A) \quad 23.4 \]

At steady state, both \( J_1 \) and \( J_2 \) current component should be equal, and they can be identified by SILC. Equating 23.5 and 23.6, one can eliminate \( f_T \), the trap occupation function. Thus we get the following expression for SILC.

\[ J_{SILC} = c \sigma N_{OT} \frac{P_1 P_2}{P_1 + P_2} (f_c - f_A) \quad 23.5 \]

The magnitude of P1 and P2 depends on the location of trap in the oxide. P1 and P2 can be expressed to the following equations from WKB approximation.

\[ P_1 = e^{-\int_0^\xi k(x) dx}, P_1 = e^{-\int_\xi^{T_{ox}} k(x) dx} = e^{-\int_0^{T_{ox}} k(x') dx'} \quad 23.6 \]

Where \( x \) is the distance measured from the beginning of the tunneling path and \( x' \) is the distance measured from the trap location. Since \( \xi + \xi' = T_{ox} \) the value of P1 or P2 does not depend on the position of trap.

\[ P_1 P_2 = e^{-\int_0^\xi k(x) dx + \int_\xi^{T_{ox}} k(x) dx} = e^{-\int_0^{T_{ox}} k(x) dx} \quad 23.7 \]
However, P1+P2 has a strong dependence on the position of trap as observed in Fig. 4. SILC would be maximized when P1+P2 reaches to its minimum. Due to their exponential decaying pattern from the interface the minimum will occur at sites around the half of the oxide. Hence, major contribution towards SILC comes from traps close to the middle of the oxide ($x = T_{OX}/2$).

Fig. 23.4. Tunneling probabilities of $P_1$, $P_2$, and their sum as a function of trap location ($0 \leq X \leq T_{OX}$)

Since $P_1=P_2=P$ in the middle of the oxide using Eqn. (23.7), the approximated expression for the net SILC is

$$J_{SILC} = \frac{c\sigma N_{OT} P}{2} (f_c - f_A)$$  \hspace{1cm} (23.8)

Eqn. (23.3) can be re-written as

$$J_{DIR} = AP^2 (f_c - f_A)$$  \hspace{1cm} (23.9)

By eliminating the tunneling probability $P$ between Eqn. (23.8) and Eqn. (23.9),

$$J_{SILC} = \frac{c\sigma N_{OT} P}{2} \sqrt{\frac{(f_c - f_A)}{A}} \sqrt{J_{DIR}}$$  \hspace{1cm} (23.10)
\[ \ln(J_{SILC}) = \ln \left( \frac{e \sigma N_{OT} P}{2} \sqrt{\frac{(f_C - f_A)}{A}} \right) + \frac{1}{2} \ln(J_{DIR}) \]  

The first term of the right hand side is independent of \( V_G \). Hence, this equation explains why there is a difference between SILC and direct tunneling current component.

### 23.4 Low Voltage Stress Induced Leakage Current (LV-SILC)

LV-SILC measurements are suitable for oxide thickness less than 2-3 nm. For thin oxides, the direct tunneling current at low gate voltage is much higher than increase in gate leakage due to SILC as shown in Fig. 23.5(a), and classical SILC may always be undetectable.

The solution is this problem is to reduce the \( V_G \) further and go to negative \( V_G \), close to the device flat band condition, and the energy band diagram is depicted in Fig. 23.5 (b). The band alignment of the gate and substrate results in a small amount of direct tunneling. The trap assisted tunneling current as described for the positive measurement \( V_G \) is also not present under these conditions. However, an alternate mechanism is possible in which the electron can tunnel to an interface trap and later recombine with a hole from the accumulation layer. LV-SILC is denoted as an increase gate current from the process.
The following expressions for the $J_1$ and $J_2$ current components can be written as

$$
J_1 = c\sigma N_{OT} P_{DIR}(f_C - f_T) \quad 23.12
$$

$$
J_2 = \frac{N_{OT} f_T}{\tau_R} (1 - f_A) \quad 23.13
$$

It is important to note that the LV-SILC measures the interface trap density and not the bulk traps as the case of conventional SILC. However if no Si-H bonds are broken during the stress phase, the measured trap density will be due to broken Si-O bonds, and will be proportional to the bulk trap density.

### 23.5 Quantum Yield (QY) Experiment

The techniques previously discussed measures the number of defects that are generated in the oxide. They do not provide any information regarding the energy distribution of these defects. The quantum yield (QY) measurement helps us in overcoming this limitation.

![Energy band diagram of NMOS transistor under negative gate bias with blue electrons and red holes. Kamakura, JAP, 88 (10), 2000](image)

When electrons are injected, there might be energy relaxation process making electrons get out of the trap level with lower energies. However, the number of injected red holes generated by the blue electrons can be accurately known as depicted in Fig. 23.6. As the ratio of the number of blue electrons to the number of red holes, called the quantum yield (QY), explains the energy loss during the transit, can be used as a measure of defects generated in the oxide.
The details of QY measurement can be explained with the device as shown in Fig. 23.7. The electron that tunneled in and the one that was generated by impact ionization flow out of the device through the substrate contact and contribute to the bulk current. Since the substrate is n-type and the source/drain contacts are p-type, holes that were generated flow into the source/drain contact and can be measured as an increase in source/drain current (they cannot go to the substrate contact). In this particular experimental set-up, electrons and holes get separated and collected in different contacts.

\[
QY = \frac{I_{SD}}{I_{SUB}}
\]

Defects in the oxide can give a significant amount of an additional gate leakage current. If this trap assisted tunneling were elastic there would be corresponding number of hot holes generated by impact ionization. Furthermore, hot holes will be collected from the source and drain contacts and we will see this additional current which comes from impact ionization after stress. However results from QY measurement show that even though the total leakage current has increased after stress, the overall average impact ionization efficiency decreases as shown in Fig. 23.8.
This can be only explained by the fact that the additional SILC component is not as efficient in generating electron-hole pairs as the direct tunneling current. It suggests that the trapped electron in a bulk defect loses some energy as the charged defect undergoes an energy relaxation and reconfiguration process as shown in Fig. 23.9. As a result, when the electrons tunnel out from the trap, they arrive with a lower energy compared to the direct tunneling electrons, reducing the impact ionization rate. By comparing the experimentally observed reduction in impact ionization rate with one from simulation results, the possible loss of energy within the oxide for the trap assisted tunneling process was estimated to be around 1-1.5 eV.

Fig. 23.8. (a) $I_G-V_G$ and (b) II coefficient $\alpha$, before stressing the device and during the stress.

Fig. 23.9. Trap assisted tunneling currents in gate oxide. There is an energy relaxation process which is around 1-1.5 eV.
QY experiment is critical, because it explains why there is no correlation in a thin oxide. If the additional SILC component is capable of impact ionizing and generating hot carriers, a positive feedback loop would have set in and new defects would tend to form close to the existing defects. However, the experiment results show that there is no space correlation. The reason is that SILC current has an energy which is 1eV down compared to the direct tunneling current, meaning there are few generated hot holes. Hence, we can have multiple soft breakdowns which are spatially uncorrelated. This can lead to improved device lifetime, which would not have been possible unless the electron looses a fraction of energy in the oxide during the trap assisted tunneling process and become inefficient in impact ionization at the cathode. What about a thick oxide? In this case the breakdown has to be localized. Because here we apply 12-13V and even after the energy relaxation trap assisted electrons are equally efficient as direct tunneling electrons.

23.6 Conclusion:

In this lecture, we have discussed a number of new measurement techniques to capture the trap density: 1) pulse Capacitance-Voltage (CV) method, 2) Stressed Induced Leakage Current (SILC) method, 3) Low Voltage Stressed Induced Leakage Current (LV-SILC) method, and 4) Quantum Yield (QY) experiments. Classical SILC probes mid-thickness traps in thick oxides, and LV-SILC is appropriate to probe surface states in thin oxides. QY experiments show that native traps are elastic, while stress-induced traps are inelastic. In addition, it should be noted that low-frequency (few kHz) charge pumping (CP) can be correlated to SILC and QY experiments for a comprehensive analysis.
Reference


Review Questions

[Q1] Can you use charge pumping method to determine bulk trap density?

[Q2] What method would you use if you want to determine defect close to the middle of the oxide?

[Q3] Define quantum yield (QY). How does quantum yield change with electron energy?

[Q4] Can you think of similar use of QY in HCI measurement? Please explain.

[Q5] QY experiments used gate injection technique. Can you use substrate injection?

[Q6] There is a striking similarity between SILC and SRH in terms of the position of the traps. Can you say what the similarity is?

[Q7] What is the difference between SILC and LV-SILC? Why do we use LV-SILC?