25. THEORY OF SOFT AND HARD BREAKDOWN

25.1 Review/Background:

In previous content, I explained the importance of soft breakdown (SBD) in extending the lifetime of PMOS, which usually has a short first breakdown time especially when it comes to the first transistor out of ten trillion transistors in modern IC industry. So the question will be answered here is that what condition must be fulfilled to ensure that the breakdown is soft rather than hard.

25.2 Oxide breakdowns need not be catastrophic

In Figure 25.1, it is observed that the gate current increases in steps as the soft breakdowns occur one by one. In most cases, the transistor is still functional after two soft breakdowns. It is illusional that the time interval between the second and third breakdowns because the time is in logarithm scale. The truth is that if we make the x-axis in linear scale, the gap between the second and third plateaus is significantly larger than the one between the first and second plateaus. The lifetime of PMOS is extended due to this fact.

![Figure 25.1 The gate current increase with SBDs.](image)

There is also a difference between hard breakdown (HBD) and SBD when it comes to the gate current. Referring to Figure 25.2, you can tell how the mechanism
behind the gate current change after SBD and HBD. The first left plot shows the gate current is the tunneling current before stress. The gate current is really noisy at low voltages because it is too low for the equipment to measure and then the current gradually increase as the gate voltage increases. On the other hand, the current is linear to the voltage if you look at the second right plot. The linear curve indicates that the gate becomes a resistor after hard breakdown and it may be due to the fact that the electrode has melted away.

Figure 25.2. **Left:** gate voltage vs. gate current with HBD (log) **Right:** gate voltage vs. gate current with HBD (linear) **Bottom:** gate voltage vs. gate current with SBD and HBD.

For the bottom plot in Figure 25.2, it is convincing that SBD conduction is non-ohmic and it retains insulating property, whereas, post-HBD conduction is ohmic. Moreover, the characteristics of the transistor will not be affected too much by SBD
because the drain current and the conductance almost remain same before and after stress as shown in Figure 25.3. Therefore, the performance of the circuit will not be influenced too much. Though there is still drain current leakage after SBD, the transistor would still function well. If it is HBD, the drain current will be zero and all the current will flow through gate.

![Figure 25.3. Transistor performance before and after stress.](image)

Furthermore, let us examine that how the noise is related to soft breakdown. In Figure 25.4, the noise of gate current is significantly increased after post-breakdown. However, the noise of drain current remains the same. As a result, SBD does not degrade ID noise for low input-impedance circuits. In addition, it has been shown that the mean threshold voltage shift small regardless the BD position. But the threshold voltage is changing as time goes in the second plot. The explanation is that the shift of threshold here is not due to breakdown but negative bias time instability (NBTI).
25.3 **Observations about soft vs. hard breakdown**

Before going further, I will explain the two ways of stressing transistors. As shown in Figure 25.5, one is using a constant voltage source as called constant voltage stress and the other is named as constant current stress because of a constant current source. For constant voltage stress, we measure the gate current and compare the pre-stress and post-stress values to determine whether it is a soft breakdown or a hard breakdown. Similarly, we compare the value before and after breakdown for constant current stress. But instead of measuring current, we switch to gate voltage. Interestingly, people usually tend to use constant current stress in the beginning of process for reliability test. Later on, they will change to constant voltage stress when they are comfortable with the process. The reason is that experiments show that breakdown is softer for constant current than constant voltage stress. It is easy to think that it is always constant voltage stress in integrated circuit. But it is actually between constant current and voltage stress. A simple case is a CMOS inverter. When HBD happens to the PMOS, the NMOS acts like a resistor.
Another interesting phenomenon is the distribution of breakdown. In Error! Reference source not found., the reliability test is conducted with different oxide thickness given a constant current under constant current stress. It is not hard to tell that there is no hard breakdown for 3.5 nm and 4.0 nm. For 5.0 nm, a fraction of the devices have SBD and the rest have HBD. Only HBD happens when we increase the thickness to 6.5 nm. Similar results occur in another test. In the test, we keep the oxide thickness constant and vary the current. As shown in Error! Reference source not found., the exact same kind of distribution is obtained.

Figure 25.5. Two different kinds of stress setup

Figure 25.6. Breakdown distribution (constant stress current)
It also turned out that breakdown is also related to the area of the transistor. As shown in the first plot in Figure 25.8, a larger area is more likely to give us a softer breakdown. Nevertheless, if you look at the plot carefully, it is obvious that it is also less likely for the breakdown to happen. Moreover, the second plot basically shows that breakdown is also softer at reduced voltage.

Figure 25.7. Breakdown distribution (constant oxide thickness)

Figure 25.8. Left: Breakdown distribution (capacitance area) Right: Breakdown distribution (gate voltage)
25.4 **A simple model for soft/hard breakdown**

First, let me introduce the simple circuit models for three different phases for breakdown. Referring to the first circuit in Figure 25.9, we only have the capacitance and the tunneling resistor since we only have tunneling current before breakdown and the current from the source is proportional to the area of the transistor. At the moment when breakdown occurs, the circuit is connected with a percolation conductor in parallel as shown in the second circuit and the breakdown current starts to be the dominant one. After breakdown happens, we can calculate the heat power by the third circuit. The bottom line is that if the power exceeds certain threshold, HBD is possible. One thing worth attention is that the breakdown current, unlike tunneling current, is area-independent. The argument is that when hard breakdown happens, all the current flow through a hole near the electrode and doesn’t depend on the area of the region.

![Figure 25.9. Circuit models for breakdown](image)

The idea of the model is to calculate the power dissipation based on the circuit model I just describe. First applying Kirchhoff circuit law, we can obtain the equation shown below.
\[ A \times C_{ox} \left( \frac{dV}{dt} \right) + A \times \alpha e^{-\beta/V} + \{g_0\}V^\delta = A \times I_s \]  

The first term on the left side is corresponding to the current flown through capacitor. The second term refers to tunneling resistor. The last term is for the percolation conductor. The term on the right side is the current from the current source. Before we proceed, it is interesting to analyze the distribution of the percolation conductance more or less. As shown in Figure 25.10, there is a kind of distribution of the percolation conductance. But the question is that how to interpret it? Luckily, there is a simple theory. If look at Figure 25.11, you will see that there are six configurations for two defect boxes touching each other. For each kind of configuration, we have different numbers of way to touch, which creates the distribution of the conductance. Moreover, the ratio between maximum and minimum conductance in the distribution is from 5 to 10. More importantly, the conductance is weakly oxide thickness dependent.

![Figure 25.10. Percolation conductance distribution](image-url)
Now the question is that how to determine the safe operation voltage. Before doing this, we first look at the following equation.

\[ G_{\text{p,crit}} = \frac{P_{\text{ther}}}{V^2} \]  

25.2

By this formula, we can calculate the threshold conductance knowing the threshold power dissipation that will lead to HBD. So the next step is to find \( P_{\text{ther}} \). As shown in the two plots on the top in the Figure 25.12, there is a threshold for soft-breakdown. The experiments show that \( P_{\text{ther}} \) is approximately 20 \( \mu \)W. Hence, the point below the red line is soft breakdown and the ones above is hard breakdown as shown in the bottom plot. Finally, we can find the threshold conductance and we can determine the possibility for SBD or HBD, since the distribution of the percolation conductance is already obtained.

Figure 25.11. Conductance distribution model
25.5 Interpretation of experiments

As shown in the upper left plot in Figure 25.12, the breakdown tends to be softer with weaker stress, which is intuitively. Another way to understand it is that more power is dissipated at larger stress, which leads to HBD. So, at intermediate stress, the breakdown is bimodal.
Another fact is that breakdown becomes softer with stress current than stress voltage. In Figure 25.13, if we stress the transistor at point A, it will move to C for constant current stress and E for constant voltage stress. But E has much higher power dissipation than C so more likely to have HBD.

25.6 Conclusion

In this chapter, we discuss about how to distinguish soft and hard breakdown by a thermal threshold related to dissipation during breakdown. Moreover, the statistical spread in soft-breakdown reflects the statistical distribution of the percolation resistance. Due to the difference in power dissipation in current stress and voltage stress, the breakdown characteristics in the two structures is dramatically different. It is also important to remember that it is the power not energy that dictates breakdown, otherwise adding a capacitor would change the breakdown distribution right away.

References

