Micro Thermoelectric Coolers for Integrated Applications

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ABSTRACT

A different approach for manufacturing arrays of micro thermoelectric coolers using integrated circuit technology is presented. The idea is to fabricate a synthetic wafer containing the necessary thermoelectric elements by first bonding alternating p and n type wafers and then slicing them to obtain an array of thermocouples. This array is then metallized using standard photolithography and evaporation techniques to yield an array of coolers. To demonstrate this approach, six element Bi_2Te_3 cooler arrays were made and characterized. In this paper scaling laws, processing details, practical limitations, and preliminary experimental results are discussed.

INTRODUCTION

Increased demand in the optical communications industry has led to many advances in semiconductor laser sources. Now, these sources are efficient and operate at low threshold currents. As a result, heat dissipation is low (100's of mW) and temperature dependent parameters can be stabilized with little cooling (<20 °C). Still, the low heat dissipation in conjunction with very small surface area (100's of μm^2) results in a high heat flux density. Recent work in the miniaturization of thermoelectric coolers (TECs), has shown the advantages of smaller coolers in these applications.[1] Basically, element lengths in the submillimeter range produce greater cooling densities than conventional coolers and allow the overall size of the cooler to be greatly reduced.

As the cost of semiconductor laser sources decreases, it is important to maintain the cost of packaging as low as possible. This paper presents a novel approach to manufacturing micro TEC's with the desired goal to facilitate packaging with semiconductor laser sources and other optoelectronic devices and thus reduce the cost of packaging and production. In standard packaging procedures, a wafer is diced into single devices or groups of devices. These are then individually mounted into a package. The ultimate goal of our approach is to develop a synthetic "wafer" of TEC's that can be bonded to a wafer of lasers or other electronic devices or circuits. The synthetic "wafer" is made by bonding n and p type wafers, slicing them, and then metallizing the contacts. When this synthetic wafer is bonded to the wafer of lasers, the whole structure can be diced together and then mounted. This process allows the use of standard integrated circuit technology to enhance mass production of mountable devices.

SCALING LAWS

In order to understand submillimeter cooler operation, a set of design rules is needed. Also, the first set of rules should only depend on length. This will be done by considering the cooling density when operating in the maximum cooling regime. In this way, the scaling of device performance as element length decreases can be easily understood.

To start, the cooling capacity at the cold side of a single thermocouple (including contact resistance) is given by[2];

$$Q = \alpha T_c I - \frac{I^2}{2}\left(R_{mat} + 2R_{con}\right) - K\Delta T \qquad (1)$$

where α is the Seebeck coefficient (205 $\mu V/K$ for Bi_2Te_3), R_{mat} is the material resistance (σ x area/length, σ_{ave}=1100 1/Ωcm), R_{con} is the contact resistance (r_c x area Ωcm^2)[3], and K is the thermal conductivity (κ x length/area, κ_{ave}=0.014 W/cmK). Next, cooling capacity in the maximum cooling regime is obtained from the condition dQ/dI=0. The cooling density is given by;

$$\frac{Q_{max}}{a} = \frac{1}{L}\left[\frac{\alpha^2 T_c^2}{\left(\frac{2}{\sigma}+4r_c\right)} - k\Delta T\right] \qquad (2)$$

at a current density of

$$\frac{I_{max}}{a} = \frac{1}{L}\left[\frac{\alpha T_c}{\left(\frac{2}{\sigma}+4r_c\right)}\right]. \qquad (3)$$

The results of Equations 2 and 3 are shown in Figure 1. This figure also shows similar expressions for the cooling and current densities in the maximum coeffecient of performance (COP) regime. Figure 1 shows that the maximum cooling increases as the element length decreases.
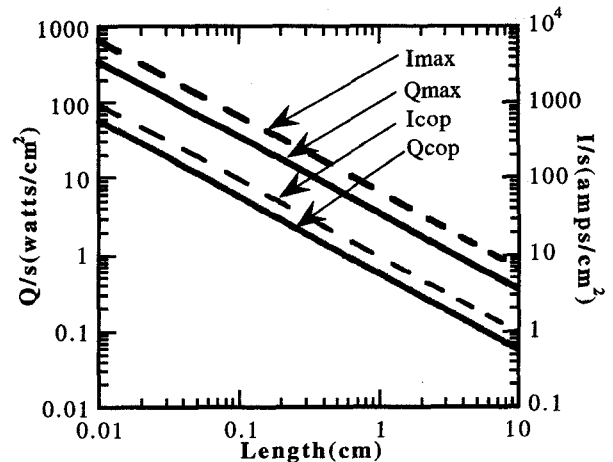

Fig 1. Cooling Density and Current Density vs Element Length in both the maximum cooling and maximum COP regimes. R_{con}=0, ΔT=17°C from a room temperature of 37°C

Also, an element length of 1mm produces a cooling density of 34.7 W/cm^2 and an element length of 100μm produces a cooling density of 347 W/cm^2. Of course, the maximum
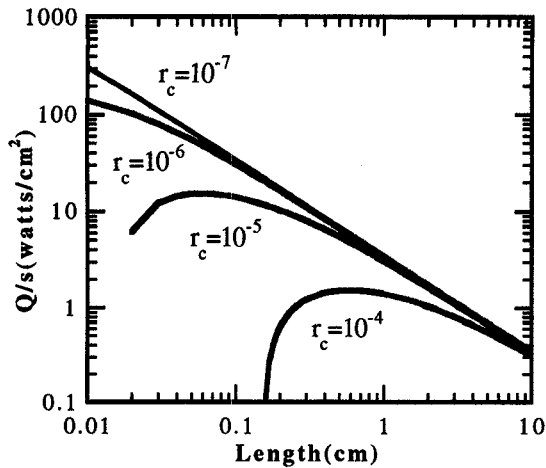
Fig 2. Cooling Density vs Element Length in the maximum cooling regime. Included is the effects of contact resistance: r_c (Ω/cm).

current density increases as well. An element of 1mm requires a current density of 654.7 A/cm^2, and an element length of 100μm requires a current density of 6547 A/cm^2.

Cooling densities in the range $\geq$100W/cm^2 are produced when the element length is smaller than 300μm.

The next step in the design rules is to determine the total cooling capacity and the total current for an array of thermocouples. These thermocouples are electrically in series and thermally in parallel, thus

$$Q_{total} = \frac{Q_{max}}{a} A_{total},\qquad(4)$$

$$I_{total} = \frac{I_{max}}{a}\frac{A_{total}}{N}.\qquad(5)$$

The total current can be reduced by increasing the number of elements per area. Thus, a 1mmx1mmx100μm device with 65 elements would have cooling capacity of 3.47W with a total current of 1A at a temperature difference of 17°C.

The last step is to analyze the effect of contact resistance as the element length decreases. This is presented in Figure 2. This figure indicates that the effect of contact resistance is more pronounced at smaller element lengths. To make devices shorter than 1mm, a contact resistance of 10^{-6} or less is needed. But, a contact resistance of 10^{-6} greatly reduces cooling at lengths $\leq$ 300μm.

DEVICE PROCESSING

Figure 3 displays the processing steps necessary to fabricate a synthetic wafer of TECs. To demonstrate and develop this approach an array of 6 element bar coolers was made. The steps necessary for this are also presented in figure 3. An overview of the steps for the array and synthetic wafer will be presented and the remainder of this section discusses the specifics in the array fabrication.

To produce a synthetic wafer, alternating n and p type wafers are first bonded together (Fig.3a). Next, the resultant structure is cut into slices (Fig. 3b). These slices can be processed into an array of bar coolers. This is done by fabricating metal contacts and then mounting the array to a substrate(Fig. 3c). To further increase the number of cooling elements per unit area the slices in Figure 3b can be bonded together(Fig. 3d). This structure is once again sliced to yield a checker-board of alternating n and p type layers (Fig. 3e). Metal contacts are fabricated and the synthetic wafer of TECs is now bonded to the wafer with the opto-electronic devices(Fig. 3f). Finally, the bonded wafers are ready to be diced and mounted into a package. The remainder of this section presents the specific processing details for the array of bar coolers.

Before the wafers can be bonded, they must be prepared in order to insure periodicity in the stack which is necessary in the subsequent photolithography steps. To do this, they are lapped on a copper wheel using diamond grit to a desired thickness. Because Bi$_2$Te$_3$ is a soft material, care must
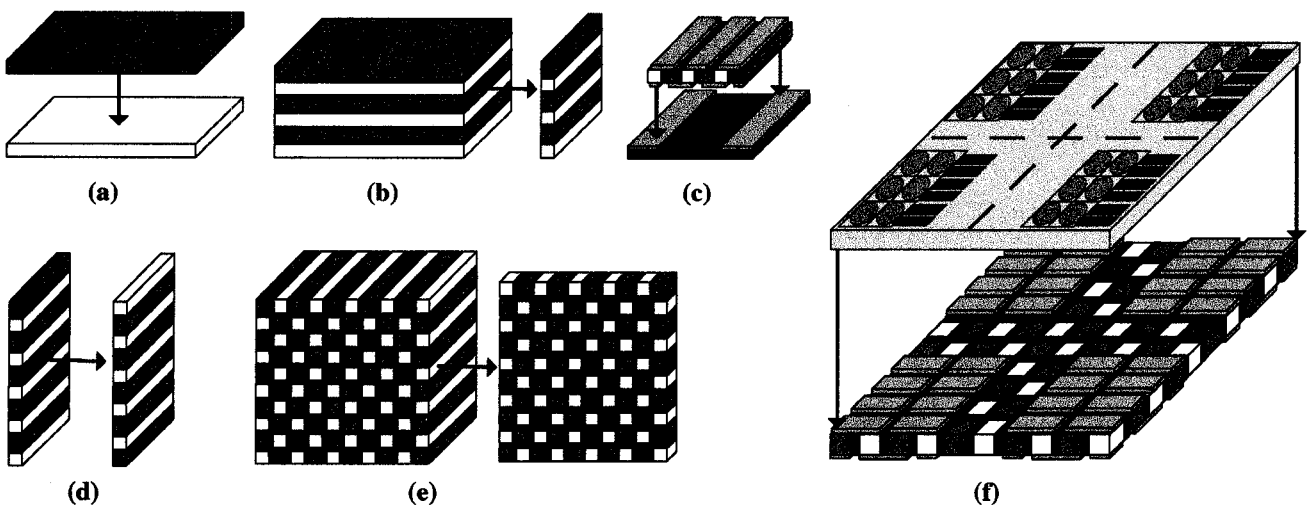

Fig3. Processing steps for a synthetic wafer of TECs. Also shown is the prototype array of bar coolers. a) p and n type wafers are bonded together. b) the resultant structure is cut into slices, c) a slice is patterned with metal contacts and mounted to a patterned substrate to make an array of bar coolers, d) to further process a synthetic wafer, the slices in b) are again bonded together. e) the resultant structure is again sliced to yield a synthetic wafer, f) the synthetic wafer is patterned with metal contacts and bonded to a wafer of opto-electronic devices(arrays of 6 PIN detectors). These can then be diced together, indicated by the dotted lines

be taken to reduce round off of the edges and scarring of the surfaces. Furthermore, polycrystalline Bi_2Te_3 has varying crystal grain structure which can produce an uneven surface with inappropriate lapping techniques. Finally, handling monocrystalline Bi_2Te_3 of thickness of 800μm or less requires special procedures as does polycrystalline Bi_2Te_3 of 400μm or less.

Next, the wafers are bonded together into a stack using a two part high temperature epoxy which will operate continuously up to 200°C. The procedure used produces an evenly thin epoxy layer between each wafer. This is done by first out-gassing the epoxy to remove any bubbles. Next, a thin layer of epoxy is spread on each wafer and then they are assembled into a stack. This stack is then placed into a vacuum press. The main features of this press are a dome shaped chuck and a silicone diaphragm. The press is exposed to house vacuum($\approx$150 Torr) which draws the diaphragm down on the dome shaped chuck which in turn applies an even pressure over the surface of the stack. Finally, the epoxy is cured with a temperature ramp that allows the whole press to remain at an uniform temperature . This technique produces an epoxy layer 1μm in thickness.

The bonded stack of wafers must now be sliced (shown in Figure 4). In this step, it is critical to use a procedure that will not destroy the stack and allows parallel slices to be made. To do this, a high concentration diamond grit wafering blade (thickness 325μm) is used on a slow speed spindle.
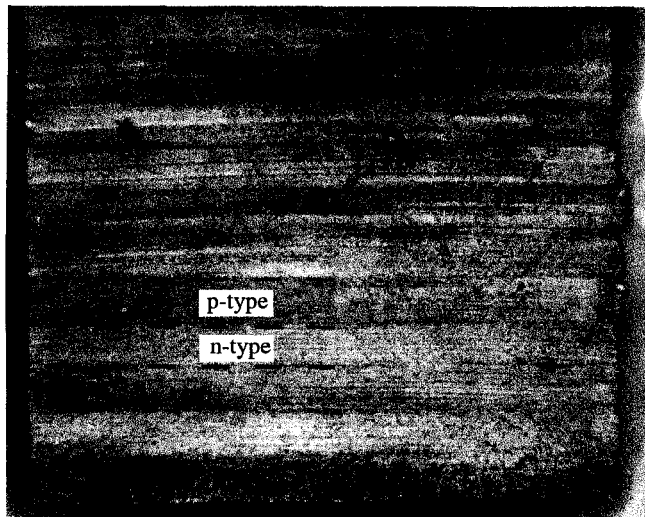

Fig 4. Top view of slice of bonded n and p wafers (refer to Fig3b).

At this point, each slice can be processed into a bar cooler. The next step is to fabricate metal contacts to allow current flow. To insure good adhesion of the metal to the Bi_2Te_3, the appropriate surfaces must be prepared. This is done by standard mechanical polishing techniques to remove any surface irregularities and damage. The metal contacts are fabricated using standard integrated circuit technology. First, the Bi_2Te_3 slice is cleaned and then a thin layer of polymer photoresist (Shipley AZ4210) is spun on. Next, a "chrome on quartz mask" with the appropriate metal contact pattern is

placed into contact with the Bi_2Te_3 slice. These are exposed under a UV light source. After the photo resist is developed, the mask pattern has been reproduced on the slice. The sample is then O_2 plasma etched to remove any photo resist scum. Metal is deposited onto the slice using thermal evaporation. First, a 300Å of Ni is deposited as both a sticking layer and a diffusion barrier for a top Au layer. Next, a 1μm layer of Au is deposited as a thick metal layer to cover the epoxy and any surface irregularities still present. This also acts as a good layer for solder adhesion. After evaporation, the bar is placed in acetone for lift off. Because both sides of the bar cooler need metal contacts, this procedure is repeated on the second side of the bar cooler.

The remaining step in manufacturing a bar cooler is to mount the device to a thermally conductive substrate. BeO is used because of its high thermal conductivity (270 W/mK, 625μm thick). The BeO is metallized in the same method as described for the Bi_2Te_3 bar cooler. The only difference is that a Ti sticking layer is used on the BeO. The bar cooler is soldered into place on the BeO using In/Pb solder. To insure good thermal contact between the cooler and substrate, thermally conductive varnish is injected in-between the two. After soldering leads to the substrate, the cooler is now finished.

PRACTICAL LIMITATIONS

When operating in the maximum cooling regime there are no theoretical limits in the increase of cooling density with the decrease of element length. Of course there are practical limits in element size that can be manufactured and handled. The most destructive step in the process is handling the material after it has been lapped (before bonding). Because of this, wafer thickness (wafer thickness translates into one dimension of the element area, see Fig3b,c) of 800μm (single crystal Bi_2Te3) and 400μm (poly crystal Bi_2Te_3) are the practical limits when directly handling the material. Using special handling techniques Bi_2Te_3 (single or poly) can be easily lapped down to 100μm or less, thus lowering the limit on element areas.   Minimum element length is less limited than area since the elements are already bonded with epoxy. This increases the mechanical integrity and allows easy handling. In this case element length are easily made to 100μm and care must be taken to make the length less.

EXPERIMENTAL RESULTS

The performance of the prototype 6 element bar cooler was evaluated by measuring the temperature at the cold side under an increasing DC current input. This was done at ambient pressure and temperature. The device was placed in good thermal contact with a heat sink using a thermally conductive paste. Thus, the hot side of the device remains at ambient temperature. The cold side temperature was measured using a thermister. In this prototype configuration, there is no cold side ceramic substrate and the thermister is placed directly on the thermocouples. The results of the temperature measurement are shown if Figure 7.
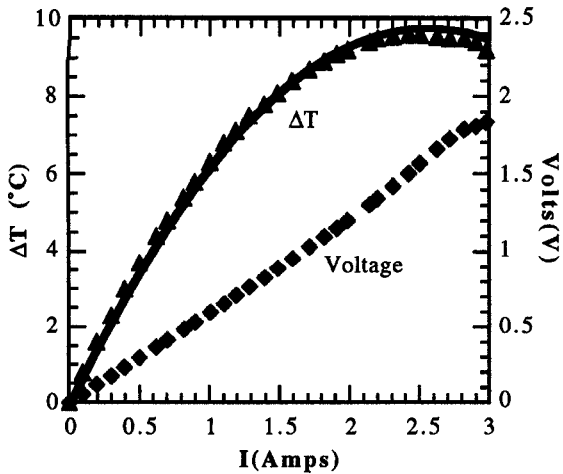
Fig7. Measurement results under DC input current. Vertical axis shows the temperature difference between the hot and cold sides and the voltage. The solid line shows the theoretical prediction.

In order to verify the results, a theoretical curve was calculated based on measured device and material parameters. The theoretical temperature difference is obtained by rearranging Equation 1 and is given by;

$$\Delta T = \frac{1}{K}\left[\alpha T_c I - I^2\left(\frac{1}{2}R_{mat} + R_{con}\right) - \frac{Q}{N}\right]. \quad (6)$$

To evaluate this, the Seebeck coefficient of the n and p type wafers was measured. This yielded average values of 203 $\mu V/K$ and 230 $\mu V/K$ respectively. Next, the resistance of the device was measured. This is obtained from the IV measurement (Figure 4). The voltage of the device is given by;

$$V = N\left[I\left(R_{mat} + 2R_{con} + R_{wire}\right) + \alpha\Delta T\right], \quad (10)$$

where R_{wire} is the resistance the current supply leads. The total resistance, given by the slope in Figure 4, is 0.63Ω. Subtracting the lead resistance, yields a device resistance of 0.15Ω. To use this value in Equation 6, it is multiplied by $1/2N(N=3)$, which yields 0.025Ω. Finally, the total thermal conductivity K, is obtained from the linear term of the measured temperature data, an average cold side temperature of 295 K, and the Seebeck coefficient(see Equation 6). These yield a K of 0.0166W/K. Substituting these values into Equation 1(with an estimation for ambient heat load) yields the following;

$$\Delta T = 1/.0166\left(-.002 + .128I - .025I^2\right) \quad (11)$$

Equation 11 is shown with the measured temperature difference in Figure 7. From this figure, the measured and calculated response show great similarity. The linear cooling term is due to the Peltier effect, and the quadratic roll off due to joule heating. Of course, the maximum temperature difference is much lower than desired. This is mostly due to the joule heating term, which is an order of magnitude more than expected. Preliminary measurements on conductivity and contact resistive reveal a material conductivity much lower than expected. Further investigation is necessary to determine the source of this high resistance. Using material with an

expected conductivity($\approx$1000 1/Ωcm), should yield a device with a maximum temperature difference of 44°C. This fact is presented in Figure 8.
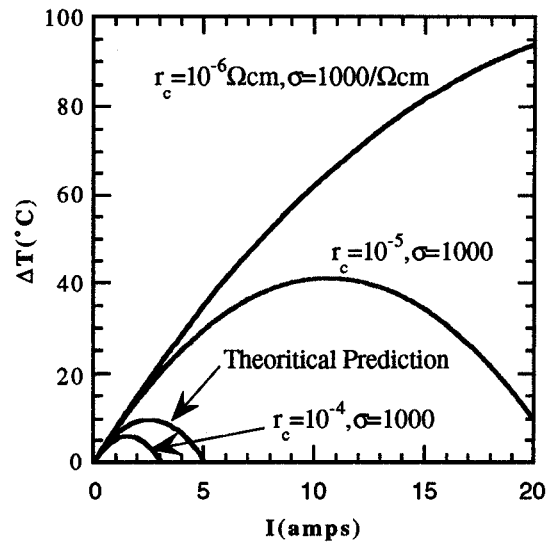

Fig8. Temperature difference vs input current for several different resistances. Also included is the theoritical prediction from Fig7.

CONCLUSIONS

This paper presented key developments in a manufacturing approach that can greatly enhance the ability to produce miniature TEC's and aid in packaging these to optoelectronic devices through the use of a synthetic wafer. These developments were validated by a prototype device which behaves as expected given the material limitations.

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