Fast Evaluation of Transient Hot Spots in VLSI chip packages

Je-Hyoung Park, Ali Shakouri, and Sung-Mo Kang

Extended Abstract

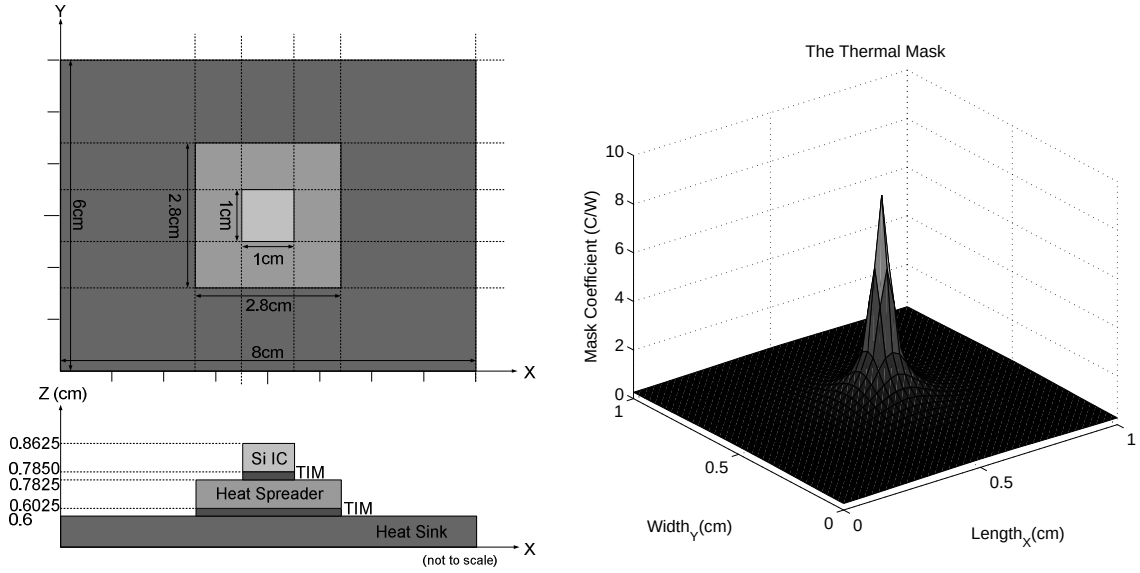
1. Introduction

The reality of high temperature non-uniformity has become a serious concern in the CMOS VLSI industry limiting both the performance and the reliability of packaged chips. Thus the surface temperature profiles of VLSI ICs have been investigated in recent years. Thus far, thermal simulations have been limited to steady-state worst case conditions, which has caused the use of conservative margins in thermal designs. It is known that the worst-case peak power consumption and its corresponding peak temperature are rarely observed [1]. When the thermal budget is tight, this approach is too costly. The temperature non-uniformity evolves with time and so do the hot spots. These transient characteristics were not simulated in prior art chip-level simulations. The transient temperature spike or localized heating can cause timing errors or even physical damages, thus reliability failures. Also, most of the transient thermal simulations of IC chips are done at the coarse architecture level. The state of the art chip-level transient thermal simulation is such that the inclusion of any realistic package configuration is prohibitively too expensive to be done for physical design optimization or performance verification in the packaged environment. To drastically reduce the time for the chip-level thermal simulation, we developed a matrix convolution technique, called Power Blurring (PB) method.

2. The Power Blurring (PB) Method

The PB method has its theoretical basis on the Green's function method and the methodological basis on image blurring used in image processing. For a given IC chip, power map can be acquired. If the power map is thought of as an image, the temperature distribution of the IC chip can be regarded as a blurred image of the power map. To perform the image blurring, a filter mask is required. A filter mask is equivalent to an impulse response, which is nothing but the Green's function of the system. The impulse response can be obtained by using Finite Element Analysis (FEA) tool such as ANSYS. To create a mask, a point heat source is applied to the center of the IC chip. An example of a packaged IC chip structure and the thermal mask are shown in Fig. 1. The thermal profile for a given power map is obtained when the thermal mask is convolved with the given power map. The advantage of the PB technique is that it can be applied to realistic chip geometries where analytical Green's function can not be obtained.

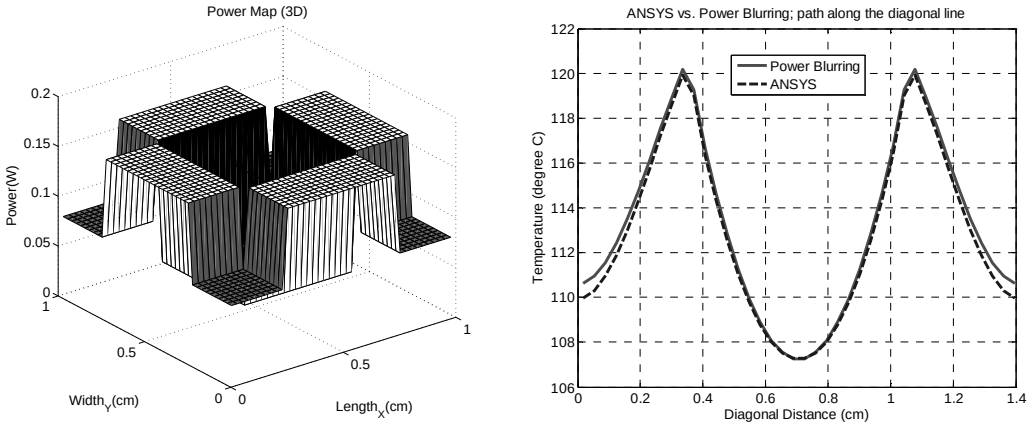
For a complicated power dissipation profile, the PB method reduced the calculation time by three orders of magnitude compared to the Finite Element Analysis (FEA) [2]. Since a point heat source at the center and that at the edge of the IC surface produce different peak temperatures and slightly different temperature profiles, usually several FEA simulations are needed in order to implement the power blurring technique for an arbitrary heat dissipation profile. The PB method was further improved by applying the Method of Image which takes into account the symmetry of the heat dissipation in a finite size chip [3]. In this paper, PB together with the method of images is applied to both steady-state and transient thermal simulations. Simulation results for various case studies are presented in the next section.



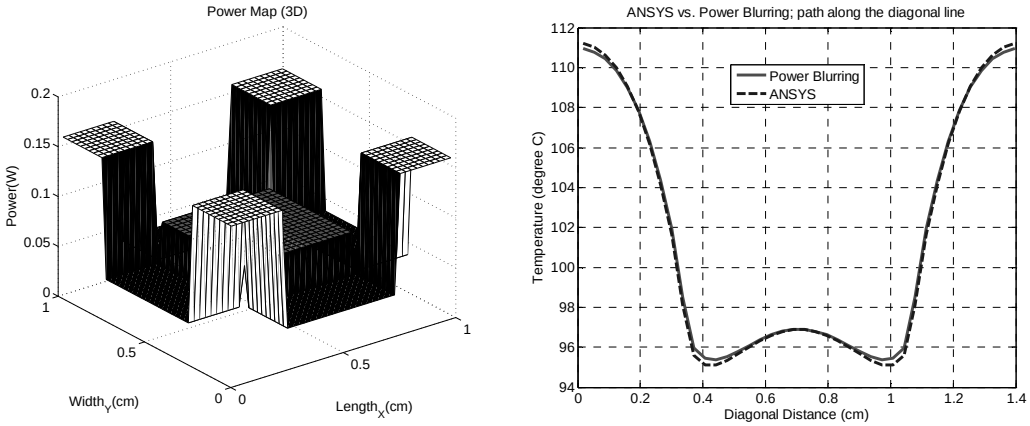
(a) (b)

Fig. 1 (a) Packaged IC chip where the heat spreader, the heat sink and the thermal interface layers are included (b) The thermal mask for a heat source at the center of the chip.

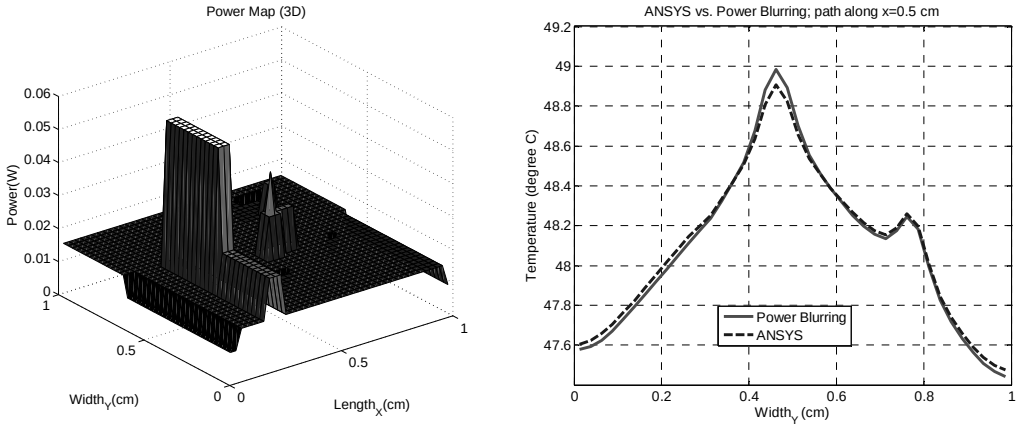
3. Case Studies



(a) Diagonal Path



(b) Diagonal Path

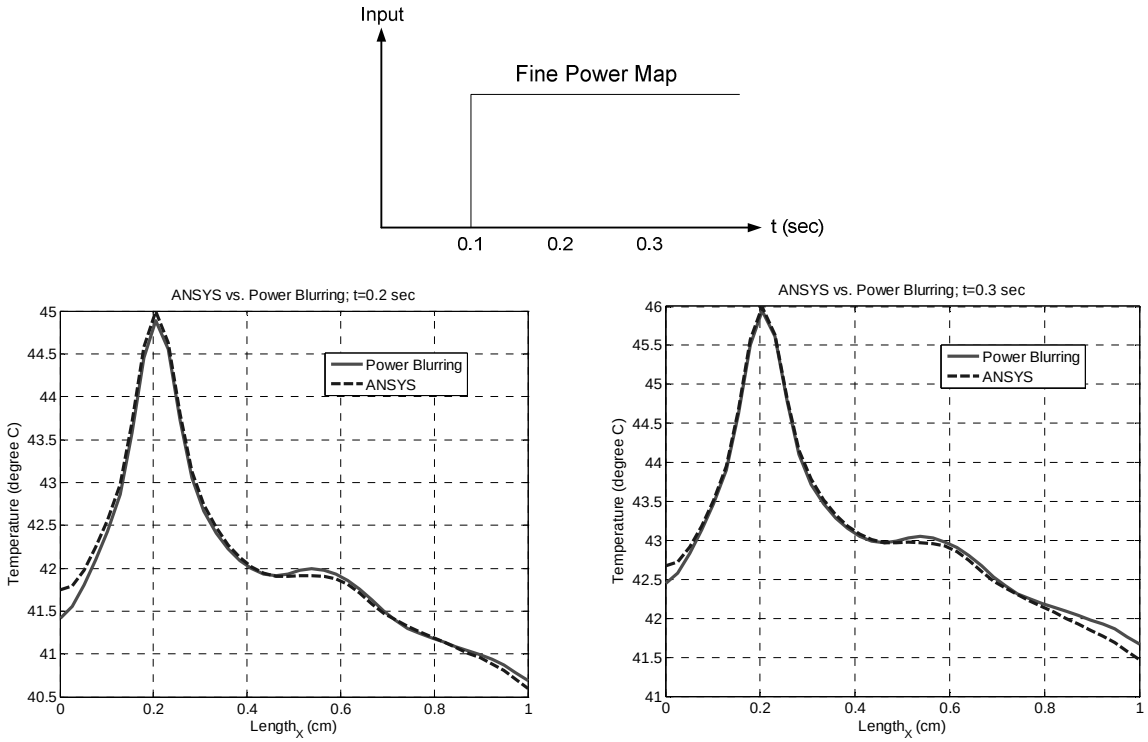


(c) Path along x=0.5cm

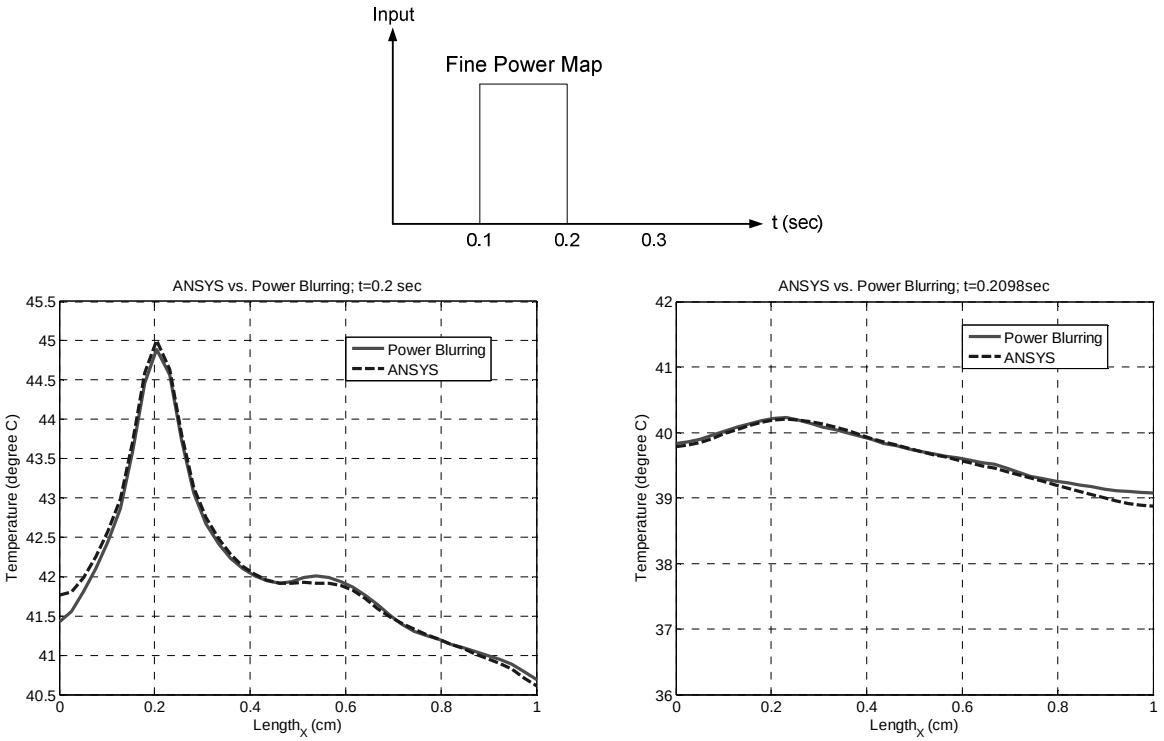
Fig. 2 Steady-state calculation results; power maps and corresponding temperature profiles along the specified paths (a) a case where there is high power consumption around the side edges, (b) high power consumption at the corners, and (c) a typical fine power map for an IC chip.

Fig. 2 shows various power maps and the corresponding temperature profiles along the specified paths. For the comparison, both PB calculation result and ANSYS simulation are plotted together. As can be seen, the PB method gives results that are in good agreement with ANSYS simulations. Maximum temperature errors are less than 1% in steady-state simulations.

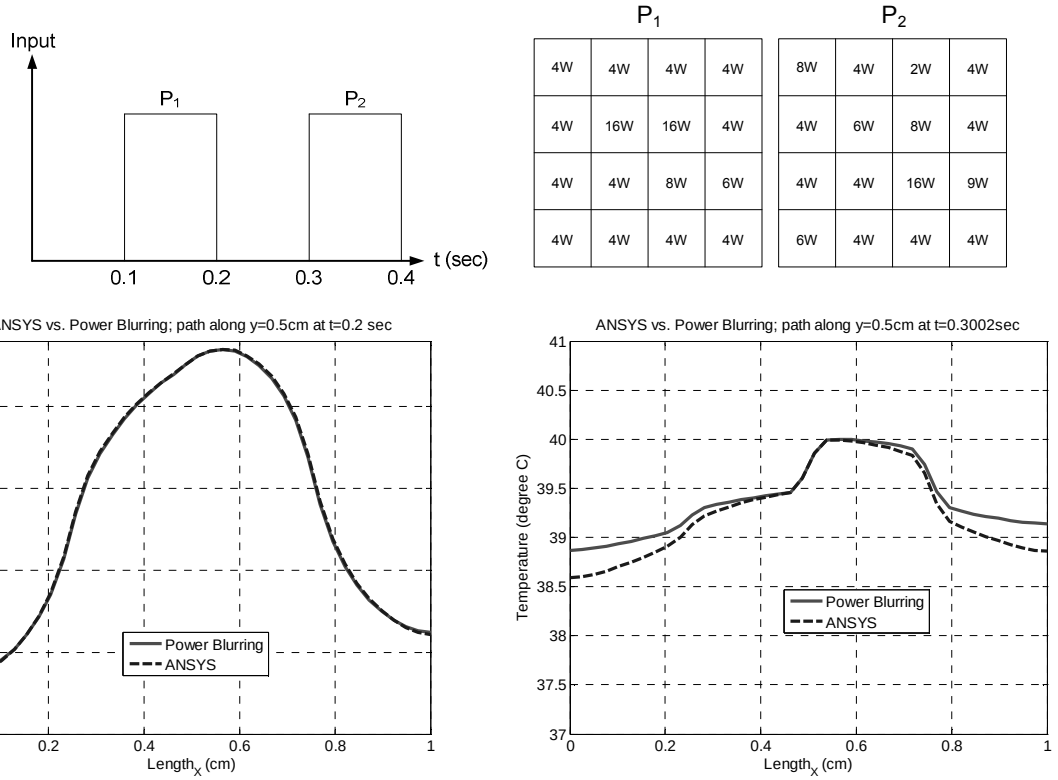
Transient simulations are performed for step and pulse inputs. To simulate a step input, the fine power map in Fig. 2 (c) is applied at t=0.1 as shown in Fig. 3 (a). Two temperature profiles at t=0.2sec and 0.3sec are presented.



(a) Path along y=0.5 cm



(b) Path along y=0.5 cm



(c) Path along y=0.5 cm

Fig. 3 Transient calculation results; input power dissipation pattern and corresponding temperature profiles along the specified path (a) step input of the fine power map, (b) pulse input of the fine power map, and (c) pulse input of the two different coarse power maps.

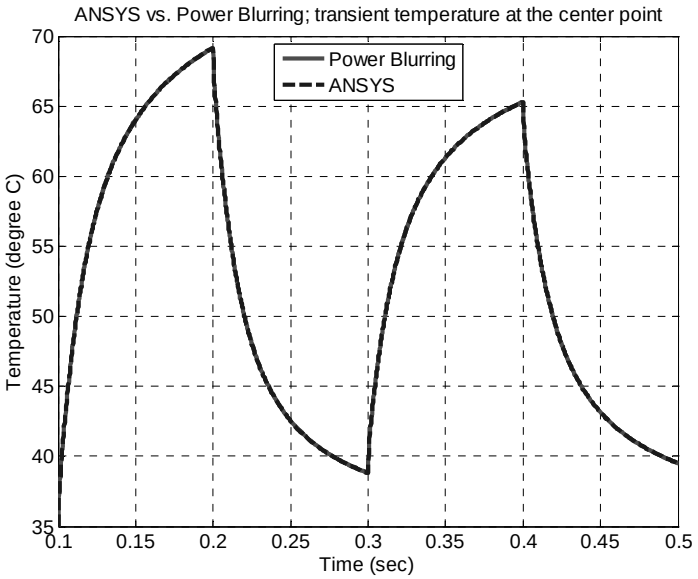


Fig. 4 Transient temperature profile at the center of the IC chip for the pulse input of the two different coarse power maps in Fig. 3 (c).

Two situations are considered for pulse input simulations. First, the fine power map was applied at t=0.1 sec and turned off at t=0.2 sec. Resulting temperature profiles at t=0.2 sec and 0.2098 sec are presented in Fig. 3 (b). Secondly, two different coarse power maps (P_1 and P_2) in Fig. 3 (c) are applied at t=0.1 sec and t=0.3 sec for 0.1 sec duration, respectively. Resulting temperature profiles at t=0.2 sec and 0.3002 sec are presented. The transient temperature profile at the center of the IC chip is also presented in Fig. 4. As can be seen, calculation results show good agreement with ANSYS simulation. Maximum temperature error of 3% was observed for all the transient case studies.

4. Conclusion

The PB technique together with the method of images can yield the temperature profile in a packaged IC with maximum error less than 3% for all case studies done and reduces the computation time by a factor of 100, compared to the simulations done by the industry standard tool, ANSYS.

References:

[1] Massoud Pedram and Shahin Nazarian, “Thermal Modeling, Analysis, and Management in VLSI Circuits: Principles and Methods,” Proceedings of the IEEE, Volume 94, Issue 8, Page(s):1487-1501, August 2006.

[2] Travis Kemper, Yan Zhang, Zhixi Bian and Ali Shakouri, “Ultrafast Temperature Profile Calculation in IC Chips,” Proceedings of 12th International Workshop on Thermal investigations of ICs (THERMINIC), France, September 2006.

[3] Virginia Martin Heriz, Je-Hyoung Park, Ali Shakouri, and Sung-Mo Kang, “Method of Images for the Fast Calculation of Temperature Distributions in Packaged VLSI Chips," Proceedings of 13th International Workshop on Thermal investigations of ICs (THERMINIC), Budapest, September 2007.