Proceedings of IPACK2007
ASME InterPACK '07
July 8-12, 2007, Vancouver, British Columbia, CANADA

IPACK2007-33880

TRANSIENT THERMAL CHARACTERIZATION OF ERAS/$IN_{0.53}GA_{0.47}AS$ THERMOELECTRIC MODULE

Y. Ezzahri, R. Singh, K. Fukutani, Z. Bian,
And A. Shakouri
Department of Electrical Engineering, University of California Santa Cruz
95064, California USA

G. Zeng and J. E. Bowers
Department of Electrical and Computer Engineering,
University of California Santa Barbara, 93106,
California USA

J. M. Zide and A. C. Gossard
Department of Materials, University of California Santa Barbara
93106-5050, California USA

ABSTRACT

Embedded metallic nanoparticles in semiconductors have recently been proven to be of great interest for thermoelectric applications. These metallic nanoparticles play the role of scattering centers for phonons and a source of doping for electrons; they reduce simultaneously the thermal conductivity and increase the thermoelectric power factor of the semiconductor. It has also shown that metal/semiconductor heterostructures can be used to break the crystal momentum symmetry for hot electrons in thermionic devices, then increasing the number of electrons participating in transport. A thermoelectric module of 200 N-P pairs of InGaAlAs with embedded ErAs metallic nanoparticles has been fabricated. Network Identification by Deconvolution (NID) technique is then applied for transient thermal characterization of this thermoelectric module. The combination of this new representation of the dynamic behavior of the packaged device with high resolution thin film temperature measurement allows us to obtain information about heat transfer within the thermoelectric module. This is used to extract the thermal resistances and heat capacitances of the module.

INTRODUCTION

Thermoelectric materials are interesting for many applications as power generators and heat pumps. The performance of thermoelectric energy conversion is quantified by the figure of merit ZT of a material defined as $ZT = \frac{\sigma S^2}{\beta} T$, where S, σ, β, and T are the Seebeck coefficient, electrical conductivity, thermal conductivity, and absolute temperature, respectively [1]. For both power generation and cooling applications, higher the ZT, better is the energy conversion efficiency. Increasing this factor can be made either by increasing the power factor σS^2 and/or reducing the thermal conductivity β. Historically, the ZT value of unity was reported over more than four decades, and it was difficult to beat this barrier of ZT due particularly to the difficulty of reducing the thermal conductivity bellow the alloy limit. Recently, some reports have shown the possibility of increasing ZT beyond the unity barrier using nanostructured thermoelectric materials [2, 3].

A new method to increase the figure of merit, ZT, of semiconductor materials has been recently proposed. This is based on embedding semimetallic nanoparticles in semiconductors [4-10]. In fact, incorporating semimetallic nanoparticles into a semiconductor can have a significant impact on the properties of the semiconductor. The particles can act as dopants, buried Schottky barriers, deep states for carrier recombination or enhanced tunneling, and phonon scattering centers. Unlike bulk thermoelectric materials, these composites have the advantage of compatibility with the complex structures traditionally associated with semiconductor thin films, which allows the consideration of increasing the Seebeck coefficient via electron filtering [11] as well as architectures which are optimized for the temperature gradient through the thickness of the device [6]. These semimetallic nanoparticles could be also used to break the crystal momentum symmetry for hot electrons in thermionic devices, and thus increase the cooling power [12].

To explore the thermoelectric energy conversion performance of such materials, a thermoelectric module made of 200 N-P pairs (N-type $(In_{0.53}Ga_{0.47}As)_{0.8}/(In_{0.52}Al_{0.48}As)_{0.2}$, and P-type $In_{0.53}Ga_{0.47}As$) with embedded ErAs semimetallic nanoparticles has been fabricated [7]. In this paper we study the thermal characteristics of such a module using a transient thermal characterization method. The overall cooling or power generation capability of the device strongly depends on the thermal properties of the N-P thermoelement as well as the parasitic thermal resistances in the module. An accurate and simple technique of measuring the thermal properties of the module is then required.

Thermal transient measurements have been used as one of the important methods for characterization of IC packages in the last 10-20 years. These measurements can be used to separate different contributions to the total thermal resistance and capacitance. They are also used to identify structure defects in the package. Temperature response measured by sensors for a given step excitation is widely used for analysis. In order to analyze the temperature response including structural information, various evaluation methods were proposed [13, 14]. Among the evaluation methods, the technique proposed by *Székely et al.* [14], based on linear *RC* network theory is very interesting. This new representation for the dynamic thermal behavior of the semiconductor packages has introduced a new notion: *the structure function* [14]. Using this quantity, the map of the heat current flow as a function of the cumulative thermal resistance in the sample can be obtained. In *Székely*'s method, the temperature response is transformed to the time constant spectrum by deconvolution technique, and then, the time constant spectrum is transformed into the cumulative or differential structure function, defined as the cumulative thermal capacitance or the derivative of the cumulative thermal capacitance with respect to the cumulative thermal resistance [14]. By interpreting these functions, thermal resistances and capacitances of each part in the sample studied can be identified [14]. This is called *Network Identification by Deconvolution* (NID) method.

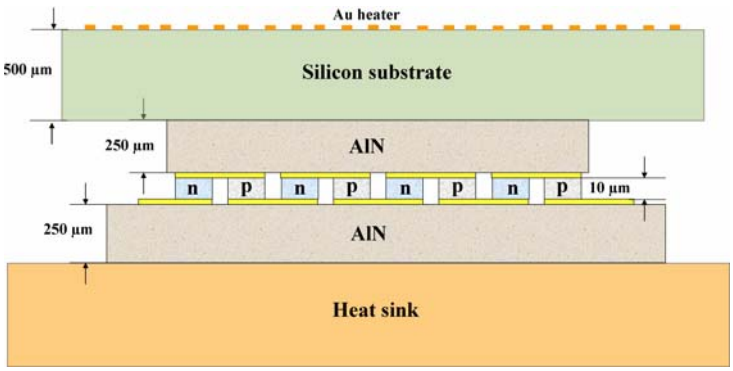
The thermal step-response transient measurement is becoming accepted as one of the most important techniques of thermal characterization of IC packages. Moreover it is recognized as an excellent, non-destructive investigation method for detecting heat conduction anomalies in chip assemblies [15]. Up to now, this method has been applied to various electronic and optoelectronic devices inside a package [14-18]. Recently, *Fukutani et al.* [19] have successfully used the NID method for thermal characterization of Si/SiGe thin film microcoolers. All the results show that NID technique is a powerful method to identify thermal resistances in the heat flow path. In this paper, we apply NID method to the thermal analysis of thin film thermoelectric module for the first time.

NOMENCLATURE

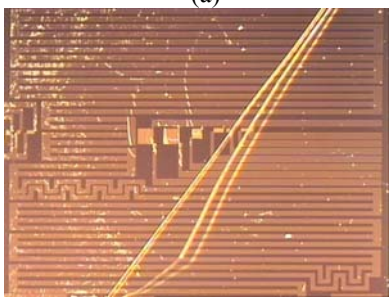
β: thermal conductivity.
γ: electrical resistance temperature coefficient of Au heater.
σ: electrical conductivity.
A: cross sectional area.
c_v: specific heat per unit volume.
C_Σ: cumulative thermal capacitance.
K_Σ: structure function.
R_Σ: cumulative thermal resistance.
R_0: Au heater electrical resistance at zero electrical excitation.
R: Au heater electrical resistance for non zero electrical excitation.
S: absolute Seebeck coefficient.
T: absolute temperature.
ZT: figure of merit.

EXPERIMENT

Figure 1 (a) illustrates a schematic diagram of the thermoelectric module we have analyzed. The thermoelectric module is made of 400 themoelements; 200 N-type 99.7% $(In_{0.53}Ga_{0.47}As)_{0.8}/(In_{0.52}Al_{0.48}As)_{0.2}$ with 0.3 % Er, and 200 P-type 99.7% $In_{0.53}Ga_{0.47}As$ with 0.3 % ErAs. Each thermoelement has a thickness of 10 μm, and a cross sectional area of 120×120 μm^2. For contact and bonding, metallic connection layers were deposited on top of the elements with a thickness of 0.7-1 μm for the contact layers and 6 μm for the bonding layers. The isolation on top and bottom of the whole device is mounted on 250 μm thick AlN ceramic plates. More detail on the fabrication process is reported in reference [7].



(a)



(b)

Figure 1: Schematic diagram of the ErAs: InGaAs/InAlAs thermoelectric power generator.

For thermal transient characterization, we have used a thin film Au heater deposited on a 500 μm silicon substrate. This heater is then mounted on the top AlN ceramic plate of the thermoelectric module using a thin silicon grease thermal paste to enhance the thermal contact between the two parts. The thermoelectric module is then put on a big copper heat sink using the same thermal paste as shown in figure 1 (a). Figure 1 (b) represents a top view photograph of the thin film Au heater.

In the experiment, the driving point behavior is investigated, which means that the same heater is used to excite the structure and to measure its temperature response. The temperature on the top of the thermoelectric module is measured through the electrical resistance change of the heater while a step function current is applied. The electrical resistance of the heater is expressed as $R(T) = R_0 + \gamma \times \Delta T$ where γ is the electrical resistance temperature coefficient. The calibration of this coefficient is done by measuring the sample's electrical resistance at various ambient temperatures.

In thermal transient measurement, a step function pulse current is applied to the heater on top of the module through one set of probes. Simultaneously, the electrical resistance change is measured through another set of probes. The current and voltage signals from the heater are detected using a digital oscilloscope. As it was already shown [19], when fast temporal resolution is needed, a high speed packaging and coplanar probes are used to reduce the signal ringing due to electrical impedance mismatch. A short time resolution of roughly 100 ns in thermal transient measurement has been achieved [20]. After the transient temperature response of the device is measured, a treatment based on linear distributed *RC* network theory was performed [14].

RESULTS AND DISCUSSION

In figure 2, we have reported the temperature transient response of the thin film heater on top of the thermoelectric module for a step excitation at the range 200 μs-2 s. The vertical axis denotes the temperature rise for an excitation power of 1W supplied to the top Au heater.

As we can see in figure 2, the temperature increase is very low, almost 2°C over 2s time range. This can be understood due to the large cross sectional area of the thermoelectric module. The temperature increase in figure 2 reflects the transient flow of heat through the whole structure: Si substrate → top AlN plate → thermoelectric module array → bottom AlN plate → Cu heat sink. This behavior is characteristic also of the geometrical path the heat flux takes from the top to the bottom of the device including successive constriction and spreading effects due to the difference in the cross sectional area between the different parts of the device.

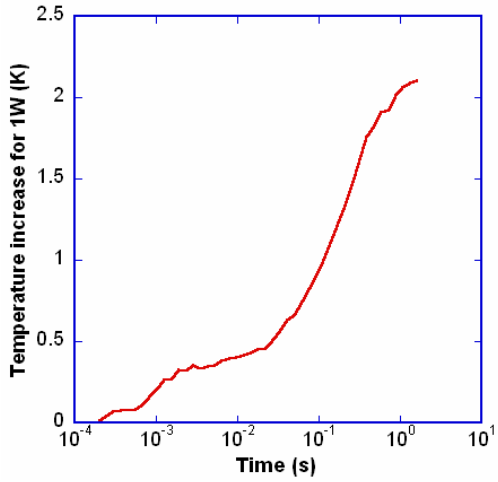


Figure 2: Measured temperature transient response of the whole device when the later is supplied by a step excitation current of 1W.

In order to use this graph to extract the thermal properties of the different parts of the whole structure, we have applied NID method using mathematical transformations [14]. The first step is the calculation of the time constant spectrum. This is obtained after transformation of the response function to the logarithmic time variable, differentiating it numerically and finally deconvolving it by certain fixed function using Bayes iteration [16]. The result is reported in figure 3.

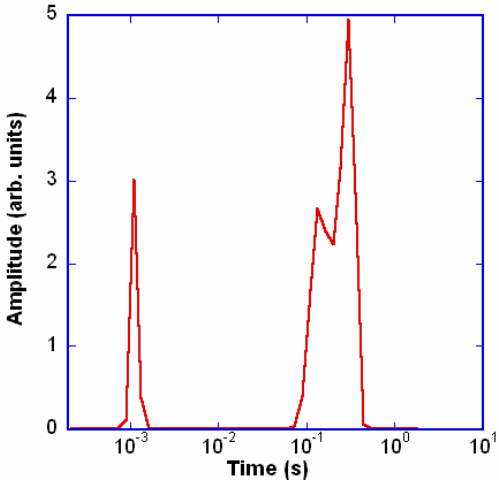


Figure 3: Time constant spectrum of the whole studied device.

Two peaks are clearly shown; the first one at about ~1ms is the signature of the heat diffusion within the top Si substrate just underneath the Au heater and above the AlN top plate. We believe that the second large peak at ~300 ms is due to the bottom AlN plate of the thermoelectric module together with the Cu heat sink.

In order to analyze the detail of the heat flux path, the second step of the analysis consists on the evaluation of the cumulative structure function and the differential structure function referred as *structure function* in brief [14]. We first plot the cumulative thermal capacitance C_Σ as a function of the cumulative thermal resistance R_Σ. Subsequently, we plot the derivative of the first graph. Evaluation of both graphs is based on the time constant spectrum and the result is reported in figures 4 (a) and (b), respectively.

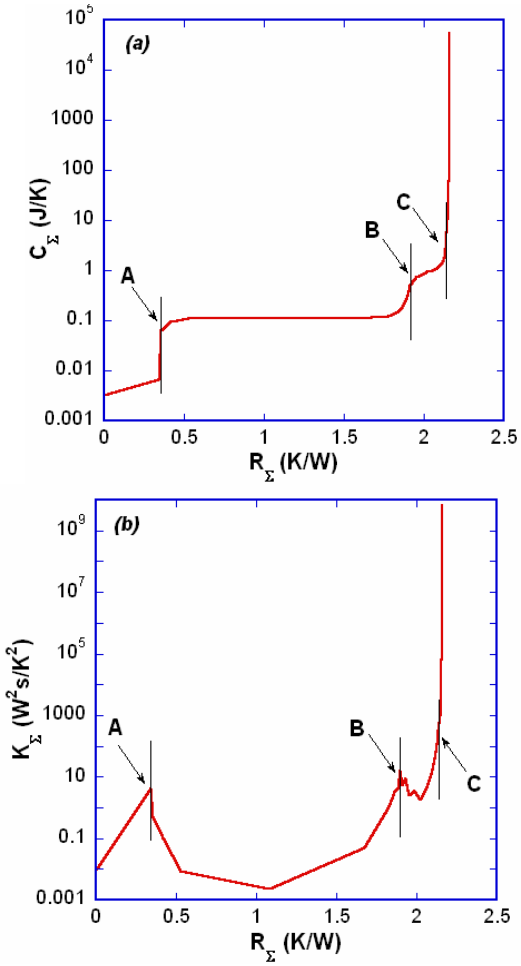


Figure 4: (a) Cumulative structure function and (b) differential structure function of the whole studied device.

Three important cumulative thermal resistance regions are indicated by capital letters on the graphs of figure 4. The left side of the first arrow **A** is due to the heat flow inside the top Si substrate. The expected thermal resistance and capacitance of the Si substrate with the dimensions (500 μm thickness, and 13.4×13.4 mm^2 cross section area) are 0.022 K/W and 0.146 J/K. These values are different from the ones obtained from the cumulative structure function (figure 4 (a)) at the arrow **A**, which are 0.35 K/W and 0.064 J/K. The effective area of the Au heater is smaller than the cross sectional area of the Si substrate. Furthermore, the volume of the Si substrate for the heat flux should be smaller than that of the actual substrate because of 3D heat spreading. The discrepancy in the values of thermal resistance and capacitance is consistent, since the thermal resistance is inversely proportional to the cross sectional area and the thermal capacitance is proportional to the volume. The high value of the thermal resistance and the low value of the thermal capacitance can be partly due to the presence of a void in the thermal paste between the Si substrate and the top AlN plate of the thermoelectric module. Additional measurements and 3D thermal simulations should shed light on the cause of the discrepancy.

The curve between arrows **A** and **B** is due to the whole thermoelectric module including the top AlN plate, the thermoelectric array module and the bottom AlN plate. The expected values of the cumulative thermal resistance and cumulative thermal capacitance of the thermoelectric module are 0.352 K/W and 0.074 J/K, respectively. From figure 4 (a), the observed cumulative thermal resistance and thermal capacitance of the thermoelectric module are 1.546 K/W and 0.246 J/K, respectively. The high value of the observed cumulative thermal resistance is due to the constriction and spreading of the heat flux through the ErAs: InGaAs/InAlAs thermoelements and the bottom AlN plate as well as additional interfaces material. The high value of the cumulative thermal capacitance needs further investigation.

The curve between arrows **B** and **C** (the end of the curve) is due to the interface between the thermoelectric module and the heat sink.

The structure function shown in figure 4 (b) can be written as $K_\Sigma(R_\Sigma) = {dC_\Sigma(R_\Sigma)}/{dR_\Sigma} = c_v \beta A^2$, where c_v is the specific heat per unit volume, β is the thermal conductivity and A is the cross sectional area in the heat flux path [16]. In other words: this function provides a map of the square of the heat flux cross sectional area as a function of the cumulative thermal resistance. The peaks of the structure function represent both increased cross sectional area and locally increased thermal capacitance.

The value of K_Σ at the first arrow **A** (figure 4 (b)) is 4.1 W^{2}s/K^2. Assuming that the thermal properties of the AlN are valid for this area, the cross sectional area is calculated to be approximately 9.3×9.3 mm^2. This value is little bit higher than the actual value of the top AlN plate which is 8×8 mm^2; this is due to the heat flux constriction at the interface Si substrate/top AlN plate. Similarly, the value of K_Σ at the arrow **B** is 15.9 W^{2}s/K^2. This value can then be converted to give a cross sectional area of 12×9 mm^2, assuming the thermal properties of the Cu heat sink. This value is very consistent with actual value of the bottom AlN plate which is 11×8 mm^2. The difference can be explained by the 3D heat spreading inside the heat sink.

Table 1 recapitulates all the expected and observed values of the cumulative thermal resistances and capacitances of the top Si substrate and the ErAs: InGaAs/InAlAs thermoelectric module power generator.

Table 1: Recapitulated expected and observed thermal resistances and capacitances of the top Si substrate and the thermoelectric power generator module. * refers to the expected values.

Properties	Top Si substrate	Thermoelectric power generator module
R_Σ (K/W)	0.022* 0.35	0.352* 1.546
C_Σ (J/K)	0.146* 0.064	0.074* 0.246

The ErAs: InGaAs/InAlAs thermoelement is only 10 μm thick, very thin in comparison with the top Si substrate and the AlN plates. Assuming average values of the thermal properties of InGaAs and InAlAs, the expected time constant of the individual thermoelement is about 30 μs. Unfortunately the presence of the top thick Si substrate and the top AlN plate hinders the extraction of the thermal properties of the individual thermoelements in power generator array; even though we used the high speed measurement techniques [20]. This problem can be solved by e.g. removing the top Si substrate, reducing the thickness of the top AlN plate and incorporating the thin film heater directly on the top of the AlN layer.

CONCLUSION

In this study, the transient temperature response of a 400 ErAs: InGaAlAs thermoelement power generator module was analyzed using Network Identification by Deconvolution based on linear *RC* network theory. This technique allowed us to separate the thermal resistance and thermal capacitance of the whole thermoelectric module including the AlN plates and the thermoelectric elements from those of the top Si substrate and the copper heat sink. The obtained thermal resistances and capacitances can be explained by taking into account the geometry of the device. Unfortunately, the presence of the top thick Si substrate and the top AlN plate hinders the extraction of detailed thermal properties of thermoelectric legs in the power generator array. It is possible to avoid this problem by removing the top Si substrate, reducing the thickness of the top AlN plate and incorporating the thin film heater on the top of this layer.

ACKNOWLEDGMENTS

This work was supported by ONR MURI Thermionic Energy Conversion Center.

REFERENCES

[1]: D. M. Rowe, “Handbook of Thermoelectrics”, CRC, 1995.

[2]: R. Venkatasubramanian, E. Sivola, T. Colpitts, and B. O’Quinn, Nature, **413**, 597, (2001).

[3]: T. C. Harman, P. J. Taylor, M. P. Walsh, and B. E. LaForge, Science, **297**, 2229, (2002).

[4]: D. O. Klenov, D. C. Driscoll, A. C. Gossard, and S. Stemmer, Appl. Phys. Lett, **86**, 111912, (2005).

[5]: D. O. Klenov, J. M. Zide, J. D. Zimmerman, A. C. Gossard, and S. Stemmer, Appl. Phys. Lett, **86**, 241901, (2005).

[6]: J. M. Zide, D. O. Klenov, S. Stemmer, A. Gossard, G. Zeng, J. E. Bowers, D. Vashaee, and A. Shakouri, Appl. Phys. Lett, **87**, 112102, (2005).

[7]: G. Zeng, J. H. Bahk, J. E. Bowers, J. M. Zide, A. Gossard, Y. Zhang, R. Sing, Z. Bian, A. Shakouri, W. Kim, S. L. Singer, and A. Majumdar, Proceeding of Materials Research Society Symposium, **886**, 0886-F12-06.1, (2006).

[8]: W. Kim, J. M. Zide, A. Gossard, D. O. Klenov, S. Stemmer, A. Shakouri, and A. Majumdar, Phys. Rev. Lett, **96**, 045901, (2006).

[9]: W. Kim and A. Majumdar, J. Appl. Phys, **99**, 034306, (2006).

[10]: W. Kim, S. L. Singer, A. Majumdar, D. Vashaee, Z. Bian, A. Shakouri, G. Zeng, J. E. Bowers, J. M. Zide, and A. Gossard, Appl. Phys. Lett, **88**, 242107, (2006).

[11]: D. Vashaee and A. Shakouri, Phys. Rev. Lett, **92**,106103, (2004).

[12]: Z. Bian and A. Shakouri, Appl. Phys. Lett, **88**, 012102, (2006).

[13]: P. E. Bagnoli, C. Casarosa, M. Ciampi, and E. Dallago, IEEE Transaction on Power Electronics, **13**, 1208, (1998).

[14]: V. Székely and T. V. Bien, Solid-State Electronics, **31**, 1363, (1988).

[15]: V. Székely, Microelectronics Journal, **28**, 277, (1997).

[16]: V. Székely, Microelectronics Reliability, **42**, 629, (2002).

[17]: M. Rencz, Microelectronics Journal, **34**, 171, (2003).

[18]: A. Poppe and V. Székely, Electronics Cooling, **8**, (2002).

[19]: K. Fukutani, R. Sing, and A. Shakouri, Proceeding of the International Workshop on Thermal Investigations of ICs and Systems, pp. 157-162, Nice, Côte d’Azur, France, September 27-29, (2006).

[20]: R. Singh, Z. Bian, G. Zeng, J. M. Zide, J. Christofferson, H. Chou, A. Gossard, J. E. Bowers, and A. Shakouri, Proceeding of Materials Research Society Symposium, **886**, 0886-F04-04.1, (2005).