Extraction of Power Dissipation Profile in an IC Chip from Temperature Map

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Abstract

In this paper, we present a new technique to calculate the power dissipation profile from the IC temperature map using an analogy with image processing and restoration. In this technique, finite element analysis (FEA) is used to find the heat point spread function of the IC chip. Then, the temperature map is used as input for an efficient image restoration algorithm which locates the sources of strong power dissipation non-uniformities. Therefore, for the first time we optimally solve the inverse heat transfer problem, and estimate the IC power map without involving extensive lab experiments. Our computationally efficient and robust method, unlike some previous techniques in the literature, is applicable to virtually any experimental scenario. Simulation results on a typical commercial IC device confirm the effectiveness of our proposed method.

Keywords

Thermal non-uniformity, power map, temperature map, heat point spread function, image restoration, thermal management.

Nomenclature

g temperature map (^0C)

n noise (^0C)

$\underline{f}$ power map (W/cm^2)

H heat point spread function ($^0C/W$)

I unit matrix

S shifting operator

P bilateral filter kernel size

α scalar weight

μ steepest descent step size

λ regularization parameter

Superscripts

l pixel number in vertical direction

m pixel number in horizontal direction

Subscripts

x vertical direction

y horizontal direction

k iteration index

1. Introduction

Thermal issues are one of the key factors limiting the performance and reliability of state-of-the-art electronic and optoelectronic devices and integrated circuits. As switching speed increases and device feature sizes are further miniaturized, localized heating problems are exasperated [1]. Temperature map measurement of an IC chip is a well-established and powerful technique that allows chip designers and process engineers to identify strong temperature non-uniformity (hot-spot) locations where there are fabrication failures [1-9]. However, a temperature map, by itself, often fails to provide enough information for IC thermal inspection, due to the fact that the formation of temperature non-uniformities can be highly complex. Note that, even one single hot-spot is often contributed by multiple discrete heat sources, and therefore the power dissipation profile has to be obtained and studied in order to achieve effective thermal management.

Typically, chip designers provide the power map to package engineers to calculate the temperature map of the chip taking into account thermal properties of the die and the package. Since the characteristic length scales of the transistors, various functional units, the die, and the package range from sub-microns to centimeters, accurate thermal analysis is done using sophisticated finite element solvers and multi grid algorithms. To identify fabrication or device failures, the calculated temperature map of the IC chip is compared to a measured one. For a more quantitative analysis of power dissipation and its spatial extent in the hot-spots, a novel iterative method is recently proposed where the temperature map is calculated for a series of power maps and the best match is experimentally identified [10]. However, these methods are accurate and useful only when few heat sources are in the chip. Unfortunately, in the more complex case of commercial ICs composed of numerous heat sources, the number of parameters involved becomes prohibitively large making this problem unsolvable even if the adaptive masking technique [10] is utilized. Also, very recently there have been some attempts to calculate the power map from the measured temperature map by implementing an experimental direct inverse filter [11]. This was done using extensive characterization of the dies by applying point heat sources at various locations and measuring the resulting temperature maps. However, since the measurements are noisy and the problem is *ill-posed*, the results obtained from such direct inverse filtering technique will always be suboptimal [12].

In this paper, by using an analogy with image processing and restoration, we present a fast and optimal numerical

solution to this inverse problem, which takes input from the temperature map and outputs the power map. Unlike the method in [10-11], our technique is much less sensitive to noise and outliers. The detailed algorithm is explained in Section 2, Section 3 presents an illustrative example, and concluding remarks are given in Section 4.

2. The Optimal Numeric Solution

Extracting power dissipation profile of an IC chip from its temperature map is done in two steps: one, estimating the heat point spread function and scaling function, and two, reconstructing the power map. The details of the proposed algorithm are discussed in the following subsection.

2.1 Image Processing Essence of Heat Spreading Behavior

The IC chip temperature map is essentially a superposition of the resulting temperature fields of each individual heat source. Therefore, instead of the typical and computationally very expensive method of solving the differential heat conduction equation for the complex model of the modern ICs, we characterize the heat spreading behavior as a spatial image filtering process. Such spatial filtering technique improves the computation time by a factor of more than a thousand, while accurate within $0.8C^o$ [13].

In our approach, the power map is treated as a gray value digital image which is basically a matrix of numerical representations of tonal values. As illustrated in Fig.1, the process of spatial filtering replaces the value of each pixel in the input image (power map) with a new value on the output image (temperature map).
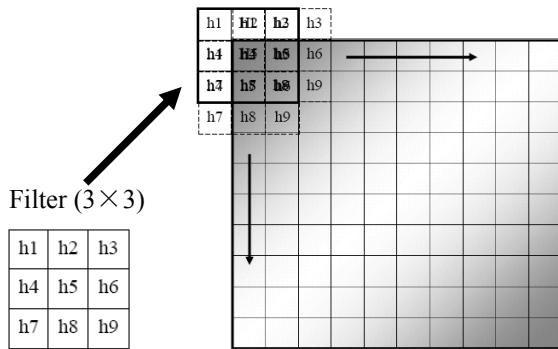

Figure 1: Concept of spatial filtering

Mathematically speaking, this is a convolution process, which can be described by the following equation

$$g(x, y) = \sum_{m,l=-a}^{a} H(m,l)f(x+m, y+l) + n(x,y),$$ (1)

where $a = (w-1)/2$ for a $w \times w$ size filter. In the case of simulating heat spreading behavior, power dissipation profile (power map) on the surface of an IC chip is represented by the matrix f. According to Equation 1, by convolving this

power map (f) with the spatial filter representing the heat point spreading function (H), the IC chip temperature map, g, is estimated. In reality, the temperature measurements are inevitably contaminated by noise, which we model as additive white Gaussian (n). Note that, when operating around the IC boundaries, a position dependant scaling function effectively scales down the heat point spread function. This scaling function can be easily estimated by using an FEA tool or a simple analytical approximation as in Ref. [13]. Figures 2-3 compare the temperature maps estimated by the FEA and the spatial filtering techniques.
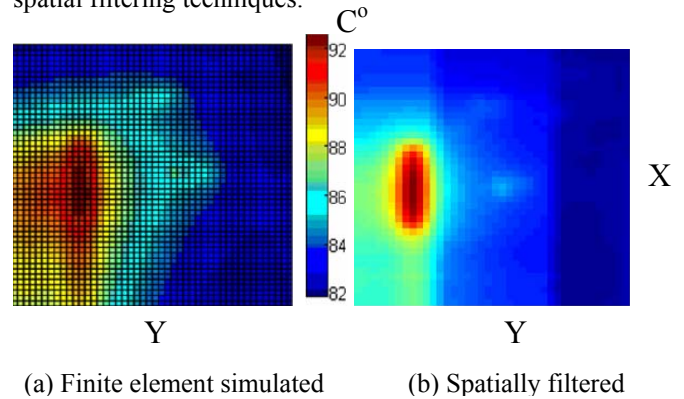

(a) Finite element simulated   (b) Spatially filtered

Figure 2: Estimated IC temperature map by (a) using FEA software (ANSYS) and (b) spatial filtering (Power Blurring) technique (Error<$0.8C^o$).
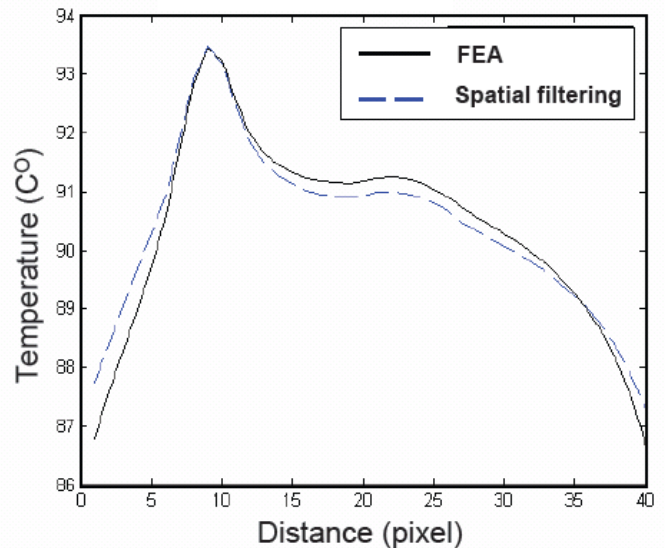

Figure 3: Estimated temperature profile along the diagonal axis using FEA and spatial filtering techniques.

2.2 Heat Point Spread Function

So far, we have shown that the computationally efficient image spatial filtering technique can be used to accurately calculate the dynamic and static temperature profiles in IC chips. In fact image blurring is a mathematically rigorous technique as the point spread function used in image analysis is the *Green's function response* of the system. The analytical Green's function can be calculated only when the sample

geometry is simple, while the point-spread function can be calculated numerically and applied to a variety of die sizes and packages. In cases where different floorplans of an IC chip are investigated, the heat point spread function can be easily parameterized for different configurations. Since the major part of the heat spreading happens in the silicon substrate, the shape of the heat point spread function does not change very much for different packages.

To find the heat point spread function, the temperature impulse response of the system is estimated via the application of a delta function power using a FEA software (ANSYS). A typical heat point spread function is shown in Figure 4.
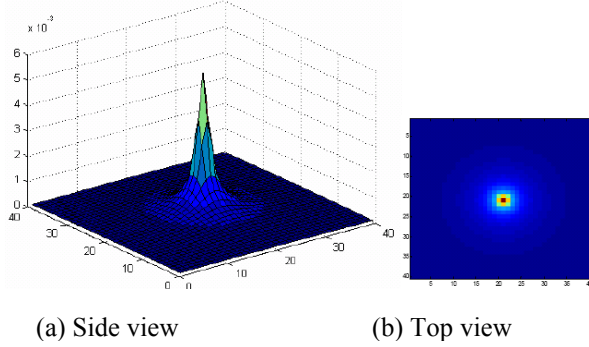

| (a) Side view | (b) Top view |

Figure 4: A 3D illustration of a typical point heat spread function estimated by a FEA software (ANSYS).

2.3 Power Trace Algorithm

In the previous section, following [13], we showed that the temperature map is related to the power map through a forward model (spatial filtering process of Equation 1). Using this forward model, in this section we define an inverse problem to estimate the IC power map from the simulated (or measured) temperature map. Our approach for solving such inverse problem is inspired from recent image restoration techniques for recovering high quality images from noisy and incomplete measurements [15].

We represent the matrix notion of (1) as

$$\underline{g} = H\underline{f} + \underline{n}, \qquad (2)$$

where H is the matrix representation of heat point spread function. Vectors $\underline{f}$, $\underline{g}$, and $\underline{n}$ represent the power map, the simulated (or measured) temperature map, and the modeling (or measurement) noise, respectively, which are rearranged in lexicographic order. With this model, least-squares approach

$$\hat{\underline{f}} = \underset{f}{\mathrm{ArgMin}}[\left\|H\underline{f} - \underline{g}\right\|_2^2] \qquad (3)$$

will result in a maximum likelihood (ML) estimate, where $\hat{f}$ is the reconstructed (estimated) power density distribution. However, such solution is not stable, which means even small amount of noise will result in large perturbations in the final solution.

Therefore, considering an efficient regularization term which delivers some general prior information for picking a stable and reliable solution in the alternative maximum *a posteriori* (MAP) framework is indeed necessary [14]. The Tikhonov [15] regularization is the most popular regularization term in the image processing literature, which forces spatial smoothness in the estimated image. However, noting that the recovered power map (f) mimics the shape of the physical heat generating elements with sharp edges (e.g. note Figure 8.a), Tikhonov regularization is not appropriate for our specific application. Alternatively, in this paper, we exploit a novel regularization term called Bilateral Total-Variation (BTV) [16], which reconstructs images with sharp edges while preserving fine details.

Such MAP cost function which outputs the localized power map is then represented as

$$\hat{\underline{f}} = \underset{f}{\mathrm{ArgMin}}[\left\|H\underline{f} - \underline{g}\right\|_2^2 + \lambda \sum_{m,l=-P}^{P} \alpha^{|m|+|l|}\left\|\underline{f} - S_x^m S_y^l \underline{f}\right\|_1] $$
$$, (4)$$

where the scalar λ is the regularization parameter, which properly weights the first term (likelihood cost) against the second term (BTV regularization cost). S_x^m and S_y^l are the operators corresponding to shifting the image represented by f by l pixels in horizontal direction and m pixels in vertical direction, respectively. The scalar weight α is applied to give a spatially decaying effect to the summation of the regularization terms, as determined by the scalar P.

The corresponding steepest descent solution of minimization can be expressed as

$$\hat{\underline{f}}_{k+1} = \hat{\underline{f}}_k - \mu\Big\{H^T(H\hat{\underline{f}}_k - \underline{g}) +$$
$$\lambda \sum_{m,l=-P}^{P} \alpha^{|m|+|l|}[I - S_y^{-l} S_x^{-m}]\mathrm{sign}(\hat{\underline{f}}_k - S_x^m S_y^l \hat{\underline{f}}_k)\Big\}, \qquad (5)$$

where μ is another scalar defining the steepest descent step size in the direction of the gradient, and $\mathrm{sign}(.)$ is a function representing the element-by-element "sign" operation (replacing the positive elements with 1, the negative elements with -1, and zero elements with 0).

3. Numerical Results

By using the algorithm described above we are able to efficiently and accurately solve the inverse heat spreading problem with high noise tolerance on the input temperature map. We demonstrate the applicability of the proposed technique by testing it on a typical commercial packaged IC chip (Figure 5). For the purpose of evaluating our results, we obtained the true power map from the designers of the IC chip, which is shown in Figure 6.
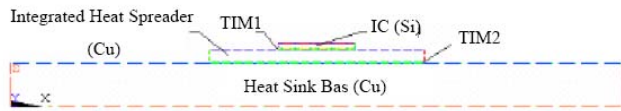
Figure 5: IC package structure and materials.

Material	Thermal Conductivity ($W/m-K$)	Density (Kg/m^3)
Silicon	117.5	2330
Copper	395	8933
TIM1	5.91	1930
TIM2	3.5	1100

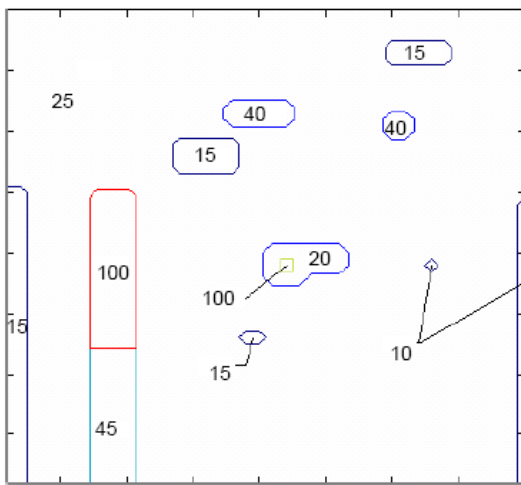**Table 1:** Material thermal properties (TIM represents thermal interface material)

Figure 6: Power map of the IC chip from design file ($1\,cm \times 1\,cm$). The regions and numbers in power profile indicate the areas where power is applied (with units of W/cm^2).
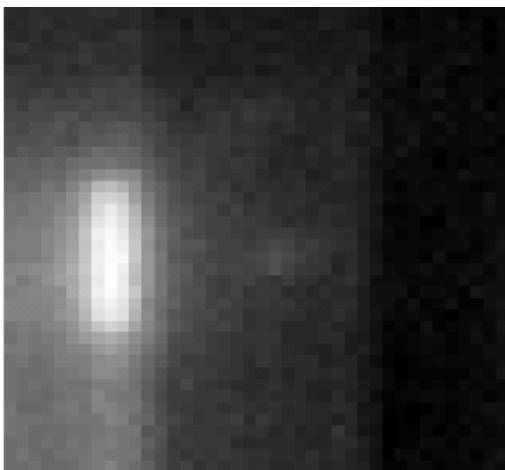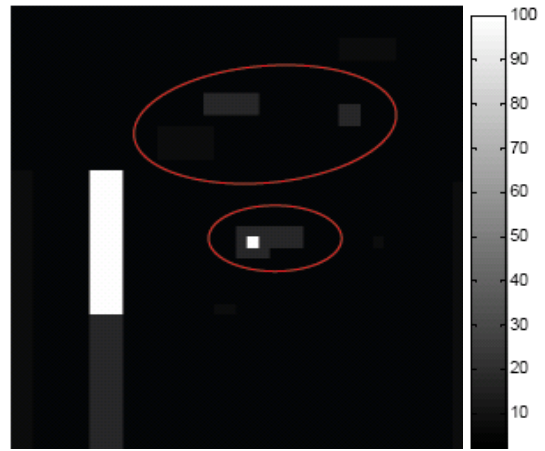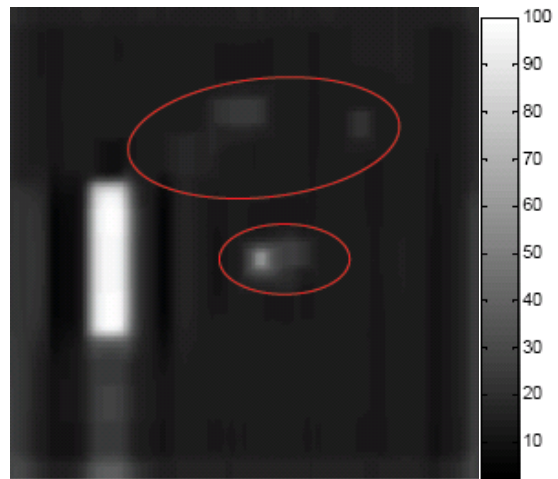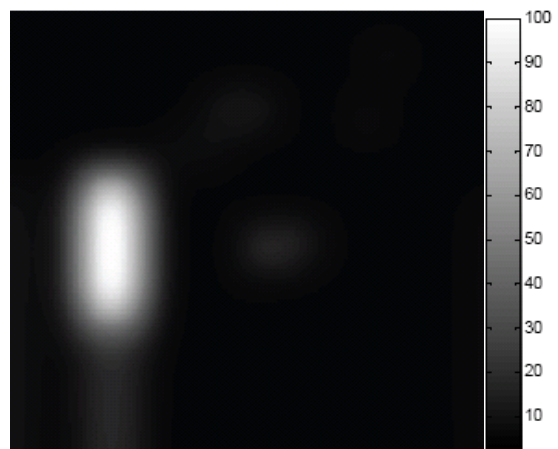

Figure 7: Temperature map of IC chip with Gaussian white noise contamination.

(a) True

(b) Power Trace

(c) Direct inverse

Figure 8: IC power maps (a) true (b) extracted using Power Trace algorithm (c) extracted using direct inverse

This flip package model consists of a $1\,cm \times 1\,cm$ silicon die IC and a Cu heat sink with an intermittent heat spreading layer surrounded by package lids. The matrix representation of the power map is defined by dividing the die on an

orthogonal mesh with congruent elements of size $0.25\,cm \times 0.25\,cm$. The material thermal properties of this chip are listed in Table 1. Further, the dominant heat transfer path is considered to be through the back of the IC chip and the Cu heat sink. We neglect the heat transfer from top of the chip through metallization layers and board, since it is a relatively small fraction of the total heat dissipation.

Following the model in (2), based on the true power map and package structure, we generated a temperature map of the IC chip (Figure 7). Zero mean Gaussian white noise with variance of one was later added to the temperature map, to simulate noise contamination.

To define the point heat spread function, we applied a 6,250 W/cm^2 heat flux to a single element of size 6.25×10^{-4} cm^2 located in the center of the IC, and waited until the temperature distribution reached the steady-state. The resulting temperature profile was normalized by the amount of heat applied to produce it, with units of $^0C/W$.

The power map of IC chip was extracted using the Power Trace algorithm that is described in Section 2.3, the result of which is shown in Figure 8(b). Comparing with Figure (a), which is the true power map in gray scale, power map extracted by using Power Trace algorithm remarkably regains the contour of most heating sources and illustrates even the very fine and tiny structures. Such fine details are not resolvable using the direct power map inverting technique of Ref. [11], illustrated in Figure 8(c).

Figure 9 shows a cross-section comparison of the true power map (blue dash line), power map extracted using the Power Trace (green solid line), power map obtained using direct inverting method (pink cross), and the input temperature map (red circle) along the center line (horizontal direction). It should be noted that the value at each pixel is represented by gray value from the image processing perspective. The power and the temperature maps are shown in arbitrary units.

4. Conclusions

In this paper, we presented a new computationally efficient and accurate IC thermal analysis technique, for estimating the power dissipation profile from the estimated (or measured) temperature map. This approach is inspired from a recent robust image restoration method [16]. The procedure for applying this new analysis tool requires two simple steps: (1) Estimating the heat point spread function by using an FEA software while using a scaling function to address the boundary problems. This step requires some knowledge about the chip and package dimension and IC's material thermal properties, which are commonly included in the chip/package design files. (2) Exploiting the estimated temperature map and solving an inverse problem to obtain the power map. The inverse problem was solved through a MAP estimation framework in which a robust regularizer is used to stabilize the solution.
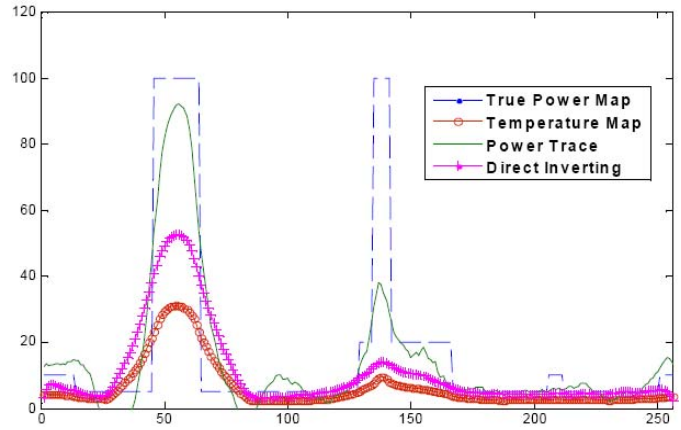

Figure 9: Cross-section comparison of true power map (blue dash line), power map extracted using Power Trace (green solid line), power map obtained using direct inverting (pink cross), and the input temperature map (red circle) along the center line (horizontal direction).

Our numerical results attest to the effectiveness of this technique for identifying the power sources of temperature non-uniformities. Our experiments were preformed on a typical commercially packaged silicon IC device, the power sources of which were unidentifiable using the state-of-the-art technique in the literature [11].

Our proposed purely software-based IC thermal analysis technique does not require sophisticated and expensive lab equipments, and is computationally very efficient. Moreover, it is extremely easy to couple or associate our proposed technique with other thermal-electrical investigating systems. Furthermore, unlike the methods in literature [10-11], our technique does not rely on calibration measurements in an actual IC chip. Also, such numerical framework makes it possible to calculate the power maps at much higher-resolution compared to the experimental based techniques. All this makes our method very suitable for practical applications. We would also like to note that by coupling our proposed technique with the in-depth temperature probing methods, such as "Infrared see through" or "Raman 3D temperature probing" [1], this 2-D technique can be extended for power mapping in 3-D.

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