Optimization of Thin Film Microcoolers for Hot Spot Removal in Packaged Integrated Circuit Chips

Kazuhiko Fukutani and Ali Shakouri*
Electrical Engineering Dept., University of California, Santa Cruz
1156 High Street, Santa Cruz, CA 95064
*ali@soe.ucsc.edu

Abstract

Hot spot removal using monolithic thin film microcoolers in a packaged chip is analyzed via an effective one-dimensional electrothermal model taking into account the three-dimensional heat and current flow in the substrate region. Various ideal and non-ideal parameters that affect the maximum cooling performance for the thin film microcoolers are discussed. Our results show that there is an optimum thin film thickness and current that give the highest cooling density at the hot spot and further thinning of thin film thickness degrades cooling performance due to finite thermal resistance between the hot side of the Si substrate and ambient, and due to electrical contact resistance. An optimally designed Si/SiGe superlattice thin film microcooler with material thermoelectric figure-of-merit, ZT, of ~0.12 is able to lower the local hot spot temperature compared to that calculated from the Si substrate with no Peltier effects. At Q_h = 300 W/cm^2 the temperature difference between the passive bulk Si substrate and thin film microcooler configuration reaches more than 7.0 ^{o}C for a hot spot 50 microns in diameter. Finally, the effect of material properties, chip to ambient thermal resistance and contact resistance on the cooling performance is also discussed. If the material *ZT* is improved by a factor of 5, hot spot temperature can be lowered by 10-30C at a heat flux of 1000W/cm^2. Seebeck coefficient improvement will have a higher impact on maximum cooling than the reduction in material's thermal conductivity or its electrical resistivity.

Keywords

"hot spot removal, superlattice, microcooler, thermoelectric coolers".

Nomenclature

S	Area [m^2]
L	Thickness [m]
I	Electrical current [A]
Q	Heat flux [W/cm^2] or Heat [W]
k	Thermal conductivity [W/mK]
T	Temperature [K]
R_{th}	Thermal resistance [K/W]
R_e	Electrical resistance [Ω]
r_{th}	Unit thermal resistance [m^2·K/W]
Z	Thermoelectric figure-of-merit [1/K]
ZT	Non-dimensional figure-of-merit

Greek Symbol:

α	Seebeck coefficient [V/K]
ρ	Electrical resistivity [Ωm]
ρ_c	Electrical contact resistivity [Ωcm^2]
Δ	Change in value

Subscripts:

SL	Superlattice thin film
sub	Substrate
ha	Heat sink to ambient
m	Junction between thin film and substrate
h	Hot spot
c	Cold side
hot	Hot side
opt	Optimum
b	Background
local	Local hot spot
a	Ambient

1. Introduction

Temperature control of microelectronic devices has become more important in recent years because power dissipation has increased substantially due to the device miniaturization and increased switching speeds. A temperature increase directly affects device's performance and reliability due to electromigration, oxide breakdown, leakage current increase, etc.. Thus, thermal management plays a vital role in integrated circuit (IC) design. According to the International Technology Roadmap for Semiconductor (ITRS) [1], a high-performance chip could dissipate as much as heat of 300 W/cm^2 by the year 2016. However, the most common cooling technology, using conventional Bismuth Telluride (BiTe) based thermoelectric coolers (TEC) with the leg thickness of millimeters, has lower cooling power density of an order of 1–10 W/cm^2 although the performance depends on the system design [2]. This value is not satisfactory for the ITRS Roadmap. Meanwhile, the maximum cooling power of thin film refrigerator is inversely proportional to the length of its elements [3]. For example, thin film coolers with the order of several microns thick are expected to provide cooling power densities larger than 1000 W/cm^2 if one neglects non-ideal effects such as metal-semiconductor contact resistance inside the TE module and the finite heat sink to ambient thermal resistance [3]. In addition, thin film material has another important advantage compared to Bulk TEC's because various methods to improve the thermoelectric figure-of-merit, ZT, value have been proposed by using superlattices and quantum dots [4-7]. On the other hand, there is another noticeable heating problem in IC chips. It is the uneven temperature distribution profile, which is called "hot spots". The temperature inside a chip can vary by 5–30 ^{o}C from one location to another. Peak flux at hot spot can reach more than six times this average value, reaching ~ 100's W/cm^2 [8]. Thus, reducing or eliminating hot spots could

lower the thermal design requirements for the whole package. One promising solution for thermal management of IC chips is hot spots removal using thin film microcoolers. In this approach high heat flux from a hot spot can be directly eliminated by a thin film microcooler monolithically integrated with ICs. Experimental results have shown that 7 ^oC cooling at 100 ^oC ambient temperature with cooling power density exceeding 600W/cm^2 is possible for unpackaged devices [9]. In addition, theoretical modeling has shown that that it is possible for SiGe thin film microcoolers with improved metal-semiconductor contact resistance and with ideal substrate to achieve a maximum cooling of 15–16 ^oC or a cooling power density over 2000 W/cm^2 [10]. However, since the cooling performance is strongly affected by the package to ambient thermal resistance [2], it is useful to predict the cooling potential of these microcoolers in packaged IC chips. In addition, the thickness of the thin film SiGe layer can be optimized for specific applications.

In this presentation, we will optimize thin film microcoolers in a packaged IC chip to maximize their cooling performance. In order to predict a maximum cooling performance and understand the sensitivity of various parameters on thin film microcooler's performances, an effective one-dimensional (1D) electrothermal model taking account the three-dimensional heat and current flow in a substrate region is developed and analyzed.

2. Calculation model

Figure 1 shows an effective 1D electrothermal model when heat flow from a hot spot is pumped out by a thin film microcooler in a packaged IC chip. In this modeling, the effect of the package is represented by a heat sink-to-ambient thermal resistance ($R_{th,ha}$), which is including interface and heat sink thermal resistances. Peltier cooling, heating and Joule heating are modeled with current sources, and consequently there are three Peltier effects and four Joule heating effects in this device. The three Peltier effects include cooling at the top metal/thin film interface (Q_1) and at the thin film/substrate (Q_2), and heating at the substrate/bottom metal interface (Q_3). The four Joule heating effects consist of heating at top metal electrode/thin film and substrate/bottom electrode interface due to contact resistances, and inside the thin film and substrate (Q_4 and Q_5). To simplify the calculation, Joule heating effects due to the contact resistances are included in the Joule heating sources inside the thin film and substrate [2]. $R_{th,SL}$ and $R_{th,sub}$ represent thermal resistances of a thin film and substrate, respectively. For the calculation of $R_{th,sub}$ and $R_{e,sub}$ taking account of three-dimensional (3D) heat and current flow, effective 1D thermal and electrical resistances (spreading resistances) were adopted instead of solving a 3D heat and current flow equation [11,12]. In addition, in case of the modeling for thermoelectric refrigerators, it is simple to show that one can always put the Joule heating current source in the middle of the thermal resistance regardless of the thermal boundary conditions at the two ends. From these modeling, the cold side temperature, T_c, can be calculated by using Kirchhoff laws if hot spot heat flux (Q_h), ambient temperature (T_a), operating current and material properties are given. Meanwhile, an actual local hot spot temperature (T_{local}) is also affected by the background heat flux (Q_b) that raises the whole chip temperature [13]. Therefore, T_{local} was calculated by taking account the effect of the background heating [13].

Material parameters for an existing Si/SiGe superlattice thin film microcooler were assumed in this study. The material parameters of SiGe thin film and Si substrate used for the calculation are as follows: $\alpha_{SL} = 3.9\times10^{-4}$ V/K, $\alpha_{sub} = 3.0\times10^{-4}$ V/K, $\rho_{SL} = 4.2\times10^{-5}$ Ωm, $\rho_{sub} = 1.8\times10^{-5}$ Ωm, k_{SL} = 8.7 W/mK, k_{sub} = 150 W/mK, which are given from experimental data [14,15]. For simplicity the temperature dependence of material properties is not taken into account in this calculation. The contact resistance between metal and semiconductor is assumed to be 10^{-6} Ωcm^2. A unit thermal resistance ($r_{th,ha}$) was assumed to be 6.138×10^{-5} m^2·K/W, assuming an ArctiCooler Model CA fan with the area contact of 9 × 11 mm^2 [16,17]. Base on this value, the heat sink to ambient thermal resistance ($R_{th,ha}$) can be calculated by the equation $R_{th,ha} = r_{th}/S_{contact}$, where $S_{contact}$ is the area of contact [16]. In all calculation, a temperature of ambient air (T_a) is also assumed to be 300 K.

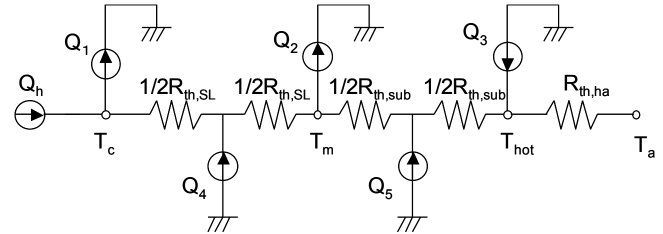

Figure 1: An effective one-dimensional electrothermal model for a thin film microcooler in a package.

3. Result and Discussion

To predict the cooling performance of the microcooler and its limitation, thin film with an area of 50 × 50 μm^2, which is located on the center of the substrate surface, and the substrate size of 1 × 1 mm^2 with a thickness of 500 μm are assumed. From the substrate geometry, the sum of the thermal resistance between the hot end of the substrate and ambient air ($R_{th,ha}$) could be calculated to be approximately 61.4 K/W based on the study by Phelan *et al*. [16]. The effects of the thin film thickness and operation current on the cooling performance of thin film microcoolers were investigated. Here, to calculate T_{local}, we assumed that hot spot Q_h = 300 W/cm^2 (ITRS requirement) and background heat Q_b = 30 W/cm^2 (Q_h/Q_b = 10). Figure 2 shows the relationship between the local hot spot temperature (T_{local}) and operating current (I) for different thin film thicknesses. One can see that T_{local} is strongly affected by the current and by the thin film thickness, indicating that there is an optimum thin film thickness and current that gives the highest cooling density to the hot spot and further thinning of thin film thickness or reducing current degrades cooling performance due to non-ideal effects such as a finite thermal resistance between the hot side of the Si substrate and the ambient, and also due to the contact resistance. Therefore, T_{local} can be minimized by adjusting both the thin film thickness and its operating current. Thin film thickness and operation current for all the thin film

microcoolers were optimized to minimize T_{local} and these devices are refereed as optimally designed thin film microcoolers in this paper.

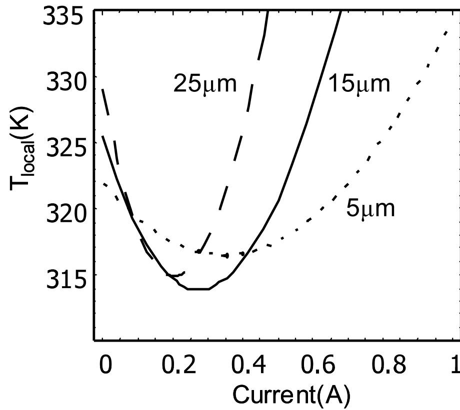

Figure 2: The relationships between T_{local} and operation current are shown for different thin film thickness.

In order to evaluate the usefulness of optimally designed thin film microcoolers whose current and thin film thickness are determined to minimize a hot spot temperature, we compared two configurations: thin film microcooler on top of silicon substrate and passive bulk Si substrate without any thermoelectric cooling (i.e. a conventional package). The results calculated from the two configurations are compared in Fig. 3.

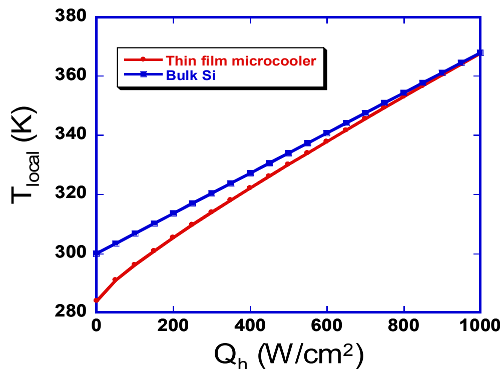

Figure 3: T_{local} calculated for thin film microcooler and bulk Si substrate cases as a function of Q_h is shown.

The figure shows the relationships between hot spot heat flux, Q_h, and the local hot spot temperature, T_{local}. As it can be seen from the graph, the optimally designed thin film microcooler is able to lower T_{local} compared to that calculated from the passive bulk Si substrate case in the entire range of this calculation although the effectiveness of the microcooler is reduced as Q_h increases. As an example, at Q_h = 300 W/cm^2 the T_{local} difference between the passive bulk Si substrate and thin film microcooler configuration reaches 7.5 ^{o}C. Therefore, it can be said that optimally designed thin film microcoolers are effective for hot spot removal in electric devices.

Figure 4 shows the value of the optimized thin film thickness (L_{opt}) calculated for different levels of Q_h. The optimized thickness decreases as Q_h increases. It indicates that at high heat fluxes thinner microcoolers are required, but that there is an optimum thin film thickness that gives the highest cooling density to the hot spot. In our calculation condition, at Q_h = 300 W/cm^2, the optimum thickness is approximately 15 μm.

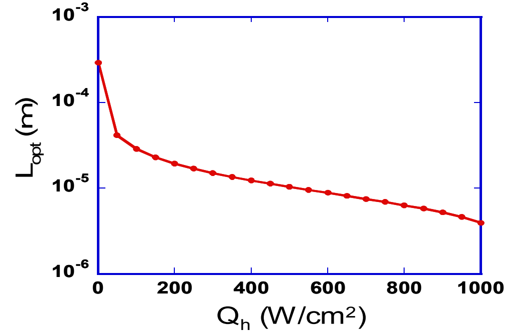

Figure 4: The optimized thin film thickness (L_{opt}) calculated for different levels of Q_h. is shown.

Figure 5 shows the optimum current and consumed power obtained for optimally designed thin film microcoolers as a function of Q_h or total heat. Since the range of optimum current is less than 0.4 A, it is not necessary to adopt multi-elements thermoelectric structures in order to reduce the operating current (this is different from bulk thermoelectric devices). The maximum consumed power is less than 50 mW in the range of this calculation, which corresponds to approximately 5% of the total heat. As it can be seen from the plot, the optimum current and consumed power increase with an increase of Q_h and decrease from some point. The reason for the current and consumed power reductions is not obvious.

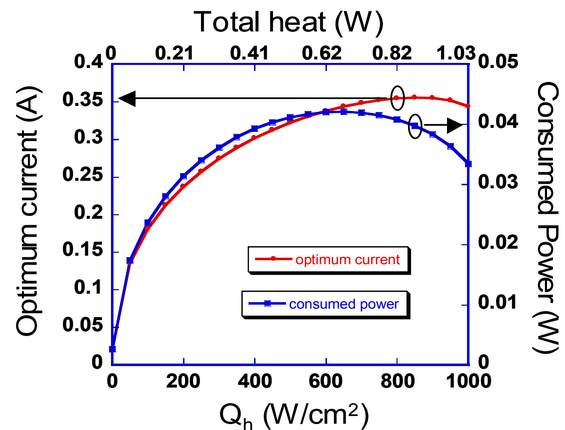

Figure 5: Optimum current and consumed power for thin film microcooler at each Q_h or total heat are shown.

Finally, the thin film microcoolers were analyzed by parametric studies to understand their limitations. Generally, TE materials are characterized by figure-of-merit, Z, which is given by the equation $Z = \alpha^2/\rho k$ [18]. α is Seebeck coefficient, ρ is electrical resistivity and k is thermal conductivity. In

general, the higher ZT of materials translate directly to either larger cooling capacity or larger cooling temperature differences (ΔT) or higher cooling efficiency [18]. Figure 6 shows the predicated cooling performance of optimally designed thin film microcooler with various ZT values. Here, the relationships between Q_h and T_{local} are shown. As shown in the equation of Z, it is possible to change Z by controlling three material properties: α, ρ and k. To understand how each parameter affects the cooling performance, when one parameter is varied to increase Z and the other two parameters are kept constant. In this comparison, ZT is assumed to be improved by a factor of 5 compared to the current value (ZT = 0.125). The thickness and area of the Si substrate are assumed to be 500 μm and 1000 × 1000 μm^2, respectively. For the purpose of comparison, the plot for the optimally designed thin film cooler with $ZT = 0.125$ (current technology value) is also shown in the same graph. We can see a huge T_{local} reduction by increasing ZT. However, even if the value of ZT is identical, the T_{local} obtained from the microcoolers with different material parameters are clearly different. The effect of decreasing ρ and k on T_{local} is the exactly the same, but the effect of increasing α on the reduction of T_{local} is much lager than that of decreasing ρ and k. It can be said that the Seebeck coefficient of thin film materials is more important factor to maximize the cooling performance in thin film microcoolers than thermal conductivity and electrical resistivity when thin film thickness and operation current are optimized. Therefore, ZT is no longer a good indicator for discussing how good the device performance is in case of optimally designed thin film microcooler in a package.

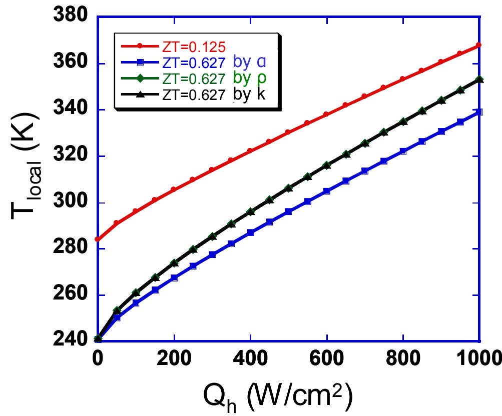

Figure 6: T_{local} as a function of Q_h when ZT is changed by any of α, ρ and k.

It was previously noted that the value of $R_{th,ha}$ has a significant impact on the cooling performance of thermoelectric coolers [2,16,19,20]. The effect of $R_{th,ha}$ on T_{local} was investigated. Figure 7 shows the relationships between Q_h and T_{local} at various $R_{th,ha}$. Optimally designed thin film microcoolers with $R_{th,ha}$ = 30.7 (a factor of 2 lower), 61.4 (current technology value) and 122.8 K/W (a factor of 2 higher) were assumed. For the purpose of comparison, the results obtained from the passive bulk Si substrate case similar to Fig. 3 are shown in the same graph. Absolute values of T_{local} decrease with a decrease of $R_{th,ha}$ for all plots because with low $R_{th,ha}$ it is possible to dissipate high heat flux to the ambient. Hot spot temperature reduction with the microcooler also increases with a decrease of $R_{th,ha}$. Therefore, it can be said that reducing $R_{th,ha}$ will enhance the cooling performance of microcoolers. Meanwhile, one can see that there is no merit to fabricate thin film microcoolers on the substrate when hot spot fluxes are lager than 800 W/cm^2 for the microcooler with $R_{th,ha}$ of 122.8 K/W, indicating higher $R_{th,ha}$ reduces the effectiveness of the thin film microcoolers.

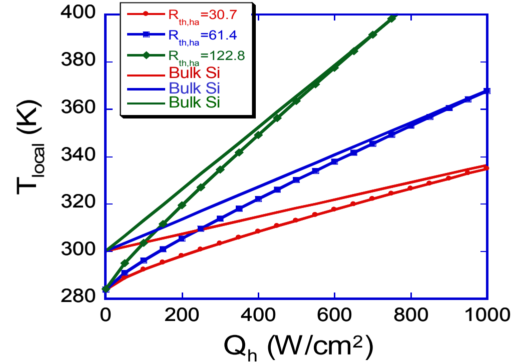

Figure 7: T_{local} as a function of Q_h is shown when $R_{th,ha}$ is changed.

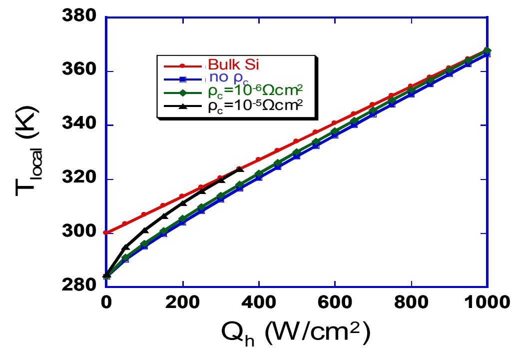

Figure 8: T_{local} as a function of Q_h is shown when contact resistivity is changed.

The effect of the contact resistance on the cooling performance was also investigated. The results calculated by different contact resistivity are shown in Fig. 8. For the purpose of comparison, the plots calculated for a passive bulk Si substrate and thin film microcooler assuming no contact resistance are also shown in the same graph. T_{local} obtained from the thin film microcooler with $\rho_c = 10^{-6}$ Ωcm^2 is not so different from that obtained from a microcooler without a contact resistance. On the other hand, the curve for $\rho_c = 10^{-5}$ Ωcm^2 rapidly approaches to T_{local} calculated from a passive bulk Si substrate case and at approximately Q_h = 350 W/cm^2 the difference becomes almost zero. Since the optimum thin film thickness becomes smaller when Q_h increases, the contact resistance which induces an additional Joule heating

becomes significant for the cooling performance as Q_h is larger.

4. Conclusion

Thin film microcoolers integrated with a heat sink were analyzed by an effective one-dimensional electrothermal model. The optimally designed thin film microcoolers with existing sink to ambient unit thermal resistance ($r_{th,ha}$ = 6.138 × 10^{-5} m^2·K/W), whose current and thin film thickness are determined to minimize the hot spot temperature, can cool 7.5 ^oC at a hot spot heat flux of 300 W/cm^2, compared to the hot spot temperature calculated from the passive bulk Si substrate case. The effects of *ZT* of thin film and substrate materials, heat sink to ambient thermal resistance and contact resistance on cooling performance are examined. The modeling results show that hot spot cooling could be improved by increasing *ZT* of the thin film material, and by decreasing heat sink to ambient thermal resistance. Especially, if Seebeck coefficient of thin film material can be increased while keeping electrical resistivity and thermal conductivity constant, hot spot cooling can be more enhanced than *Z* increased by thermal conductivity or electrical resistivity reduction. The effect of contact resistance on the cooling performance is small if the contact resistivity is less than 10^{-6} Ωcm^2.

References

1. http://public.itrs.net/ :International Technology Roadmap for Semiconductor 2004.
2. K. Fukutani, A. Shakouri, "Optimization of Bulk Thermoelectric Modules for Chip Cooling Applications", Proceedings of InterPack2005, San Francisco, CA, July 17-22, Paper IPACK2005-73410, K. Fukutani, A, Shakouri, IEEE Transaction on Components and Packaging Technologies, to be published.
3. J. Vandersande, J. Fleurial, "Thermal Management of Power Electronics Using Thermoelectric Coolers", Proceeding of the 15th International Conference on Thermoelectrics, pp. 252-255, 1996.
4. L. D. Hicks, M. S. Dresselhaus, "Thermoelectric figure of merit of a one-dimensional conductor", Phys. Rev. Lett., 47, pp. 16631, 1993.
5. D. Vashaee, A. Shakouri, "Improved Thermoelectric Power Factor in Metal-Based Superlattices", Phys. Pev. Lett., 92, pp. 106103, 2004.
6. G. Chen, A. Shakouri, "Heat transfer in nanostructures for solid-state energy conversion," Journal of Heat Transfer-Transactions of the ASME, vol.124, no.2, pp. 242-252, 2002.
7. T.C. Harman, P.J. Taylor, M.P. Walsh, and B.E. LaForge, " Quantum Dot Superlattice Thermoelectric Materials and Devices", Science 297, pp. 2229-2232, 2002.
8. G. M. Chrysler, "Building blocks for thermal management of electronics", in Next-Generarion Thermal Management Materials and Systems for cooling and power conversion, Technology Venture Forum, Irving Texas, Oct. 28-30th, 2002.
9. X. Fan, G. Zeng, C. LaBounty, J. E. Bowers, E. Croke, C. C. Ahn, S. Huxtable, A. Majumdar, A. Shakouri, "SiGeC/Si superlattice microcoolers", Appl. Phys. Lett., 78, pp. 1580-1582, 2001.
10. D. Vashaee, J. Christofferson, Y. Zhang, A. Shakouri, G. Zeng, C. LaBounty, X. Fan, J. Piprek, J. E. Bowers, E. Croke, "Modeling and optimization of single-element bulk SiGe thin-film coolers", Microscale Thermophysical Engineering, Vol. 9, pp. 99-118, 2005.
11. S. Song, S. Lee, V. Au, "Closed-Form Equation for Thermal Constriction/Spreading Resistance with Variable Resistance Boundary Condition", IEPS Conference, pp. 111-121, 1994.
12. S. Lee, S. Song, V. Au, K. P. Moran, "Constriction/Spreading Resistance Model for Electronics Packaging", ASME/JSME Thermal Enginnering Conference, pp. 199-205, 1995.
13. K. Fukutani, Y. Zhang, A. Shakouri, to be published.
14. S. T. Huxtable, A. R. Abramson, C. Tien, A. Majumdar, C. Labounty, X. Fan, G. Zeng, J. E. Bowers, A. Shakouri, E. T. Croke, "Thermal conductivity of Si/SiGe and SiGe/SiGe superlattices", Appl. Phys. Lett. 80, pp. 1737-1739, 2002.
15. Y. Zhang, G. Zeng, J. Christofferson, E. Croke, J. E. Bowers, A. Shakouri, "Measurement of Seebeck coefficient perpendicular to SiGe superlattice", Proceeding of 21st International Conference on Thermoelectrics, August, 2002, Long Beach, California, USA.
16. P. E. Phelan, V. A. Chiriac, T. Y. Lee, "Current and Future Miniature Refrigeration Cooling Technologies for High Power Microelectronics", IEEE Transaction on Components and Packaging Technologies, Vol. 25, No. 3, pp. 356-365, 2002.
17. G. Wagner, "Optimization of the ArctiCooler for Lowest Thermal Resistance in a Minimum Volume", Inter Society Conference on Thermal Phenomena, pp. 180-184, 2000.
18. D. M. Rowe, CRC Handbook of Thermoelectrics, (New York, CRC, 1995).
19. R. Simons, R. Chu, "Application of Thermoelectric Cooling to Elecric Equipment: A Review and Analysis", 16th IEEE SEMI-THERM Symposium, pp. 1-9, 2000.
20. G. Solbrekken, K. Yazawa, A Bar-Cohen, "Chip Level Refrigeration of Portable Electronic Equipment Using Thermoelectric Devices", Proceedings of InterPack2003, Maui, HA, Jul 6-11, Paper IPACK2003-35305, R. Taylor, G. Solbrekken, "An Improved Optimization Approach for Thermoelectric Refrigeration Applied to Portable Electronic Equipment", Proceedings of InterPack2005, San Francisco, CA, July 17-22, Paper IPACK2005-73190.