Three-Dimensional Electro-Thermal Modeling of Thin Film Micro-Refrigerators for Site-Specific Cooling of VLSI ICs

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Abstract

Non-uniform high temperature distribution has become a primary concern in view of VLSI performance and reliability. This problem becomes much severer in the nanometer-scale technologies as the required operating frequency moves into the multi-giga Hertz range. Effective handling of "hot spots" is an important issue. Recently, a cooling technology based on heterostructure integrated thermionic (HIT) micro-refrigerator has been proposed as one of possible on-chip thermal management solutions. Since high temperature can severely impact VLSI performance and reliability, it is important to obtain on-chip temperature profiles of VLSI chips together with micro-refrigerators attached. This paper, for the first time, presents a detailed three-dimensional modeling and FDM analysis of single thin film micro-refrigerator integrated onto a chip. The model takes into account of the Peltier cooling and heating, Joule heating, and heat conduction. The new model has been validated by verifying the maximum cooling and device's power consumption with experimental data and ANSYS simulation results.

Key words: electro-thermal analysis, micro-refrigerator, Peltier effect, Seebeck coefficient, and finite difference method (FDM)

1. Introduction

The state-of-the-arts high density CMOS chips at high frequency consumes large power. Extensive efforts have been devoted to lower the overall on-chip temperature. However, effective handling of "hot spots" is an important emerging issue because they can significantly degrade reliability and chip performance [1, 2]. To mitigate this problem, site-specific cooling technologies are required. Recently, a cooling technology based on heterostructure integrated thermionic (HIT) micro-refrigerator has been proposed as one of the possible solutions [3]. This cooling technology has advantages over other cooling technologies as it enables monolithic integration for site-specific cooling, especially, for CMOS VLSI circuits. SiGe superlattice devices have achieved 7°C cooling at 100°C ambient temperature and cooling power densities exceeding 500W/cm^2 [4, 12].

For accurate analysis of performance and reliability of VLSI ICs, thermal profiles of chips are indispensable. Methodologies for electro-thermal modeling of VLSI chips have been published in the literature [1, 5]. However, obtaining accurate temperature profiles of VLSI chips with micro-refrigerators attached is not a simple task. One dimensional modeling of thermoelectric coolers and thin film micro-refrigerator was attempted [6, 7] but one-dimensional model can only predict the temperature at the specified position. Thus, it can not be applied to find temperature profile over a large chip area.

In this paper, using finite difference method (FDM), a detailed 3-D modeling and analysis of single thin film micro-refrigerator integrated onto a chip is presented.

The remainder of the paper is organized as follows. In Section 2, basic principles for thermoelectric cooling are reviewed. Section 3 describes three-dimensional electro-thermal modeling methodology. Simulation results will be presented in Section 4, followed by conclusions in Section 5.

2. Background

2.1 The Thermoelectric Effects

Thin film micro-refrigerators are similar to thermoelectric (TE) coolers. However, micro-refrigerators are based on a superlattice-enhanced thermionic emission process. In this process, hot electrons from a cathode layer are selectively emitted over a barrier to an anode junction. This causes evaporative cooling of the cathode layer. Two main interactions between heat and electricity are the Seebeck and Peltier effects. An open-ended solid develops electrical potential between two ends when there exists a temperature gradient along the solid, which is known as the Seebeck effect and the Seebeck coefficient is defined as the ratio between potential difference and temperature difference, $S = \Delta V / \Delta T$ (V/K). The Seebeck effect reflects that electrical and thermal current (heat) are coupled.

When two different materials are in contact, and an electrical current is flowing through the junction, heat is generated or absorbed at the junction, which is known as the Peltier effect. Depending on whether heat is absorbed or generated, cooling or heating occurs. The Peltier cooling or heating power is given by $P = (S_1 - S_2) \cdot T_j \cdot I$, where S_1 and S_2 are the Seebeck coefficients of the material 1 and 2, respectively, Tj is the junction temperature in Kelvin, and I is the electrical current. The sign of $(S_1 - S_2)$ and the direction of the current determine the occurrence of either heating or cooling at the junction [9].

2.2 Cooling Power and Figure of Merit

An example of one-dimensional thermoelectric cooler is shown in Fig. 1. Two dissimilar materials, A and B, are in contact making two junctions, and the current I flows though them. Let us assume that cooling occurs at the first junction and heating occurs at the second junction (Q_c and Q_h are cooling and heating powers, respectively). Then, the cooling power at the first junction is affected by the Joule heating inside material B, and the heat conduction from the second junction. Thus, the effective cooling power for one-dimensional thermoelectric cooler can be written as [10]

$$Q_{c_eff} = (S_A - S_B)T_1 I - \eta I^2 R_B - \frac{T_2 - T_1}{Rth_B} \quad (1)$$

where, S_A and S_B are the Seebeck coefficients of material A and B, respectively, T_1 and T_2 are the junction temperatures, R_B is the electrical resistance of material B, Rth_B is the thermal resistance of material B, and η is the contribution factor. The first term is for the Peltier cooling, the second term for the contribution from the Joule heating, and the last term for the heat conduction from the hot junction.

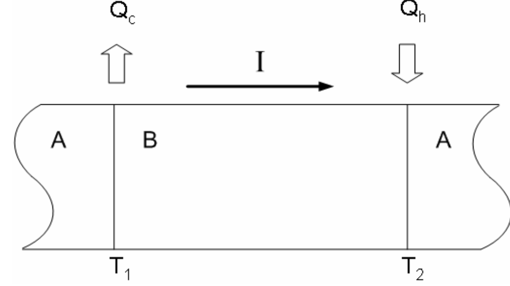


Fig. 1. An example of one-dimensional thermoelectric cooler. Q_c and Q_h are cooling and heating powers, respectively. Electric current *I* is flowing through two junctions between material A and B.

To get a better cooling effect, we need to minimize the Joule heating and the heat conduction from the hot junction. For characterization of thermoelectric material, the figure of merit, ZT, below is widely used:

$$ZT = \frac{S^2 \sigma T}{k} \quad (2)$$

where, S is the Seebeck coefficient, σ is the electrical conductivity, k is the thermal conductivity, and T is the absolute temperature. The higher the ZT value, the better the cooling. For high value of ZT, a material with both high electrical conductivity and low thermal conductivity is desired. However, usually a good electrical conductor is also a good thermal conductor. Thus, it is very difficult to obtain ZT value higher than 1. It has been reported that the ZT value higher than 1 can be achieved using a BiTe/SbTe superlattice structure grown by Molecular Beam Epitaxy (MBE) [11]. However, BiTe is not compatible with silicon integrated circuits. SiGe superlattices have lower ZT value at room temperature but they can be monolithically integrated with silicon devices. Thin film micro-refrigerators using SiGe superlattice structure have been fabricated and measured [12]. They can be fabricated on silicon wafer and thus are good candidates for spot-cooling solution of VLSI chips.

2.3 The Structure of the Micro-Refrigerator

Our goal in this work is to obtain a temperature profile of a chip which is attached to a micro-refrigerator. A three-dimensional schematic of a micro-refrigerator in two-chip configuration is shown in the Fig. 2. The bottom block is the substrate on which the micro-refrigerator is fabricated,

and the top block is the chip to be cooled. Between the chip and the substrate, the micro-refrigerator is located. Basically, the micro-refrigerator is composed of many different thin layers. A cross-sectional view and a top view of the overall structure are shown in Fig. 3 and 4, respectively.

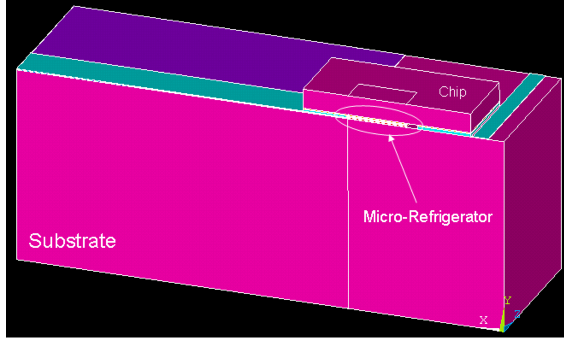


Fig. 2. 3-D schematic of the micro-refrigerator in two-chip configuration (due to symmetry, only half of the structure is shown) [3].

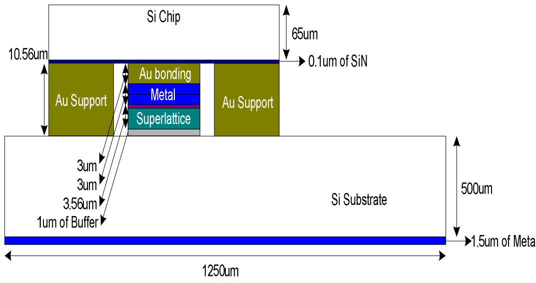


Fig. 3. Cross-sectional view of the micro-refrigerator in two-chip configuration.

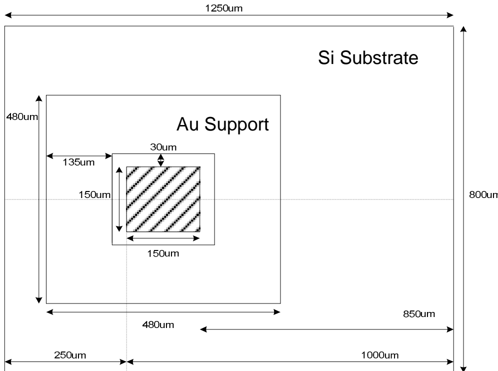


Fig. 4. Top view of the micro-refrigerator in two-chip configuration (silicon chip is not shown).

3. 3-D Electro-Thermal Modeling

3.1 Heat Conduction and Finite Difference Approximation

Governing equation for heat conduction is given by [13]

$$k\frac{\partial^2 T(x,y,z,t)}{\partial x^2}+k\frac{\partial^2 T(x,y,z,t)}{\partial y^2}+k\frac{\partial^2 T(x,y,z,t)}{\partial z^2}+q^* = \rho c_p \frac{\partial T(x,y,z,t)}{\partial t} \quad (3)$$

where, k is the thermal conductivity, ρ is the density, and c_p is the specific heat, q^* is the heat generation per volume, and $T(x, y, z, t)$ is the temperature of the position (x, y, z) at time t. Equation (3) represents the energy conservation. In steady state, Equation (3) becomes

$$k\frac{\partial^2 T(x,y,z)}{\partial x^2}+k\frac{\partial^2 T(x,y,z)}{\partial y^2}+k\frac{\partial^2 T(x,y,z)}{\partial z^2}+q^*=0 \quad (4)$$

For numerical analysis, Equation (4) can be approximated by a Taylor's series, which is known as the Finite Difference Method (FDM). The approximated equation is given by

$$\begin{aligned}&\frac{k\Delta y\Delta z}{\Delta x}\left[T(x+\Delta x)-2T(x)+T(x-\Delta x)\right]\\&+\frac{k\Delta x\Delta z}{\Delta y}\left[T(y+\Delta y)-2T(y)+T(y-\Delta y)\right]\\&+\frac{k\Delta x\Delta y}{\Delta z}\left[T(z+\Delta z)-2T(z)+T(z-\Delta z)\right]+q=0\end{aligned} \quad (5)$$

where, q has the unit of power, and $\Delta x, \Delta y, and\ \Delta z$ are the incremental distances in x, y, and z directions. The coefficient of each term is the inverse of the thermal resistance of the volume in the direction of heat flow. Thus, we can get

$$\begin{aligned}&\frac{\left[T(x+\Delta x)-2T(x)+T(x-\Delta x)\right]}{Rth_x}\\&+\frac{\left[T(y+\Delta y)-2T(y)+T(y-\Delta y)\right]}{Rth_y}\\&+\frac{\left[T(z+\Delta z)-2T(z)+T(z-\Delta z)\right]}{Rth_z}+q=0\end{aligned} \quad (6)$$

Equation (6) is a discrete equation which is valid for only certain points in the space. If we regard the temperature and the heat as voltage and current, Equation (6) can be regarded as a statement of Kirchoff's Current Law (KCL) in electrical circuit theory. The net heat flow at a certain node should be zero.

3.2 Boundary Conditions

Following the experimental setup [3, 4], the bottom of the substrate is set to 353 K (the bottom of the substrate is in contact with temperature con-

trolled stage, which is set to 353K (80°C)) and the ambient temperature is 300K (room temperature). For the surfaces in contact with the air, natural convection is assumed (heat transfer coefficient of $10\times10^{-12}(watt/\mu m^2\cdot K)$ [14]).

3.3 Material Parameters

Table 1. Material Parameters for Si/SiGe supperlattice [4, 8]

	Metal	SiNx	Si	Buffer	Super-lattice	Cap
Thermal Conductivity (W/mK)	200	1	125	6.5	6.5	8
Resistivity (Ohm-cm)	1.0e-5	1000	0.001	0.0016	0.0016	0.02
Seebeck Coefficient (µV/K)	0		325		200	

3.4 Conductance Matrix

Using Equation (6), the thermal problem can be treated in the same way as an electrical problem. To this end, the equivalent circuit of the structure using thermal resistors needs to be constructed. The whole structure is broken into small segments and each segment is represented by a node. Then, each node is connected to neighboring nodes with thermal resistors. An example is shown in Fig. 5. T(i,j,k) and the current source represent the node temperature and the heat current, respectively.

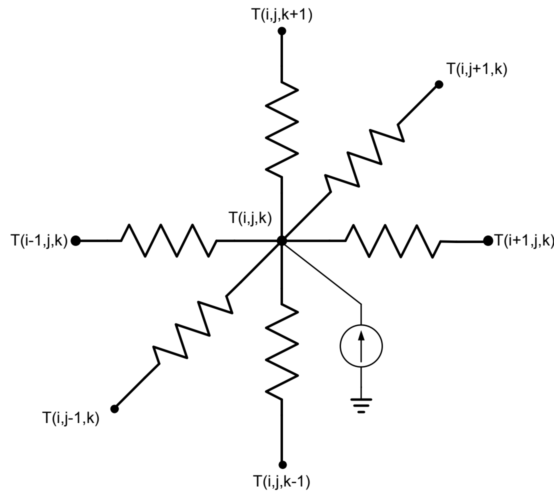


Fig. 5. Thermal resistance network from the view point of a node (i,j,k) for temperature calculation.

According to Equation (6), the sum of all the heat currents at the center node should be zero, and this equation should be valid for all nodes inside the structure. Thus, we eventually obtain a system of equations, each of which is in the form of Equation (6). The system of equations can be transformed into a matrix equation in the form of

$$A\cdot T=B \tag{7}$$

The A is a square matrix and T and B are vectors. The matrix A contains the coefficient of each term except "q" in Equation (6), which is equivalent to the thermal conductance. The vector B contains the heat flowing into or out of each node. The solution of Equation (7), T, provides information on the temperature distribution in the structure.

3.5 Cooling and Heating Power

For simulation of the micro-refrigerator, we need to consider both cooling and heating powers. In Fig. 6, all the power components are specified. An electrical current is applied to the top metal contact, and returns through the bottom metal contact after passing through the superlattice and the substrate.

As stated before, the Peltier effect causes both cooling and heating. The Peltier cooling occurs at two junctions (one between metal and superlattice, and the other between superlattice and substrate). On the other hand, the Peltier heating occurs at the junction between the substrate and the bottom metal contact. The sum of cooling powers should be less than the heating power.

When a current flows through a solid, the Joule heating occurs internally. If a current flows through the solid uniformly, the Joule heating can be easily calculated using a one-dimensional electrical resistance. However, the current flow in the substrate is non-uniform, and thus a one-dimensional resistance is not appropriate. The current spreading effect needs to be taken into account for the Joule heating inside the substrate.

The calculation of the Joule heating considering the current spreading requires calculation of the potential distribution. To this end, an electrical resistance network needs to be constructed. This can be easily implemented by replacing the thermal resistance with an electrical resistance once the thermal resistance network is constructed. In Fig. 7, the substrate and its electrical resistance network are shown. Let us assume that a current is applied through the dark area on the top of the substrate. In the electrical model, a group of current sources represent applied currents, each of which has a current value proportional to the effective area of corresponding node. Hence, the potential distribution can be obtained in the same manner as the temperature distribution is obtained.

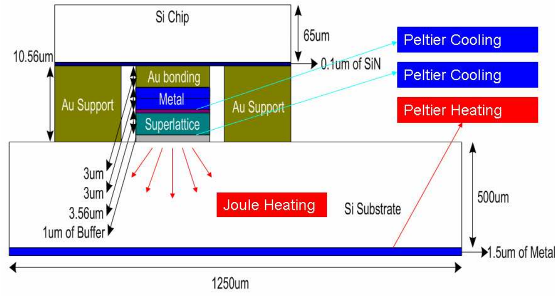


Fig. 6. Power components for electro-thermal simulation: (1) Peltier cooling at the two junctions (one between the top metal and the superlattice, and the other between the superlattice and the substrate) (2) Peltier heating at the junction between the substrate and the bottom metal (3) Joule heating in the electrical current path.

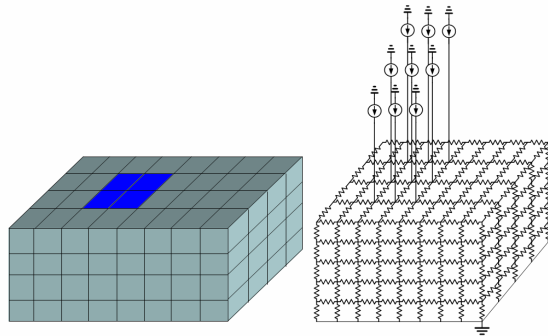


Fig. 7. Silicon substrate and its equivalent circuit for calculation of Joule heating.

In Fig. 8, the potential distribution on the surface of the substrate is shown when the input current is 350mA. Once the potential distribution inside the substrate is identified, the Joule heating can be calculated as follows.

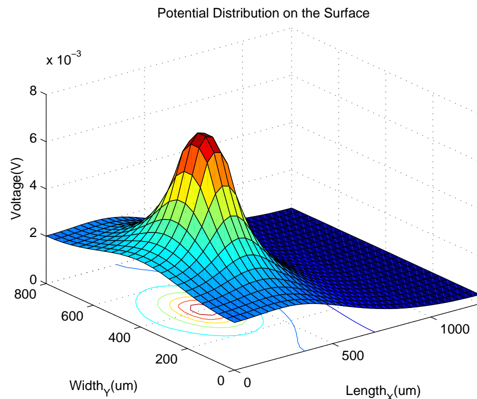


Fig. 8. An example of potential distribution in the substrate.

We consider the Joule heating for a certain node inside the substrate as shown in Fig. 9. Each node has six neighboring nodes at the most. Between the center node (i,j,k) and neighboring nodes, electrical current values are given by,

$$I_n = \frac{V(i,j,k) - V_n}{R_n} \tag{9}$$

where, n=1,2,3,4,5,6. Hence, the total Joule heating corresponding to the node (i,j,k) can be written as

$$P_{Joule}(i,j,k) = \sum_{n=1}^{6} \frac{1}{2} \frac{(V(i,j,k) - V_n)^2}{R_n} \tag{10}$$

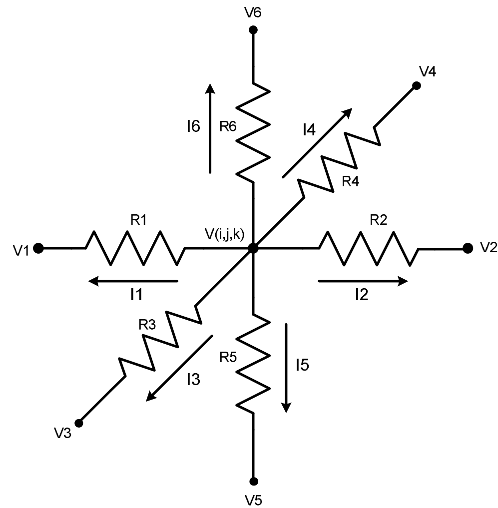


Fig. 9. Electrical resistance net for the calculation of Joule heating.

4. Simulation Results and Discussion

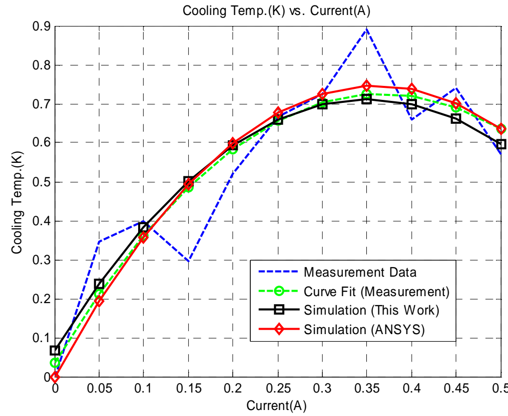
Based on the methods described above, an electro-thermal simulator was built with C language in Windows platform. Direct linear system solver based on LU decomposition and back-substitution was used [15].

4.1 Cooling Temperature and Power

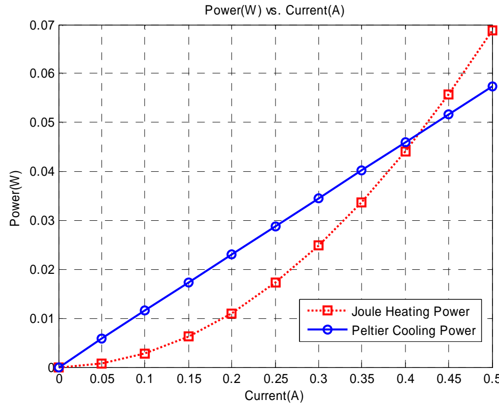
Fig. 10 (a) shows the cooling temperature vs. the applied current (cooling temperature is defined as temperature difference between the chip and the temperature controlled stage). The simulation results are in good agreements with the experimental data [3, 4] and ANSYS [16] simulation results. Fig. 10 (b) shows the cooling and heating powers vs. the applied current.

The Peltier cooling and heating powers depend on the Seebeck coefficients and the applied current. The Seebeck coefficients are the material parameters. Hence, the Peltier cooling and heating powers are linear functions of the applied current.

The straight line in the figure represents the Peltier cooling power (the Peltier heating power is same in magnitude as the Peltier cooling power, but with opposite sign). On the other hand, the Joule heating power shows a quadratic dependence on the applied current, as expected.



(a)



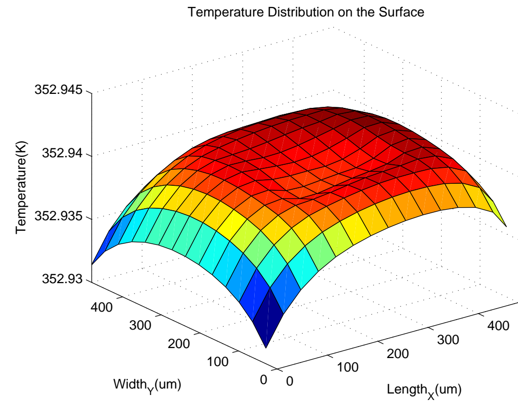
(b)

Fig. 10. (a) Cooling temperature comparison with measurement data, (b) Peltier cooling and Joule heating powers vs. applied current (Peltier heating power has the same amount as Peltier cooling power with opposite sign).

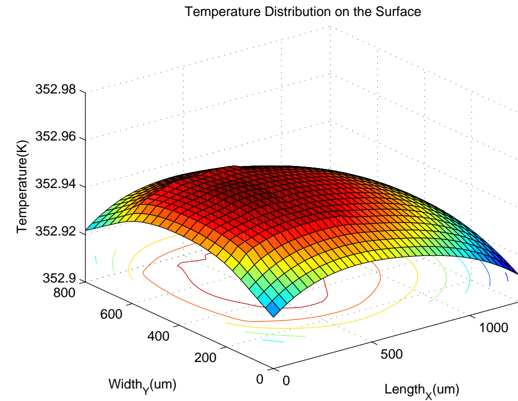
Maximum cooling occurs at around 350mA. However, the dominance of the Joule heating power over the Peltier cooling power happens at around 400mA. This is due to the contribution of the Peltier heating power at the bottom junction between the substrate and the metal in Fig. 6, which results in the third term in Equation (1).

4.2 Temperature Distribution without Active Cooling

Fig. 11 shows temperature distributions on the surfaces of the chip and the substrate when the micro-refrigerator is off. Without active cooling, the temperature of the whole structure will be close to the temperature-controlled stage temperature in steady state. Due to the natural convection boundary conditions, the nodes around the periphery have lower temperatures than those in the center. However, the difference is negligible.



(a)



(b)

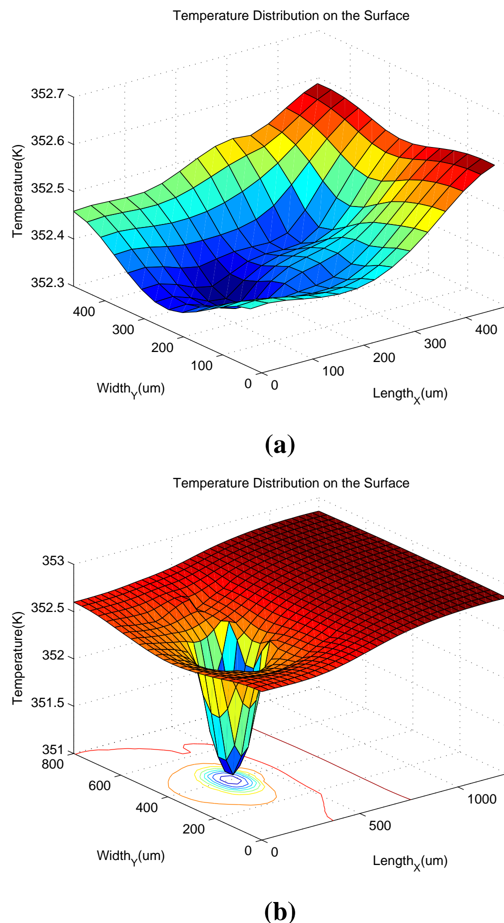
Fig. 11. Temperature distributions with the micro-refrigerator off; (a) on the surface of the chip, and (b) on the surface of the substrate.

4.3 Temperature Distribution with Active Cooling

In Fig. 12, temperature distributions on the surfaces of the chip and the substrate are shown when the input current for the micro-refrigerator is 350mA (maximum cooling point). Due to the Peltier cooling, the center regions close to the cooler have lower temperature than those in periphery in Fig. 12 (a).

5. Conclusion

In this paper, a three-dimensional modeling methodology for a single micro-refrigerator in two chip configuration was presented. Based on the analogy between electrical and thermal problems, equivalent thermal resistance and electrical resistance networks were built for numerical analysis using the FDM method. A methodology for calculation of the Joule heating considering non-uniform current flows in the substrate was proposed. Cooling temperatures obtained by simulation using our proposed model show good agreements with the experimental data and the ANSYS simulation results.



(b)

Fig. 12. Temperature distributions with the micro-refrigerator on (the input current: 350mA); (a) on the surface of the chip, and (b) on the surface of the substrate.

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