Ultra Fast Calculation of Temperature Profiles of VLSI ICs in Thermal Packages Considering Parameter Variations

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Abstract

Due to the aggressive scaling down of the CMOS technology, VLSI ICs become more and more vulnerable to the effect of non-uniform high temperatures which can significantly degrade chip performance and reliability. Therefore, we are interested in surface temperature profiles of VLSI ICs. In IC thermal analysis, heat conduction equation is conventionally solved by grid-based methods which are computationally expensive. To reduce the computation time, we developed a matrix convolution technique, Power Blurring (PB). It calculates the steady-state temperature profile with maximum temperature errors less than 1% for various types of power distributions. It requires a spatial impulse response, called the thermal mask, which can be obtained by using Finite Element Analysis (FEA) tools such as ANSYS. The thermal mask is a function to be convoluted with power distribution for temperature profile. Thus, the PB method uses FEA repeatedly for the changes in parameters of thermal packages such as thermal conductivity, convection heat transfer coefficient, and silicon substrate thickness to obtain new thermal mask. Our test structure is divided into 49,323 elements of which 1600 correspond to the surface of the silicon substrate. Performing FEA repeatedly is time consuming. In this paper, we will describe the PB method and propose a method for parameterization of the thermal mask to avoid many FEA simulations under parameter variations. The PB method using parameterized mask yields maximum error less than 2.3% for various case studies and reduces computation time from 17 seconds to 0.1 second for our test structure.

Key words: Power Blurring (PB), thermal package, temperature profile, thermal mask parameterization, and finite element analysis (FEA)

1. Introduction and Background

As MOSFET feature sizes decrease and on-chip power density increases, non-uniform temperature rise in VLSI chips has drawn our attention because chip performance and reliability are strong functions of chip temperature distribution. For accurate estimations of performance, reliability, and power consumption, precise thermal profile is indispensable. To obtain a steady-state thermal profile for a region of interest, the heat conduction equation shown in Equation (1) needs to be solved with given boundary conditions [1].

$$k\frac{\partial^2 T(x,y,z)}{\partial x^2}+k\frac{\partial^2 T(x,y,z)}{\partial y^2}+k\frac{\partial^2 T(x,y,z)}{\partial z^2}+q^*=0 \quad (1)$$

where k is the thermal conductivity, ρ is the density, and c_p is the specific heat, q^* is the heat generation per volume, and $T(x, y, z)$ is the temperature of the position (x, y, z).

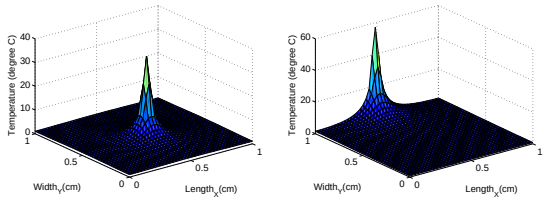
In IC thermal analysis, heat conduction equations have been conventionally solved by grid-based methods, such as Finite Difference Method (FDM) or Finite Element Method (FEM), which involve a huge amount of data and are computationally expensive. In an effort to accelerate computation of temperature distribution, a matrix convolution technique, called "Power Blurring (PB)," has been developed [2].

This PB method has its theoretical basis on the Green's function method and the methodological basis from image blurring used for image processing.

The Green's Function method first finds a solution to the partial differential equation with a point source as the driving function. This solution is called the Green's function, which is equivalent to the impulse response of the system. Subsequently, a solution to an actual source is represented as a superposition of the impulse responses to the point sources at different locations [3]. In image processing, an image can be blurred using a filter mask. The filter mask is a matrix whose coefficients represent a rule about how to modify the image. As the filter mask is moved from one position to another in the image, convolution operation is performed.

For a given IC chip, power map can be obtained by monitoring chip activities. If we think of the power map as an image, the thermal profile of the IC chip corresponding to the power map can be regarded as a blurred image of the power map while the filter mask is treated as the impulse response (i.e. Green's function) of the system. Hence, the new method is named "Power Blurring."

In our case, a spatial impulse response is used as a filter mask and is called "the thermal mask," which can be obtained with full 3D finite element analysis (FEA) using ANSYS [4]. Previously, the PB method required several FEA simulations since the shape of the impulse response depends on the position where the point heat source is applied, which is a shortcoming. For example, a point heat source at the center and that at the edge of the IC surface produce different peak temperatures and different temperature profiles as shown in Figure 1. This is due to the finite size of an IC chip; hence a point heat source experiences different boundary conditions depending on its locations.



(a) (b)

Fig. 1 Temperature profiles on the surface of an IC chip with a point heat source at the (a) center and (b) edge.

The PB method was further improved by applying the Method of Image which takes into account the symmetry of the heat dissipation at the boundary for a finite sized chip [5].

In this paper, the PB method will be reviewed and case studies for various stead-state power maps will be presented. Finally, a method for parameterization of the thermal mask will be proposed and justified.

The remainder of the paper is organized as follows. In Section 2, the PB method and case study results for various steady-state power maps are presented. The thermal mask parameterization and simulation results are presented in Section 3, followed by conclusions in Section 4.

2. Power Blurring Method

2.1 Package Model (Test Structure)

Figure 2 shows our package model for case studies. Material properties were adopted from [2]. The configuration consisted of a Si IC with a surface area of 1cm× 1cm and a Cu heat sink with a heat spreading layer. The Si IC was orthogonally meshed with element size of $0.025\times 0.025\text{cm}^2$ for FEA.

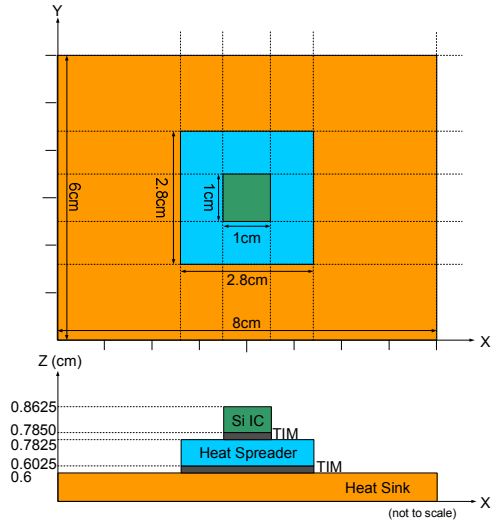


Fig. 2 Packaged IC chip where the heat spreader, the heat sink and the thermal interface material (TIM) are included.

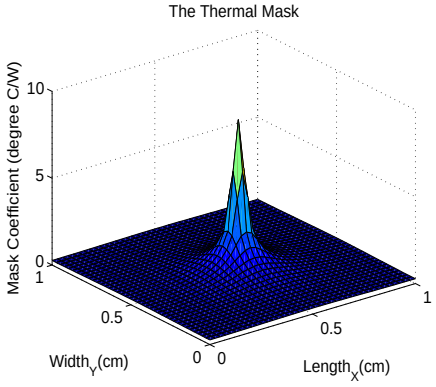
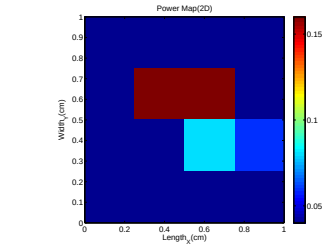


Fig. 3 The thermal mask.

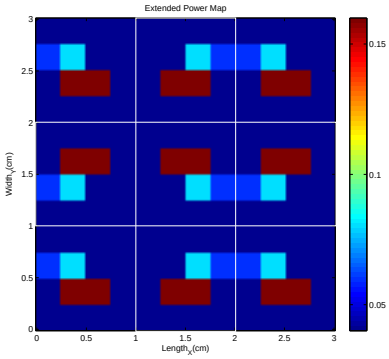
2.2 The Thermal Mask

First, spatial impulse response of the package is obtained by ANSYS simulation using a point heat source as an approximate delta function; 6,250 W/cm^2 heat flux is applied to a single element in the center of the Si IC. Assuming a flip chip package, 0.15 W/cm^2-K is used for convective heat transfer coefficient at the bottom surface of the heat sink, and other minor heat transfer paths are neglected in this analysis. The ambient temperature is set to 35°C. To generate the thermal mask, the resulting surface temperature profile is normalized by the amount of power applied to produce the temperature distribution. Figure 3 shows the thermal mask with unit of °C/W (thermal resistance). The thermal mask generates a temperature profile when it is convoluted with the power map.

2.3 Method of Image and Error Reduction



(a)

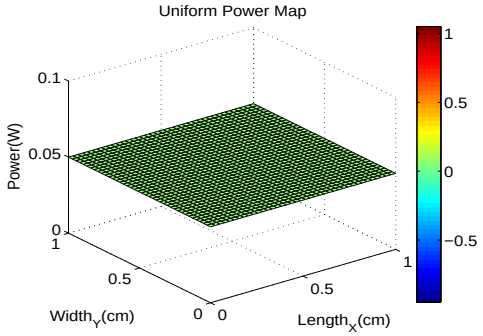


(b)

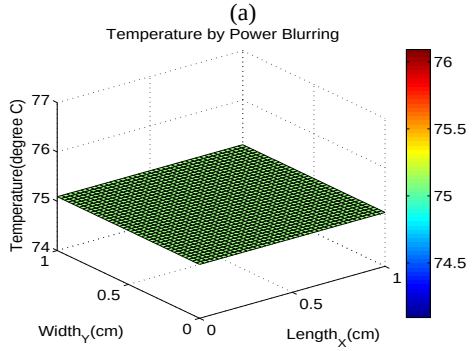
Fig. 4 (a) A coarse power map and (b) corresponding extended power map using the Method of Image.

Boundary conditions on the surfaces of Si IC chip are adiabatic. Thermal problems can be often translated into electrical problems to take advantage of well developed analysis methods. Electromagnetic problems involving a planar perfect electric conductor can be solved through the Method of Image in which the surface is replaced by image sources that are mirror images of the sources with appropriate signs [6, 7]. A similar principle can be applied to the thermal problems involving adiabatic boundary conditions. No heat transfer occurs at the adiabatic boundary. Thus mirror images can replace the adiabatic boundaries as shown in Figure 4.

Introducing the Method of Image into the PB method causes another source of error because of the incomplete symmetry. The heat spreader and the sink are bigger than the Si IC chip and there is three-dimensional heat spreading. For uniform power distribution such as one shown in Figure 5 (a), the PB method predicts the temperature profile in Figure 5 (b), whereas ANSYS generates a different temperature profile in Figure 5 (c). Thus, the temperature deviation between the real temperature and one by the PB method is intrinsic to PB method with the Method of Image applied and shown in Figure 6.



(a)



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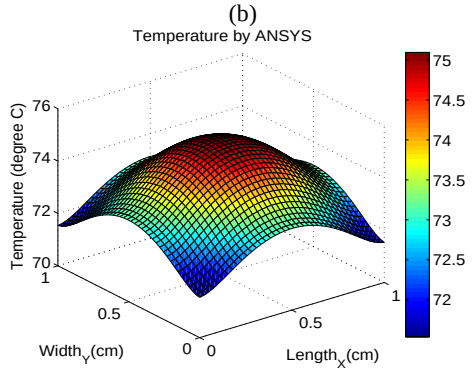


(c)

Fig. 5 (a) Uniform power map and corresponding thermal profiles by (b) the PB method and (c) ANSYS

Temperature rise is linearly proportional to the input power. Thus the intrinsic error in Figure 6 is linearly dependent on the input power level. On the other hand, the relative deviation given in Equation (2) below is constant regardless of input power level because both temperatures (T_{PB} & T_{real}) are linearly dependent on input power. Thus, Equation (2) can be used for error compensation.

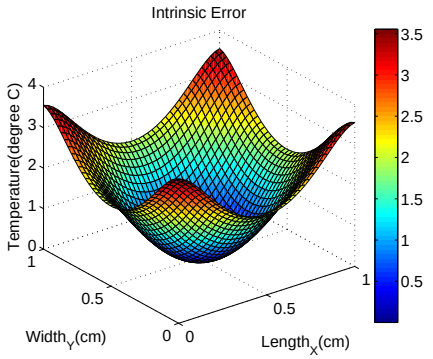
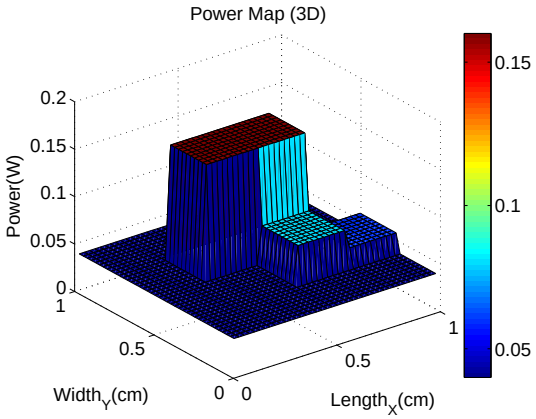


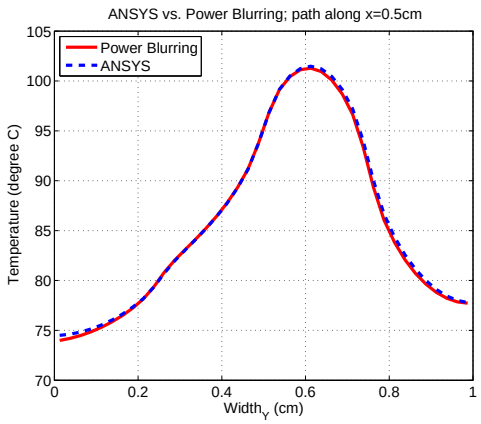
Fig. 6 Intrinsic error in the PB method

$$E_r=(T_{PB}-T_{real})/T_{real} \quad (2)$$

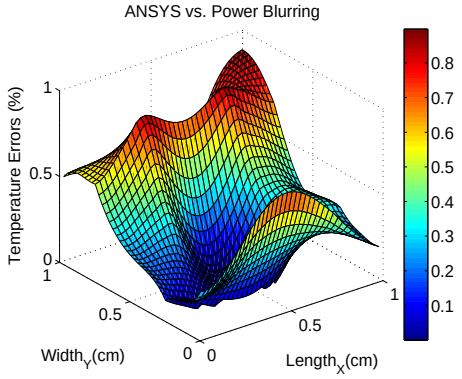
2.4 Case Studies



(a) A coarse power map



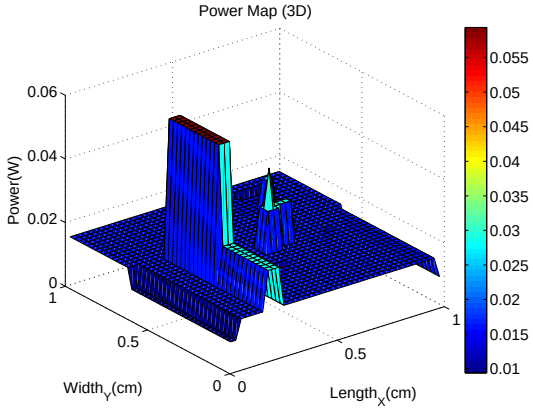
(b) path along x=0.5cm



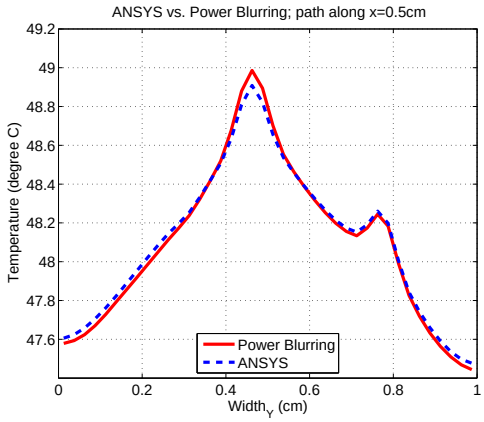
(c)

Fig. 7 (a) A coarse power map for an IC chip, (b) corresponding temperature profile, and (c) relative temperature error between ANSYS and Power Blurring.

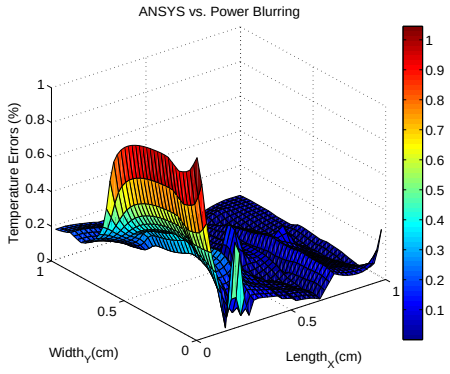
A coarse power map and the corresponding temperature profiles along the specified paths are given in Figure 7 (a) and (b), respectively. As can be seen in Figure 7 (c), the maximum temperature error is less than 1% in this case.



(a) A fine power map



(b) path along x=0.5cm



(c)

Fig. 8 (a) A typical fine power map for an IC chip, (b) corresponding temperature profile, and (c) relative temperature error between ANSYS and Power Blurring.

A typical fine power map and the corresponding temperature profile along the specified path are given in Figure 8 (a) and (b), respectively. As can be seen in Figure 8 (c), the maximum temperature error is less than 1% in this case.

3. Thermal Mask Parameterization

In the PB Method, the thermal mask needs to be obtained first. Thus this method is dependent on FEA by ANSYS (or it could be measured experimentally). The thermal mask needs to be recalculated when some parameters are changed. To avoid this inconvenience, the thermal mask is parameterized for several parameters such as thermal conductivity of the substrate, convection coefficient, and chip thickness. The thermal mask is almost symmetrical about the center. Hence the thermal mask can be represented as one dimensional analytical function by curve fitting. The function is in the form of $y = m1 + m2 \times \exp(m3 \times x)$, where m1, m2, and m3 are fitting parameters.

3.1 Thermal Conductivity Variation

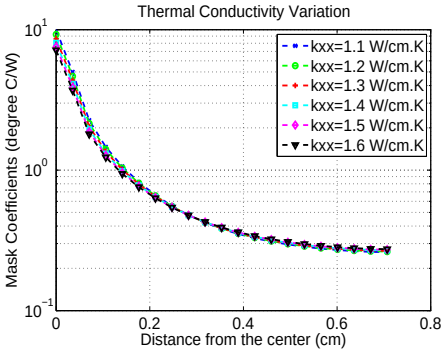


Fig. 9 Thermal Mask coefficients with different substrate thermal conductivities.

Consecutive simulations were performed with different thermal conductivity values ranging from 1.1 W/cm-K to 1.6W/cm-K with 0.1W/cm-K step, and results are shown in Figure 9. With higher thermal conductivity, overall temperature of the Si IC chip is lower because heat can be removed by heat sink more easily. Thus the thermal mask has lower values when the thermal conductivity value is higher.

Table 1 Curve fitting parameters.

Thermal Conductivity (W/cm-K)	m1	m2	m3
1.1	0.36332	9.6293	-20.963
1.2	0.36442	8.8657	-20.717
1.3	0.3654	8.2168	-20.49
1.4	0.36629	7.6584	-20.279
1.5	0.3671	7.1725	-20.084
1.6	0.36786	6.7458	-19.902

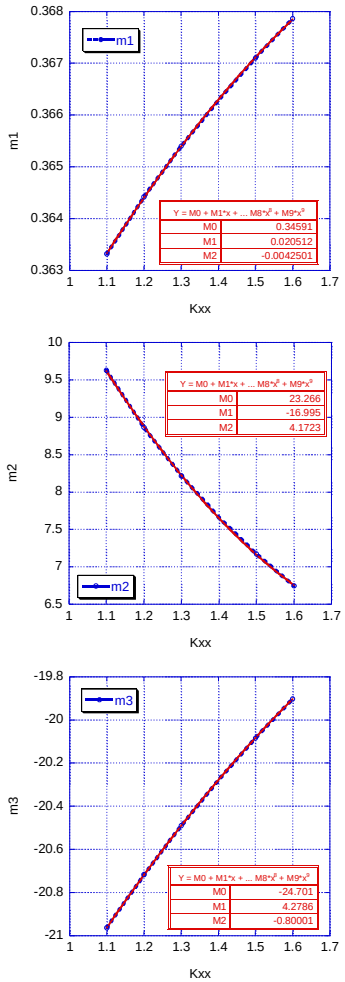


Fig. 10 Three curve fitting parameters (m1, m2, and m3) represented as a function of thermal conductivity.

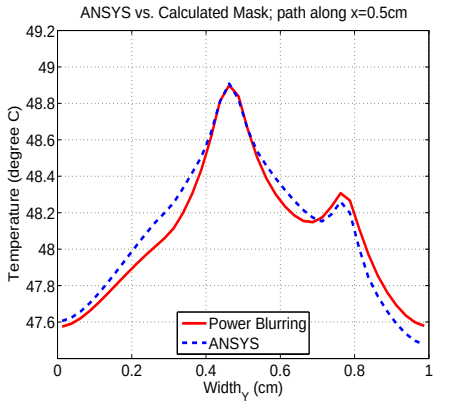
Table 1 summarizes curve fitting parameter values for different thermal conductivities. When curve fitting parameters (m1, m2, and m3) are plotted with respect to thermal conductivity (kxx), we can notice that those parameters can be represented as a function of thermal conductivity as shown in Figure 10. Analytical expressions for curve fitting parameters (m1, m2, and m3) are given by Equations (3) – (5).

$$m1 = 0.34591 + 0.020512 \times Kxx - 0.0042501 \times Kxx^2 \quad (3)$$

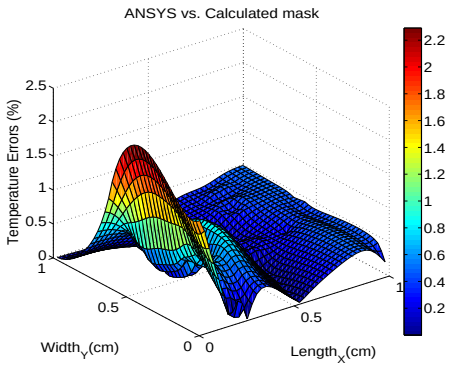
$$m2 = 23.266 - 16.995 \times Kxx + 4.1723 \times Kxx^2 \quad (4)$$

$$m3 = -24.701 + 4.2786 \times Kxx - 0.80001 \times Kxx^2 \quad (5)$$

When thermal conductivity is 1.25w/cm-K, m1=0.3649, m2=8.5415, and m3=-20.6028, respectively. Figure 11 shows comparisons between temperature profiles by ANSYS and the PB method using the parameterized mask. As can be seen, parameterized mask shows a good performance resulting in a maximum error of 1.1 °C (2.29%).



(a)



(b)

Fig. 11 Comparisons between ANSYS and the PB method using the parameterized mask: (a) thermal profile along x=0.5cm and (b) relative errors.

3.2 Convective Heat transfer Coefficient Variation

To investigate the effect of convection coefficient variation on the mask, multiple simulations were performed with different convection coefficient values ranging from 0.1 W/cm^2-K to 1W/cm^2-K with 0.1W/cm^2-K step. Figure 12 shows mask values obtained through 10 simulation runs. Convection occurs only at the bottom surface of the heat sink. Thus the convection coefficient has effect on lowering the temperature offset (i.e. the tail of the thermal mask).

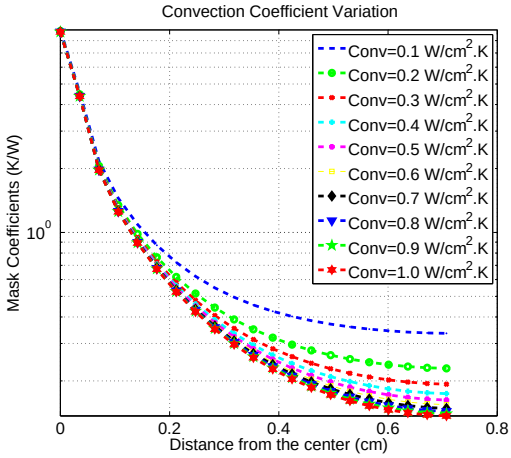


Fig. 12 Thermal mask coefficients with different convection coefficients.

Table 2 Curve fitting parameters.

Convection Coefficient (W/cm^2-K)	m1	m2	m3
0.1	0.43509	8.5293	-20.59
0.2	0.32923	8.5293	-20.591
0.3	0.293	8.5292	-20.591
0.4	0.27425	8.5292	-20.592
0.5	0.26257	8.5291	-20.592
0.6	0.25446	8.5291	-20.592
0.7	0.24845	8.529	-20.592
0.8	0.24374	8.529	-20.593
0.9	0.23994	8.529	-20.593
1.0	0.23678	8.529	-20.593

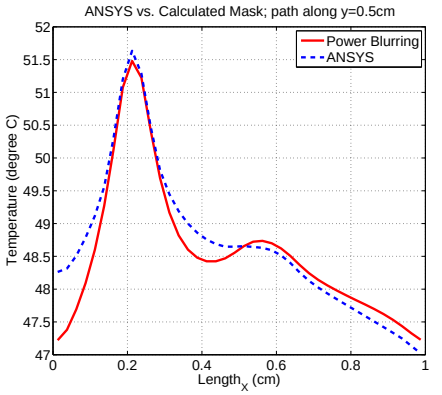
Mask parameterization for convection coefficient variation can be done in a similar way as the thermal conductivity case. Fitting parameters are summarized in Table 2. Fitting parameter m1 can be represented as a function of convection coefficient (h_f). Analytical expressions for curve fitting parameters (m1, m2, and m3) are given by Equations (6) – (8).

$$m1 = 0.75623 - 5.1822 \times h_f + 26.09 \times {h_f}^2 - 75.65 \times {h_f}^3 + 130.67 \times {h_f}^4 - 132.62 \times {h_f}^5 + 72.907 \times {h_f}^6 - 16.734 \times {h_f}^7 \quad (6)$$

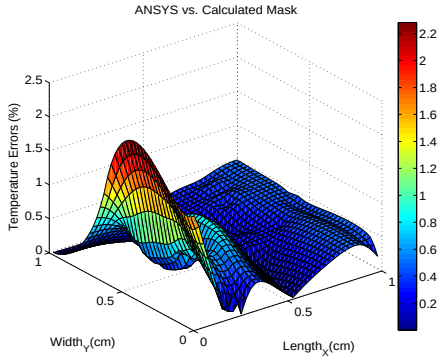
$$m2 = 8.529 \quad (7)$$

$$m3 = -20.59 \quad (8)$$

When convection coefficient is 0.15 (w/cm^2-K), the thermal mask can be approximated as $y = 0.3675 + 8.529 \times \exp(-20.59 \times x)$. Figure 13 shows comparisons between temperature profiles by ANSYS and the PB method using the parameterized mask. As can be seen, the parameterized mask shows a good performance resulting in a maximum error of 1.1 °C (2.29%).



(a)



(b)

Fig. 13 Comparisons between ANSYS and the PB method using the parameterized mask: (a) thermal profile along y=0.5cm and (b) relative errors.

3.3 Chip Thickness Variation

To investigate the effect of chip thickness variation on the mask, multiple simulations were performed with different chip thickness ranging from 100um to 1000um. Figure 14 shows thermal mask coefficients obtained through 10 simulation runs.

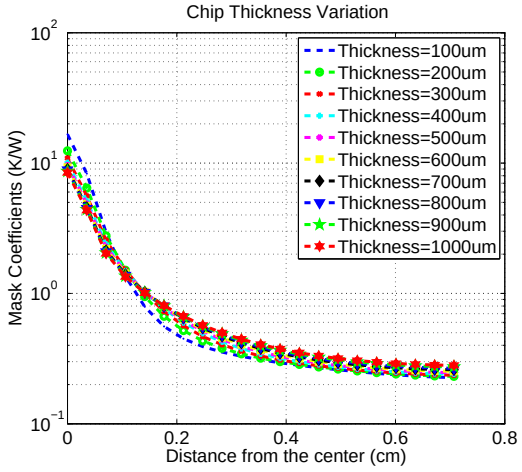


Fig. 14 Thermal mask coefficients with different chip thicknesses.

Table 3 Curve fitting parameters.

Chip Thickness (um)	m1	m2	m3
100	0.24595	16.533	-22.96
200	0.28046	12.206	-20.851
300	0.30494	10.624	-20.419
400	0.32245	9.7437	-20.298
500	0.33718	9.3009	-20.459
600	0.34805	8.9033	-20.45
700	0.35717	8.5896	-20.408
800	0.36672	8.4702	-20.574
900	0.37412	8.2531	-20.49
1000	0.38104	8.0596	-20.381

Mask parameterization for chip thickness variation can be done in a similar way as the previous two cases. Fitting parameters are summarized in Table 3. Fitting parameter (m1, m2, and m3) can be represented as a function of chip thickness (T). Analytical expressions for curve fitting parameters (m1, m2, and m3) are given by Equations (9) – (11).

$$m1 = 0.20704 + 0.00044445 \times T - 4.6249e-7 \times T^2 + 1.9298e-10 \times T^3 \quad (9)$$

$$m2 = 25.427 - 0.12274 \times T - 0.00039573 \times T^2 - 6.4986e-7 \times T^3 + 5.2274e-10 \times T^4 - 1.6326e-13 \times T^5 \quad (10)$$

$$m3 = -28.474 + 0.080248 \times T - 0.00029566 \times T^2 + 4.6816e-7 \times T^3 - 1.6034e-10 \times T^4 - 4.2783e-13 \times T^5 + 5.1682e-16 \times T^6 - 1.7331e-19 \times T^7 \quad (11)$$

When chip thickness is 775um, m1=0.3636, m2=8.4233, and m3=-20.518, respectively. Thus the thermal mask can be approximated as

$y = 0.3636 + 8.4233 \times \exp(-20.518 \times x)$. Figure 15 shows comparisons between temperature profiles by ANSYS and the PB method using the parameterized mask. As can be seen, the parameterized mask yields a maximum error of 1.1 °C (2.29%).

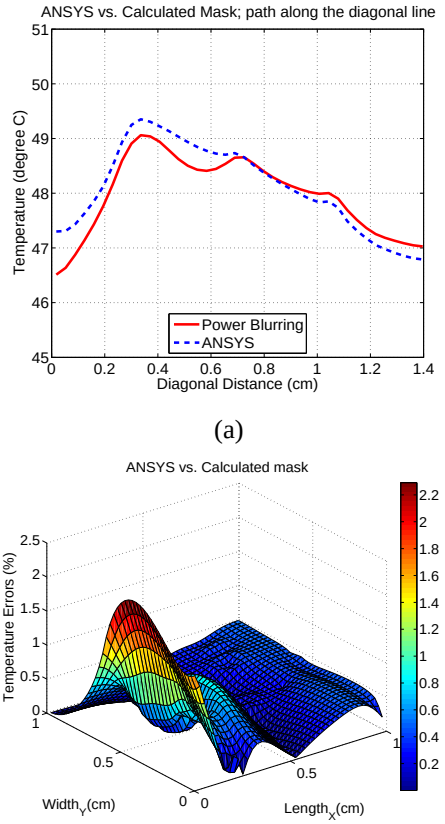


Fig. 15 Comparisons between ANSYS and the PB method using the parameterized mask: (a) thermal profile along diagonal path and (b) relative errors.

4. Conclusion

In this paper, an accelerated temperature calculation method called "Power Blurring" and the error reduction method were discussed. Throughout various case studies, the PB method shows very reliable results with maximum error less than 1% for steady-state power maps. To mitigate the dependence on ANSYS for the thermal mask generation, a method of mask parameterization was proposed and used. The PB method using parameterized masks performs well with maximum error around or less than 2.3%. Our method reduced the calculation time by a factor of 170 compared to ANSYS simulation.

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