Fast Computation of Temperature Profiles of VLSI ICs with High Spatial Resolution

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Abstract

The reality of high temperature non-uniformity has become a serious concern in the CMOS VLSI industry limiting both the performance and the reliability of packaged chips. Thus the surface temperature profile of VLSI ICs has become critical information in chip design flow. For fast computation of surface temperature profile, Power Blurring (PB) method has been developed. This method can be applied to simulations with high spatial resolution, which have been prohibitively expensive with conventional methods. Comparative case studies with different levels of resolution illustrate that not only localized small hot spots can be overlooked but even the average chip temperature can be underestimated, and hence the necessity of thermal simulation with high spatial resolution. Using our PB method, we obtained transistor level thermal map ($5\times5\mu m^2$ grid) of a $5\times5mm^2$ chip with a computation time of 20 seconds.

Keywords

Thermal simulation, Power Blurring, Power dissipation profile (power map), Temperature distribution (thermal profile), Finite element method (FEM), Finite difference method (FDM)

1. Introduction

The ongoing scaling down of CMOS technology has made thermal related issues in VLSI ICs increasingly more exasperated in recent years. These issues, especially the strongly localized temperature non-uniformity (hot spot), significantly limit the performance and reliability of VLSI ICs. In addition, the increasing leakage power and its exponential dependence on the temperature require much attention to thermal-aware simulations and optimization. Although state-of-the-art thermal measurement techniques (e.g. thermo-reflectance imaging [1, 2]) are very useful in obtaining the IC surface temperature profile, a thermal-aware simulator that can predict the IC temperature profile without resorting to actual measurements is very much needed in physical chip design process such as routing and placement.

Effective methods for the computation of temperature profiles from the power dissipation profiles are important tools for chip designers and reliability engineers to identify hot spots or meet thermal requirements prior to actual chip fabrication. Typically, the computation of an IC's temperature profile from its power dissipation profile is performed by grid-based solvers using finite element method (FEM) or finite difference method (FDM). This approach works fairly accurately but it requires sophisticated meshing of the grid structure and prohibitive calculation time for high resolution simulation. High spatial resolution simulation is essential for the identification of hot spots less than 100 microns in diameter. Furthermore, coarse grid power map can underestimate the average chip temperature and hot spot temperature.

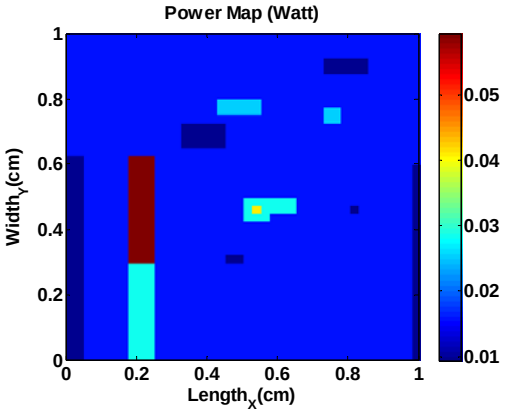
In an effort to accelerate the computation of IC chip temperature profile with high accuracy, we have developed a matrix convolution based technique, called "Power Blurring (PB)". In the perspective of PB technique, the temperature profile of an IC chip is essentially a superposition of the resulting temperature fields of each individual point heat source. As we can find the point-spread-function (or the thermal mask) for heat dissipation, equivalent to the Green's Function (i.e. impulse response of the system), the temperature profile can be obtained from its underlying power dissipation profile by using a spatial convolution process [3, 4, 5].

In this paper, we further improve our PB method to predict IC chip temperature with high spatial resolution, which is prohibitive for finite element solvers to accomplish. We will also illustrate the necessity of high resolution prediction through comparison of temperature profiles obtained by different levels of resolution. The remainder of this paper is organized as follows. In Section 2, the PB method will be briefly reviewed. Comparative study on grid size dependence of the temperature profile will be discussed in Section 3. In Section 4, detailed discussion on the application of PB method to high spatial resolution will be presented, followed by conclusions in Section 5.

2. Fast Computation Technique to Calculate Temperature (Power Blurring Method)

Figure 1 shows a comparison between the temperature profiles calculated by finite element solver (ANSYS [6]) and the temperature profile calculated by the PB method for a given test structure shown in Figure 2. In this example, The Si IC was orthogonally meshed with moderate element size of $250\times250\mu m^2$. As can be seen, PB method produces accurate thermal profile with significant saving of computation time. In this particular case, computation time was reduced by a factor of 293. The main strength of PB technique is that it exploits the dominant heat spreading in the silicon substrate and it uses the superposition principle. With two finite element simulations, the temperature point spread function for a sophisticated package can be calculated. This method is

similar to the Green's function technique that has been recently applied to IC thermal analysis [7, 8]. Instead of using analytical expressions of the Green's function that could be found only for simple planar geometries and that require an infinite series, an impulse function of the package is calculated using a numerical technique and then it is applied to an arbitrary heat dissipation profile. In realistic packages, 3-D heat spreading plays an important role because heat spreader and the heat sink are typically larger than the chip. This can be easily modeled using the power blurring technique, whereas no direct analytical solution for the whole packaged chip has been found yet [9].



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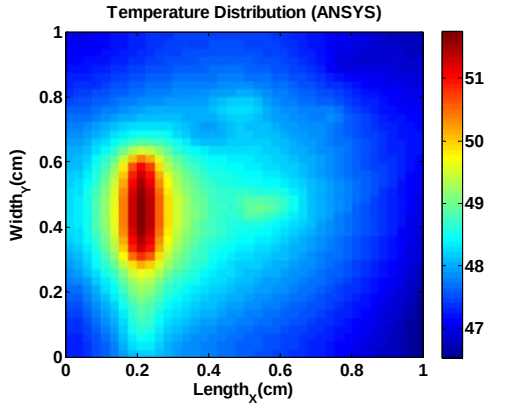

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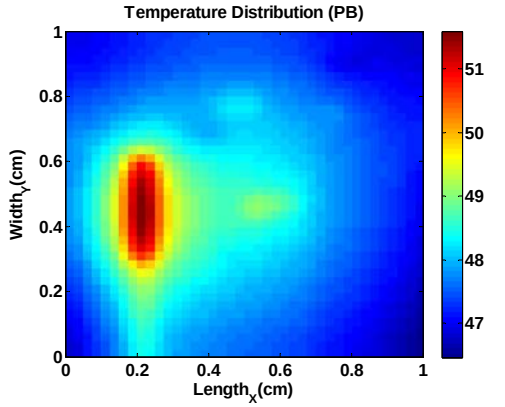

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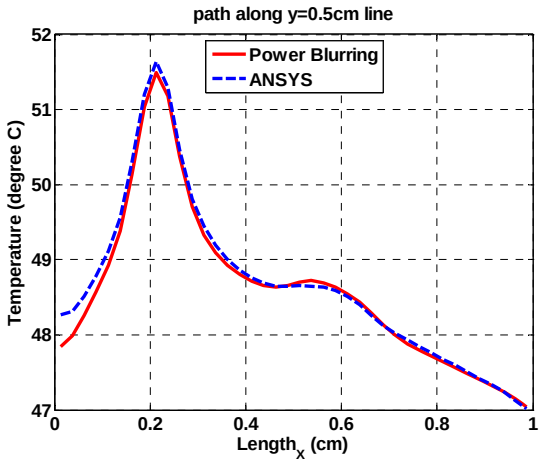

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Figure 1: (a) a typical power dissipation pattern in VLSI ICs, (b) estimated temperature profile by ANSYS (14.63 sec), (c) estimated temperature profile by PB method (0.05 sec) (d) cross-section comparison.

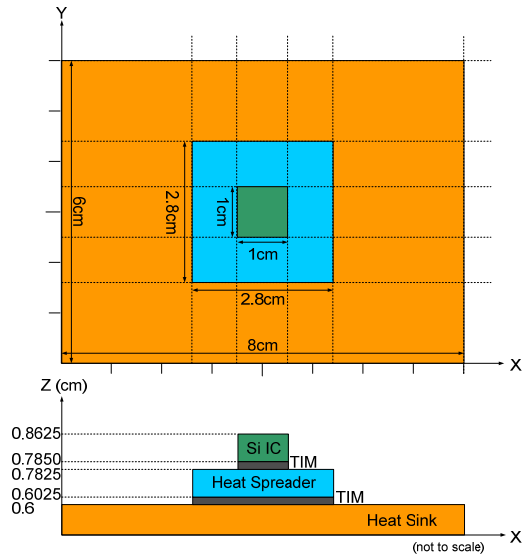


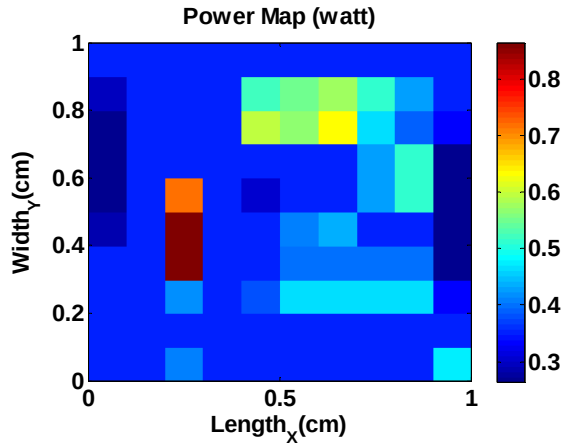
Figure 2: Packaged IC chip where the heat spreader, the heat sink and the thermal interface material (TIM) are included (parameters are given in [4]).

3. Comparative Study on Grid Size Dependence of the Temperature Profile

Our PB method was applied to thermal simulations with different levels of resolution. Each temperature profile was compared with corresponding FEA result for justification.

3.1. Coarse meshing

Figure 3 represents coarse meshing scheme. The Si IC was orthogonally meshed with element size of $1000 \times 1000 \mu m^2$. In this case study, PB method produces temperature profile with maximum error less than 0.4%, reducing the computation time by a factor of 176 compared to ANSYS simulation (ANSYS took 3.52 sec whereas PB took 0.02 sec).



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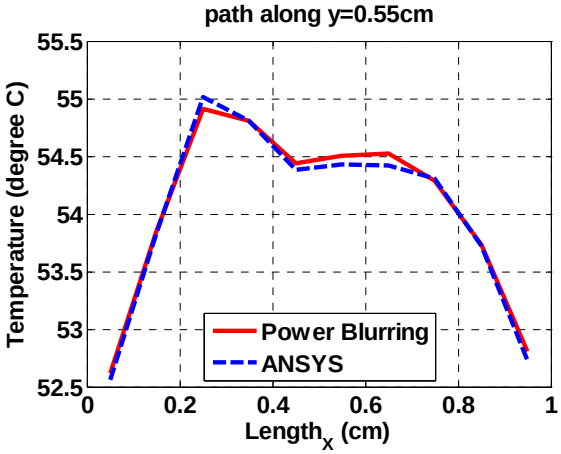

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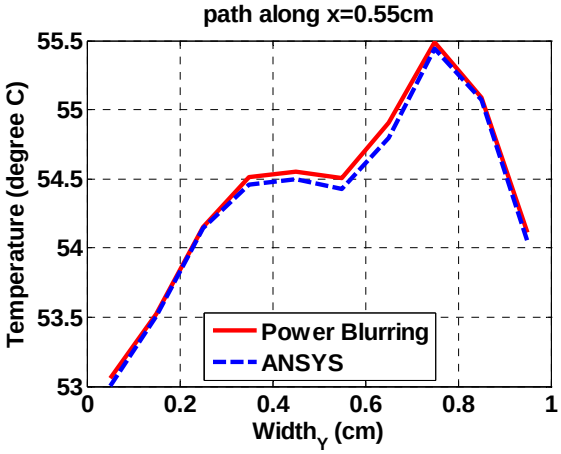
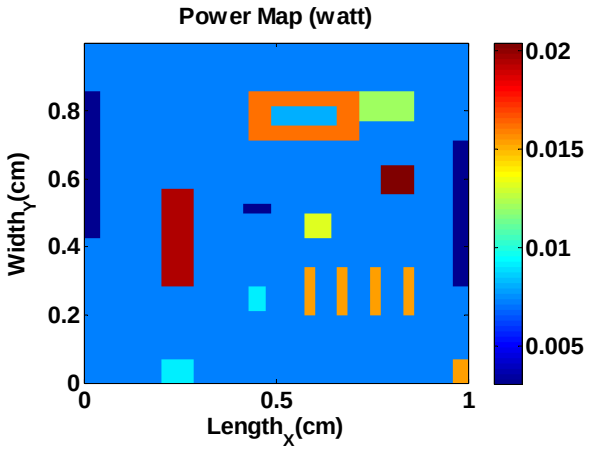


(c)

Figure 3: (a) coarse power map with 1000µm resolution, (b) and (c) temperature profile along the specified path.

3.2. Fine meshing

Figure 4 represents fine meshing scheme. The Si IC was orthogonally meshed with element size of $143 \times 143 \mu m^2$. In this case study, PB method produces temperature profile with maximum error less than 1%, reducing the computation time by a factor of 202 compared to ANSYS simulation (ANSYS took 72.83 sec whereas PB took 0.36 sec).



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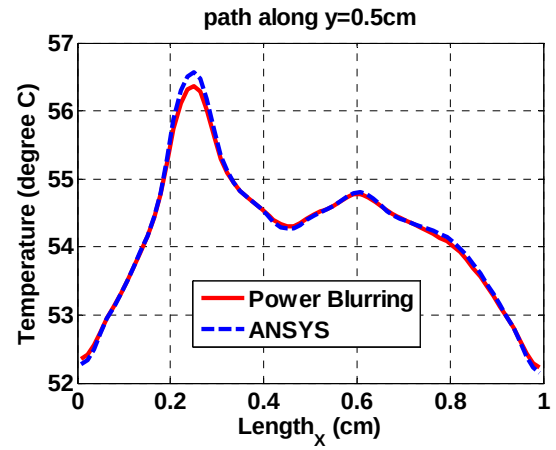

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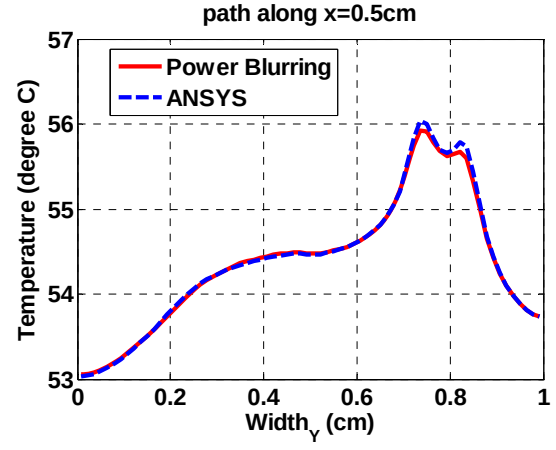

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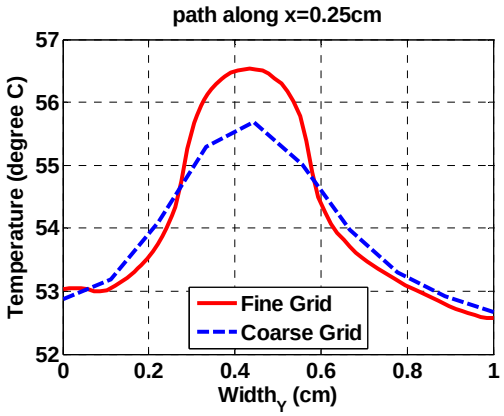
Figure 4: (a) fine power map with 143 µm resolution, (b) and (c) temperature profile along the specified path.

3.3. Comparison between coarse and fine meshing schemes

To investigate the dependence of thermal profile on the resolution, coarse meshing results and fine meshing results are compared in this section (coarse power map was derived from fine power map).

In Figure 5, temperature profiles obtained with fine grid scheme are compared to those obtained with coarse grid

scheme along the specified paths. As can be seen, thermal profiles with low resolution can underestimate hot spot temperatures.



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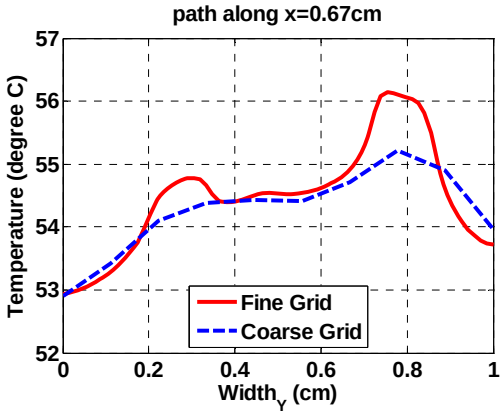

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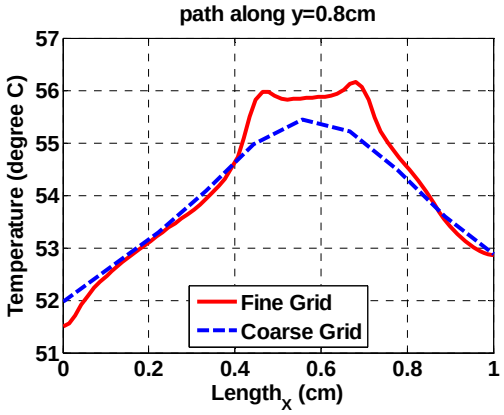

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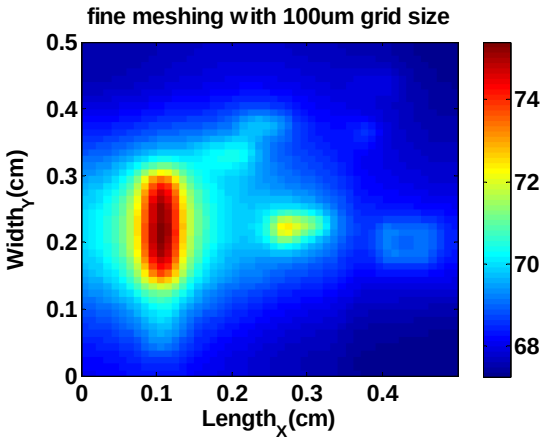
Figure 5: Temperature profile comparison between coarse meshing scheme and fine meshing scheme.

4. Very Fine Meshing with Transistor Level Resolution

For better accuracy, it is required to use finer mesh grid. However, we cannot increase resolution indefinitely due to limited computation resources. To generate a temperature profile from a very fine power map, the conventional numerical analysis methods are ineffective. However, the PB method only requires a thermal mask which can have a user-specified resolution using curve fitting based on the circular symmetry of the thermal mask [5]. Thus it can be applied to any level of resolution.

The PB method is implemented with a matrix convolution process, which is much faster than the conventional numerical analysis methods such as FEM or FDM. However, performing convolution with large-sized matrices is also a time-consuming task. The matrix convolution process can be simplified as a matrix multiplication using the Fourier transform. To deal with large-sized matrix, we employ FFT algorithm in MATLAB [10]. In the acquisition of transistor level thermal map with $5\times5\mu m^2$ grid for a $5\times5mm^2$ chip in Figure 6 (b), the PB method took only 20 seconds.

Figure 6 shows a comparison between temperature profiles calculated by this advanced PB method with fine meshing and very fine meshing. We find that the very fine meshing performs much more accurate in terms of showing the micro-scale hot-spots corresponding to each individual device. We also find a discrepancy on the average chip temperature between the fine meshing and the very fine meshing results. A very fine meshing (comparable to the individual device size) is necessary for thermal analysis for VLSI ICs in terms of accuracy. The advanced PB method can accurately and efficiently calculate the thermal profiles of packaged high density power VLSI ICs.



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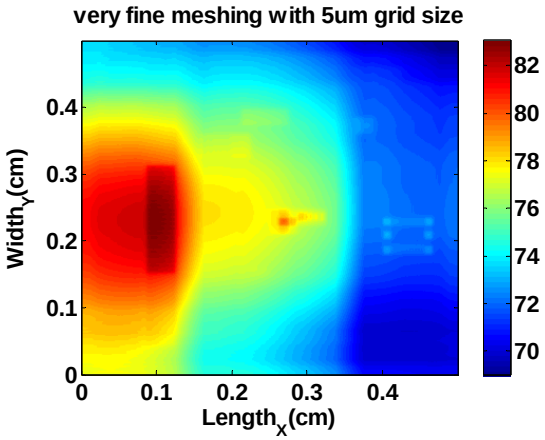

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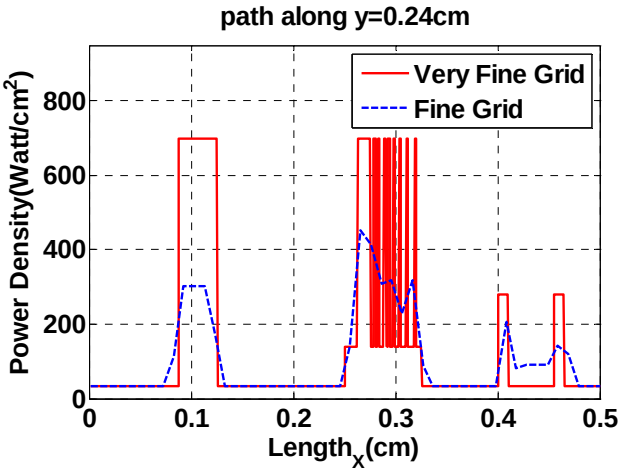

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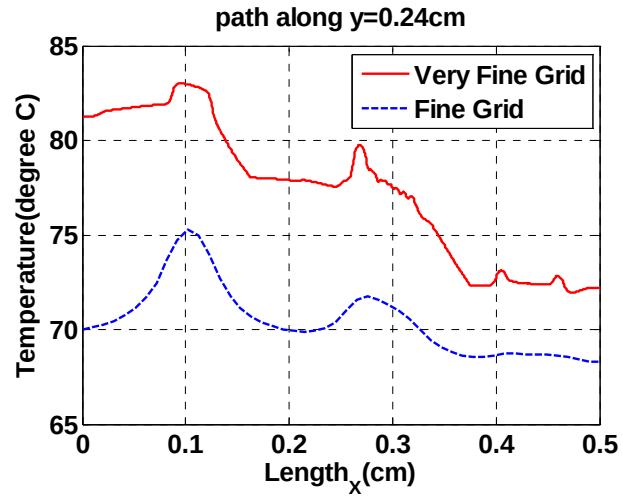

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Figure 6: A comparison between temperature profiles calculated by advanced PB technique with fine meshing and very fine meshing schemes; (a) calculated temperature profile based on a fine meshed (50 × 50, 100μm/grid) power dissipation profile (b) calculated temperature profile based on a very fine meshed (1000×1000, 5μm/grid) power dissipation profile (c) power density profile along chip cross-section (d) temperature profile along chip cross-section.

5. Conclusions

In this paper, a fast computation method called "Power Blurring" was applied to predict IC chip temperature with high spatial resolution. It has been difficult to accomplish this task with the conventional numerical analysis methods. By using various case studies, we have shown that high spatial resolution thermal simulation with high computational efficiency such as our advanced PB method is necessary to predict hot spot temperatures of large chips for high accuracy.

Acknowledgments

This research has been supported in part by the grants from the UC Santa Cruz (UCSC), UC MICRO/Intel, and National Science Foundation (NSF) CSR SMA Program.

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