Integrated Cooling for Si-based Microelectronics

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Abstract

Thin film thermoelectric coolers are advantageous for their high cooling power density and their potential integrated applications. $Si_{1-x}Ge_x$ is a good thermoelectric material at high temperatures and superlattice structures can further enhance the device performance. $Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x$/Si superlattice structures were grown on Si substrates using molecule beam epitaxy. $Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x$/Si superlattice thin film micro-coolers with the film thickness on the order of several microns were fabricated using integrated circuit processing technology. Micro thermocouples and integrated thermistor sensors were used to characterize these coolers. Maximum cooling power density on the order of hundreds of watts per square centimeter was measured at room temperature. It is possible to monolithically integrate these coolers with Si-based microelectronic devices for localized cooling and temperature stabilization.

Introduction

Overheating is one of the main threats to the lifetime and reliability of optoelectronic and microelectronic devices. In addition to passive methods such as natural convection or forced air cooling, thermoelectric (TE) devices are widely used to cool optoelectronic devices as an active cooling method. But their application to high power microelectronic devices is limited. This is because of the relatively low efficiency and low cooling power density of conventional TE coolers. Conventional TE coolers are based on Bi_2Te_3 compounds and they have dimensions on the order of millimeters to centimeters. Their maximum cooling power density is below 20 W/cm^2 and the efficiency is about 1/5 of that of compressor-based refrigerators. Another limitation for application to microelectronic devices is the packing issues. Sometimes the cooler is much lager than the microelectronic chips. The additional packaging for TE coolers can add additional reliability issues.

Integrated thin film thermoelectric cooling is an attractive way to solve these problems. First, the cooling power density is inversely proportional to the thickness of the TE element of the cooler. High cooling power density is one of the main advantages of thin film refrigerators. Integrated cooling can also solve packaging issues. Additionally, integrated cooler can be cost effective and compact. By fabricated micro coolers in selective areas of the chip it is possible to remove hot spots instead of cooling the whole chip, thus improving the overall cooling efficiency. Development of hot spots is one of the main problems that fail a microprocessor chip. If we can selectively cool the hot spots, the total energy consumed in the coolers will be relatively small while the chip reliability can still be improved. For monolithic integration with silicon-based microelectronics, thermoelectric materials that can be processed with integrated circuit (IC) technology are required and the materials that can be grown on silicon are preferred. The processing of conventional TE cooler materials such as Bi_2Te_3 is a bulk technology and incompatible with standard IC processing. $Si_{1-x}Ge_x$ is a good thermoelectric material for high temperature applications; it has been used for thermo-nuclear power generation in spacecrafts [1~3]. At room temperature, the figure of merit ZT of bulk $Si_{1-x}Ge_x$ is around 0.1 (for x=0.3) [3], which can give a maximum cooling of over 10 K. Although this cooling is much less than that of Bi_2Te_3 coolers, SiGe coolers can be monolithically integrated with Si-based microelectronic devices and have many potential applications. Recently, superlattice structures have been proposed to increase the thermoelectric figure of merit ZT beyond that of alloy materials by various mechanisms, such as quantum confinement, thermionic emission, carrier pocket engineering and phonon engineering [4~7]. ZT up to 0.96 and 1.25 was predicted on (111) oriented strain-symmetrized and strain-nonsymmetrized Si/Ge superlattices at 300K, respectively, through carrier pocket engineering [6]. $Si_{1-x}Ge_x$/Si superlattice microcoolers have been demonstrated on both n-type and p-type (001) oriented samples with a maximum cooling of 4.2K at room temperature [8~10]. In this paper, we report the fabrication and characterization of both $Si_{1-x}Ge_x$ alloy and $Si_{1-x}Ge_x$/Si superlattice microcoolers for integrated cooling.

Experiment

There are two maim methods to make integrated thin film coolers on silicon. One is to use in-plane current and heat transport, and the other is to use cross-plane transport. The in-plane cooler device structure is described in reference [11~13]. For this kind of devices, the thin film TE material is deposited on SiO_2 or SiN_x membranes and the substrate such as silicon is removed beneath the cooler in order to reduce the heat conduction between the cooler's cold and hot sides. The cooling power is small due to the small cross section area of the TE film. In this paper, we use cross-plane electrical and thermal transport. Figure 1 shows the schematic diagram of a single element device structure. For the cooling of p-type material, the current goes from the top metal contact, through the $Si_{1-x}Ge_x$ or $Si_{1-x}Ge_x$/Si superlattice, to the bottom contact;

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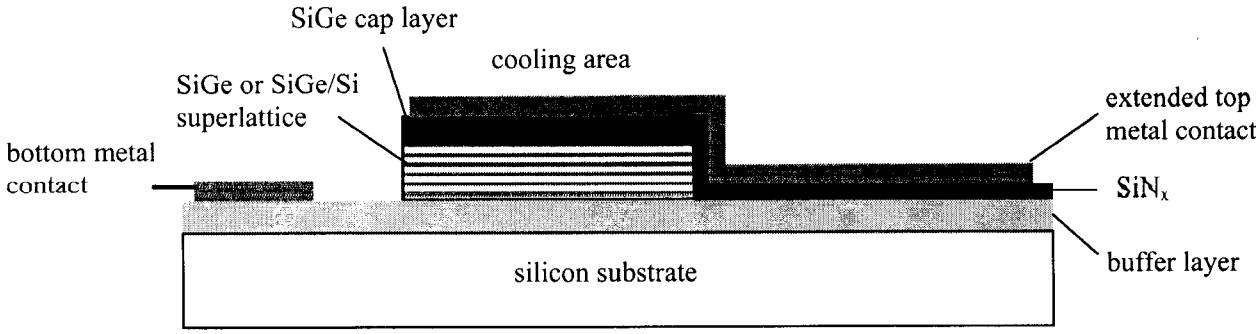

Figure 1. Schematic diagram of a single element SiGe/Si microcooler structure

for the cooling for n-type material, the current direction reverses. Since the device size (cooling area) is much larger than the thickness of the thin $Si_{1-x}Ge_x$ or $Si_{1-x}Ge_x$/Si superlattice layer, the electrical current and heat flow along the cross-plane direction. Thin film coolers using cross-plane transport can have large cooling power density, but they also require low contact resistance and very good heat sink due to the low electrical and thermal resistance of the thin film in the cross-plane direction [14]. Figure 2 shows the cooling vs. specific contact resistivity for various film thicknesses. It can be seen that the cooling is very sensitive to the contact resistance and the specific contact resistivity of low 10^{-7} Ω-cm^2 is required for thin film coolers in the order of several micron thick.

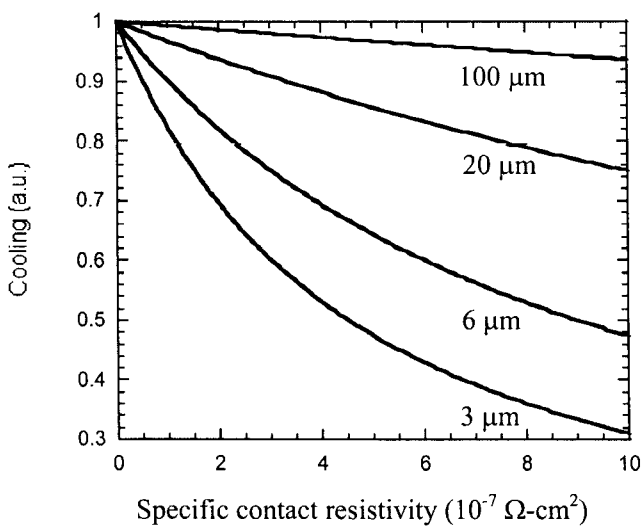

Figure 2. Cooling vs. specific contact resistivity for various TE film thicknesses: 100 μm, 20 μm, 6 μm and 3 μm. (assuming the TE film electrical resistivity 0.003 Ω-cm and ideal heat sink)

P-type $Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x$/Si superlattices were used here as the thermoelectric material for the thin film microcoolers. They were grown on (001) oriented boron doped silicon substrates with molecular beam epitaxy (MBE) [10]. The film thickness is about 3 μm and the boron doping level is 5~7 cm^{-3}. Since $Si_{1-x}Ge_x$ has a larger lattice constant than that of the silicon substrate, buffer layers are needed [8~10]. Finally, a 0.3μm SiGe cap layer doped to 2×10^{20} cm^{-3} was used to reduce the electrical contact resistance of the cooler.

Thousands of SiGe/Si microcoolers were fabricated with standard silicon IC processing technology on each wafer at the same time. The cooling areas of each cooler ranged from 30 × 30 μm^2 to 150 × 150 μm^2, which were defined by the mesa etch down to the buffer layer. Ti/Al metallization was made on top of the mesa and on the SiGe buffer layer next to the mesa for top and bottom contacts respectively. To facilitate sending current to the cooler and device testing, Ti/Au was deposited for the extended top metal contact after a SiN_x passivation step, as shown in figure1. Microcoolers were fabricated with the same processing on three different samples: a. 3 μm SiGe/Si superlattice: 200 periods (12 nm $Si_{0.75}Ge_{0.25}$/ 3 nm Si), b. 3 μm $Si_{0.8}Ge_{0.2}$ alloy, and c. p+ silicon substrate for comparison.

Results

The microcoolers were tested on a temperature-controlled heat sink. Current was sent to the cooler through the top and bottom metal contact, and the cooling temperature was measured by two micro thermocouples with on the top of the cooler and one the heat sink for reference. The cooling temperature is relative to the device temperature at zero current. Figure 3 shows the test results for the $Si_{0.75}Ge_{0.25}$/Si superlattice sample and the p+ silicon substrate sample on 60 × 60 μm^2 devices at a heat sink temperature of 25 °C. Cooling by as much as 4.2 K was measured on $Si_{0.75}Ge_{0.25}$/Si superlattice coolers. This is over four-fold improvement comparing to the bare silicon coolers.

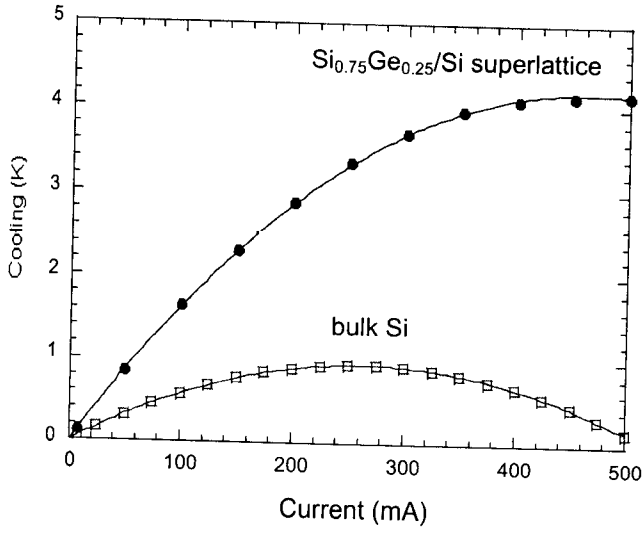

Figure 3. Measured cooling on $Si_{0.75}Ge_{0.25}$/Si superlattice and bulk Si 60 × 60 μm² devices at 25 °C heat sink temperature.

The cooling vs. electrical current test result on the $Si_{0.8}Ge_{0.2}$ thin film microcooler is shown in figure 4 for the device size of 50 × 50 μm². Up to 4.3 K and 13.8 K was measured at heat sink temperature of 25 °C and 250 °C respectively. This cooling increase with heat sink temperature matches the TE properties of bulk $Si_{1-x}Ge_x$ and the temperature dependence of $Si_{1-x}Ge_x$/Si superlattice microcoolers. [3, 8~10]

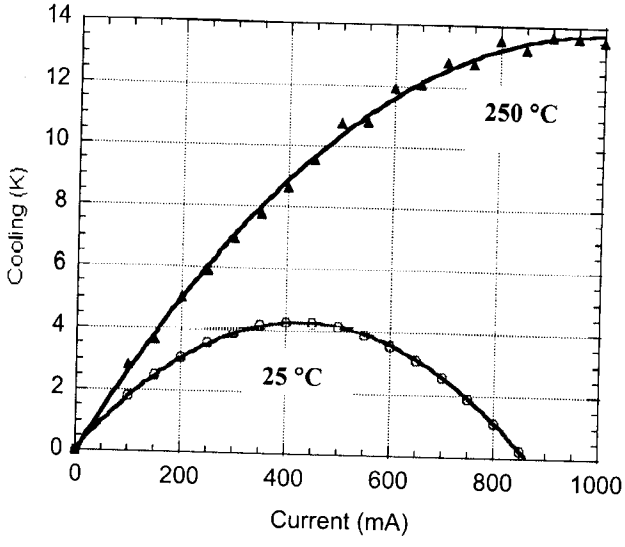

Figure 4. Measured cooling on $Si_{0.8}Ge_{0.2}$ 50 × 50 μm² devices at heat sink temperature of 25 °C and 250 °C.

Besides cooling temperature, cooling power density is another important parameter for microcoolers. Due to the small size of the microcooler, it is difficult to accurately measure cooling with a non-integrated external heat load to the device. We used integrated thermistor sensors to characterize the cooling power. After the microcooler processing described in the experiment section, narrow metal lines were deposited onto the top of the microcooler after another SiN_x passivation. By measuring the resistance, these narrow metal lines can be used as thermistor sensors to measure the temperature of the microcoolers. Sending current to these metal lines, they can work as a heat source and heat load to the microcoolers can be calculated. Figure 5 shows the cooling power measurement results on the $Si_{0.75}Ge_{0.25}$/Si superlattice 40 × 40 μm² microcooler at room temperature. A maximum cooling power density of 600 W/cm² was measured at zero cooling temperature, which is much larger than conventional bulk coolers.

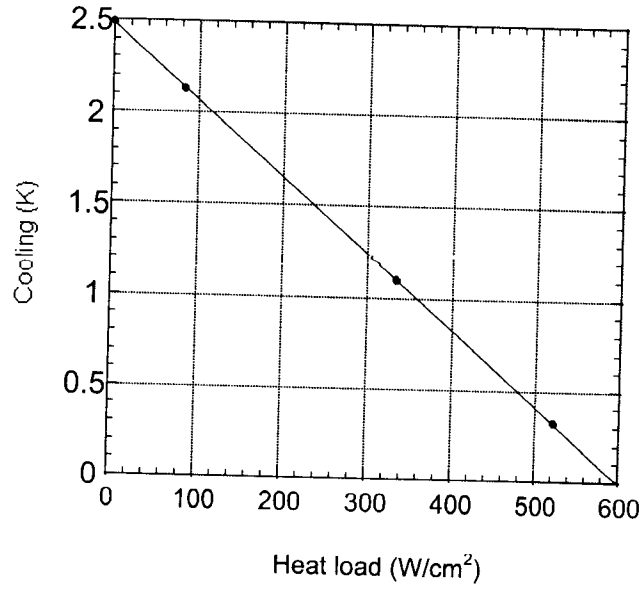

Figure 5. Measured maximum cooling vs. heat load on $Si_{0.75}Ge_{0.25}$/Si superlattice 40 × 40 μm² microcooler at room temperature.

Discussion

Over 4 K cooling was measured on both $Si_{0.8}Ge_{0.2}$ alloy and $Si_{0.75}Ge_{0.25}$/Si superlattice microcoolers at room temperature. Based on the TE properties of bulk SiGe, maximum cooling of over 10 K could be expected. This difference comes from some non-ideal effects in the microcooler, such as contact resistance, non-ideal heat sink, heat conduction from the top contact metal, the poor TE property of the silicon substrate, etc. Also the doping and structure of the TE materials haven't been optimized. With materials and device optimization, device performance can be improved.

The superlattice was used to enhance the TE cooling by thermionic emission and phonon engineering etc. Although over four-fold improvement over silicon was observed, the device performance difference between superlattice and SiGe

alloy is small. Since the superlattice in this paper was uniformly doped to around 6×10^{19} cm^{-3}, the effective barrier maybe too low for effective thermionic emission. Further investigation and superlattice optimization are needed.

Since the microcooler processing is compatible with IC processing, it is possible to monolithically integrate these microcoolers with Si-based microelectronics for localized cooling or temperature control. To further simplify the integration, lattice matched SiGeC/Si can be used to eliminate the buffer layer. [15]

Conclusions

$Si_{1-x}Ge_x$ and $Si_{1-x}Ge_x$/Si superlattice thin film microcoolers with the film thickness on the order of several microns were fabricated using integrated circuit processing technology. Micro thermocouples and integrated thermistor sensors were used to characterize these coolers. Maximum cooling power density on the order of hundreds of watts per square centimeter was measured at room temperature. With further device optimization, it is possible to monolithically integrate these coolers with Si-based microelectronic devices for localized cooling and temperature stabilization.

Acknowledgments

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