High Cooling Power Density of SiGe/Si Superlattice Microcoolers

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ABSTRACT

Fabrication and characterization of SiGe/Si superlattice microcoolers integrated with thin film resistors are described. Superlattice structures were used to enhance the device performance by reducing the thermal conductivity, and by providing selective emission of hot carriers through thermionic emission. Thin film metal resistors were integrated on top of the cooler devices and they were used as heat load for cooling power density measurement. Various device sizes were characterized. Net cooling over 4.1 K and a cooling power density of 598 W/cm^2 for 40×40 μm^2 devices were measured at room temperature.

INTRODUCTION

With the rapid development of VLSI technology, heat generation and thermal management are becoming one of the barriers to further increase clock speeds and decrease feature sizes. There has been an increasing demand for localized cooling and temperature stabilization of optoelectronic devices. Thermoelectric (TE) coolers based on bulk Bi_2Te_3 are commonly used for electronic and optoelectronic device cooling, but they cannot be directly integrated with the IC fabrication process. Recently p-type BiTe/SbTe thin film coolers have been demonstrated with high thermoelectric figure-of-merit and cooling power density[1]. Si-based microcoolers are attractive for their potential monolithic integration with Si microelectronics. SiGe is a good thermoelectric material especially for high temperature applications[2,3], and superlattice structures can further enhance the cooler performance by reducing the thermal conductivity between the hot and the cold junctions, and by selective emission of hot carriers above the barrier layers in the thermionic emission process[4-19]. SiGe/Si superlattice structures were grown on Si substrates using molecular beam epitaxy (MBE). Thin film resisters were integrated with the cooler devices. It shows the possibility to monolithically integrate these coolers with Si-based microelectronic devices for localized cooling and temperature stabilization.

EXPERIMENTAL DETAIS

The structure of the microcooler samples consisted of a 3 μm thick 200 × (5nm $Si_{0.7}Ge_{0.3}$/10nm Si) superlattice grown symmetrically strained on a buffer layer designed so that the in-plane lattice constant was approximately that of relaxed $Si_{0.8}Ge_{0.2}$. The doping level is 5×10^{19} cm^{-3} for both the superlattice and the buffer layer. A 0.5 μm $Si_{0.9}Ge_{0.1}$ cap layer was grown on the superlattice with the top 0.25 μm doped to 2×10^{20} cm^{-3} for device ohmic contact. This $Si_{0.7}Ge_{0.3}$/Si superlattice has a valance band offset of about 0.2 eV, and hot holes over this barrier produce thermionic cooling. In addition, superlattice structure has many interfaces that

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increase phonon scattering, and therefore lower thermal conductivity. The samples were grown with MBE on five inch diameter (001)-oriented Si substrates, doped to 0.001 ~ 0.006 Ω-cm with Boron.

Mesas 0.6 μm high were formed using reactive ion etching down to the SiGe/Si superlattice layer. 100 nm titanium layer was deposited to form a titanium silicide on the Silicon surface and to act as a metal barrier to separate SiGe and Al. Subsequently 1μm thick aluminum layer was deposited. To facilitate wire bonding, additional metal layers of titanium and gold were used. Annealing was done at a temperature of 450 °C for 5 seconds.

In order to facilitate integration of thin film resistor on top of the device, the metal contact to the cold junction was extended to the side with 0.3 micron thick SiN_x insulating layer underneath (see Fig. 1). In this single element cooler configuration, heat flow to the cold junction from the electrode pad has to be taken into account, and the pad width can be optimized to get a balance between heat conduction to the substrate and the resistive Joule heating in the metal layer. Coolers with various side pad widths were characterized for this purpose. Fig. 1a shows the scanning electron micrograph (SEM) of devices with an area of 6400 μm^2 which have different side pad widths. Fig. 1b shows the measured cooling on top of the device versus applied current. It can be seen that device #3 has the best performance. With further processing a thin film metal resister was integrated on top of the device and used as a thermal load for cooling power density measurement. An SEM image of the processed devices with the heater is shown in Fig. 2.

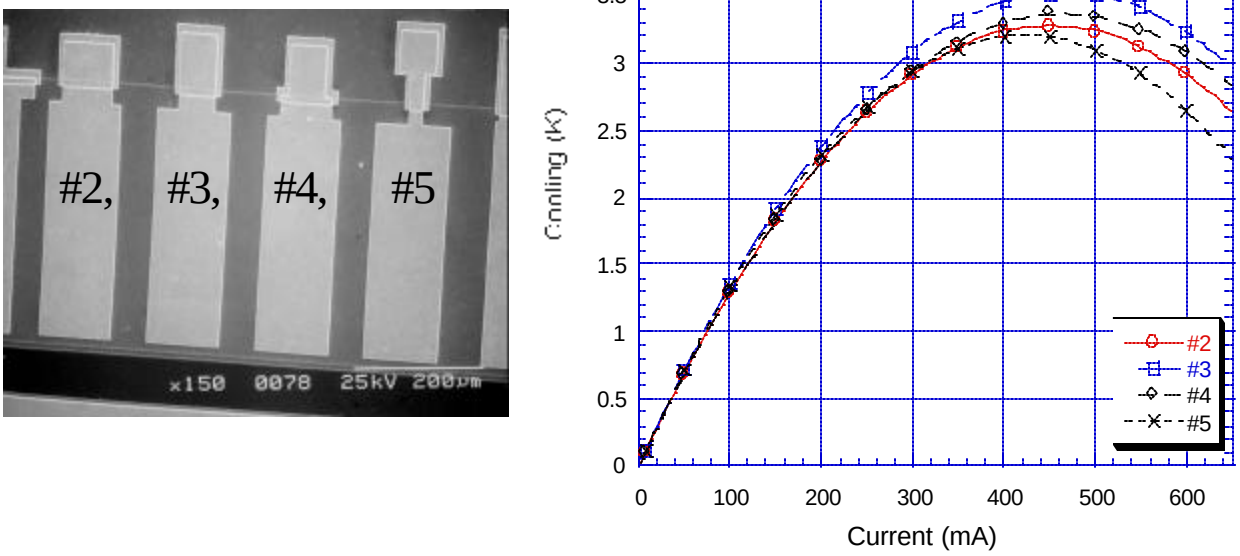

Fig. 1 (a) Devices with an area of 6400 μm^2 and with different side pad widths. (b) Measured cooling on top of the device versus current.

Devices were tested at room temperature. Device cooling was measured using two micro thermocouples, one thermocouple bead size ~50 micron was placed on top of the cooler and

another one on the substrate far away from the device. Fig. 3 shows the test results for coolers (processed without the heater on top) ranging in size from 40×40 μm^2 to 100×100 μm^2. The maximum cooling of about 4.1 K was measured for the 60×60 μm^2 device.

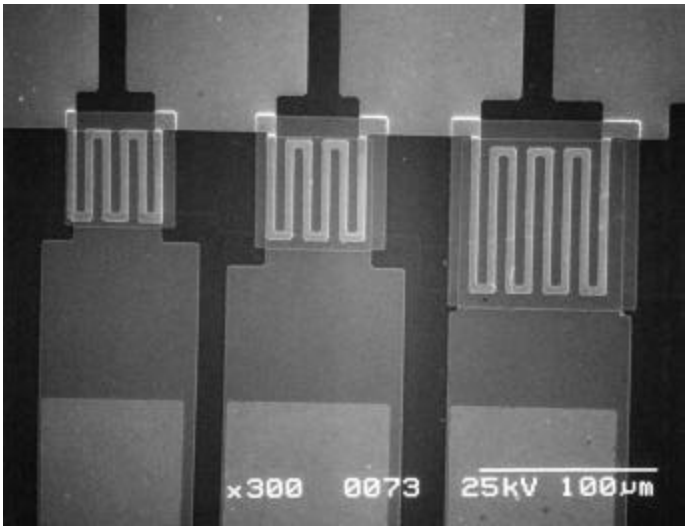

Fig. 2 Processed SiGe/Si coolers with integrated thin film metal wire resisters.

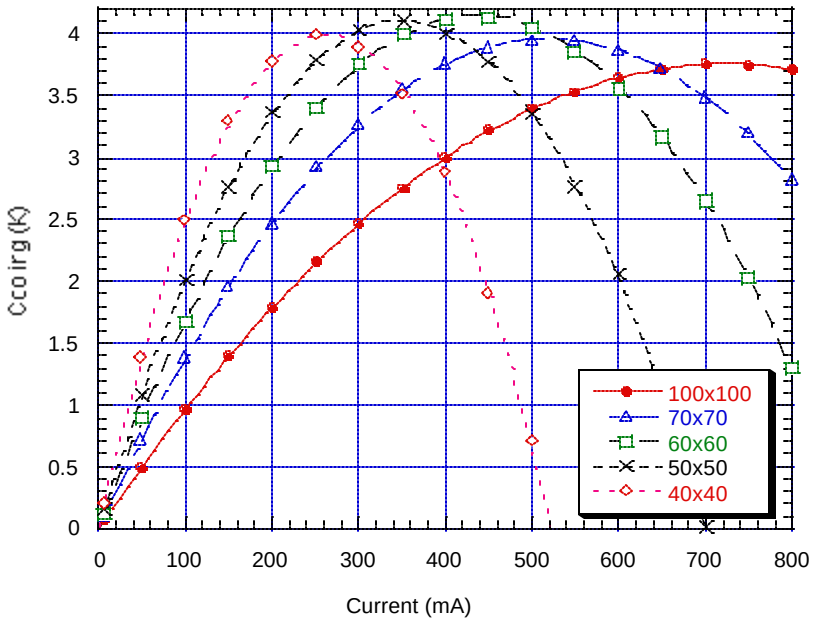

Fig. 3 Cooling measured on top of the device versus current for 40×40 μm^2, 50×50 μm^2, 60×60 μm^2, 70×70 um^2 and 100×100 μm^2 SiGe/Si coolers.

The integrated thin film wire resister was used as a heater. A constant electric current was applied through the metal wire to provide a constant heat load while the cooling with this thermal

load was measured. The maximum cooling power is defined as the heat load power density that makes the device's maximum cooling temperature equal to zero. Fig. 4 shows that the cooling versus heat load power density for 40×40 μm^2 device. It can be seen that this device has a maximum cooling power density of 598 W/cm^2 at room temperature.

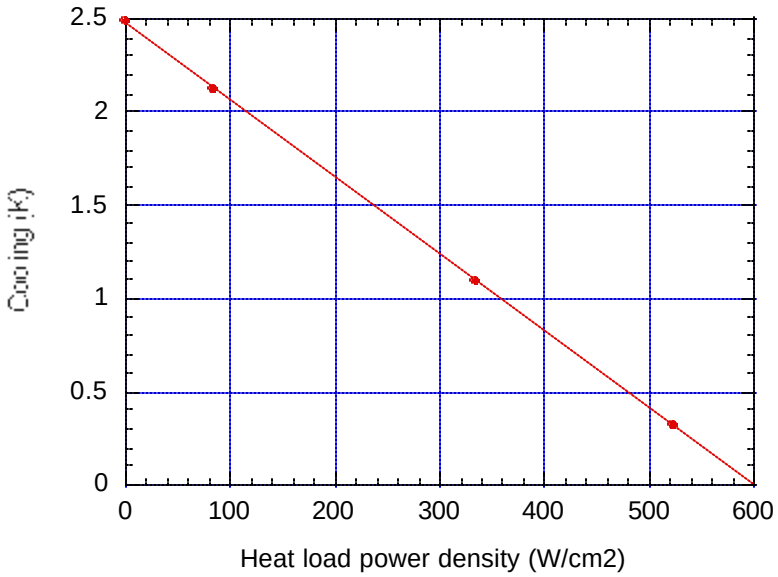

Fig. 4 Measured cooling power density for 40×40 μm^2 SiGe/Si cooler at room temperature.

DISCUSSION

According to conventional bulk thermoelectric cooler models, the maximum cooling is determined by the TE figure-of-merit and is independent of the cooler size. However, with the device minimization the cooler thermal and electrical resistances both become very small and non-ideal effects, such as metal-semiconductor contact resistance and heat sink thermal resistance, must be considered in the device modeling. These non-ideal effects not only reduce the maximum cooling but also make the cooling performance device size dependent. For example, the cooler thermal resistance is inversely proportional to the cooler area, while the thermal resistance of the silicon substrate beneath the device is inversely proportional to the square root of the cooler area[20,21]. The ratio of the cooler thermal resistance to the substrate (heat sink) thermal resistance increases with decreasing the device size. Therefore as the device gets smaller, substrate becomes closer to an ideal heat sink and the overall micro refrigerators cooling performance improves. Another difference from conventional bulk TE coolers is that the thin film microcoolers characterized here are single element devices instead of the p- and n-type array structures. One should consider heat conduction from side contact to the cold junction of the device. For the cooler structures in this paper, the side contact scales with the linear dimension of the cooler. Thus larger devices tend to be less affected by the heat conduction from side contact and also by the fixed thermal load of the thermocouple on top of the device. Because

of all the non-ideal effects, there is an optimal device size for the microcooler, which is shown in the measurements in Fig. 3 where 60 $\mu m \times 60$ μm devices have the largest cooling.

CONCLUSION

Thin film resister wires were integrated into the cooler devices, which were used as controllable electric thermal loads. A cooling power density of 598 W/cm^2 for coolers of 40×40 μm^2 and cooling up to 4.1 K for coolers of 60×60 μm^2 were measured at room temperature. With standard IC processing technology, thin film metal wire resisters were integrated into the cooler devices which are used as electric thermal load to the coolers. This shows the possibility of monolithic integration of devices with micro thin film coolers.

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