Proceedings of 2000 IMECE
Fundamentals of Heat Transfer in Mircrodevices and Microsystems
November 5-10, 2000 in Orlando, Florida

Paper Number: 2-8-2-15

# Transferred-Substrate InGaAsP-based thermionic emission coolers

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## ABSTRACT

Most optoelectronic devices are based on III-V semiconductors such as the InP/InGaAsP material system. Solid state refrigeration based on the same material system can be monolithically integrated with optoelectronics. Thermionic emission cooling from InGaAsP-based heterostructures has been shown experimentally to provide cooling power densities of several 100 W/cm$^2$. Cooling by several degrees across thin films on the order of a micron thick has been demonstrated. Thermionic emission of hot electrons over heterobarriers allows for enhanced cooling power beyond what is possible from the bulk thermoelectric properties. The thermal resistance of the InP growth substrate between the hot side of the thin film cooler and the heat sink is found to be a limitation in cooler performance. Several possibilities are examined for replacing the InP substrate with a higher thermally conducting one such as

silicon, copper, or even diamond, and a process for substrate transfer to a thin copper film has been developed. Three-dimensional simulations predict an order of magnitude improvement in the thermal resistance of the substrate. Experimental results of packaged InGaAsP coolers with copper substrates will be discussed.

## INTRODUCTION

The InP/InGaAsP material system has become exceedingly important in optoelectronic devices operating near 1.55μm. This wavelength corresponds to the optical fiber loss minimum, and has become the foundation for all long haul optical communication components and systems. An important problem for these high speed, high power optoelectronic components is heating and temperature stabilization. For example, most high-speed lasers are limited by thermal effects preventing them from being biased far enough above threshold to ever get to intrinsic device limits. Distributed feedback (DFB) lasers and vertical cavity surface emitting lasers (VCSEL's) are capable of generating large heat power densities on the order of kW's/cm$^2$ over areas a few hundred square microns in size [1]. Furthermore, with the advent of dense wavelength division multiplexing (DWDM), the wavelength sensitivity of optoelectronic devices to temperature fluctuations has become critical. Thermoelectric(TE) coolers are most commonly used to meet the demands of temperature stabilization, however they have a few disadvantages. It is the troublesome task of integrating the TE cooler with optoelectronic devices which results in higher component cost and reduced reliability, and is the motivation for an alternative solution.

Cooling by thermionic emission of hot electrons over semiconductor heterobarriers was first proposed by Shakouri *et. al.* as a means of enhancing cooling power beyond what is possible from the bulk thermoelectric properties of the material [2,3]. The advantage of this approach is that the coolers

can be made with similar III-V semiconductor materials allowing for monolithic integration with optoelectronics. We have shown previously [4] that these coolers are capable of cooling power densities of 100's W/cm$^2$, and with more optimized structures it is expected that greater than 1 kW/cm$^2$ is possible. One of the ways to optimize the device is to reduce the substrate thermal resistance that is present between the hot side of the thin-film cooler and the heat sink [5]. This work examines the possibilities for replacing the poor thermally conducting InP growth substrate with a more optimal one such as silicon, copper, and CVD-grown diamond.

## SUBSTRATE TRANSFER PROCESSES

The processes for substrate transfer considered here can be categorized as either bonded or deposited. Bonded refers to the joining of the epitaxial grown layers to a surrogate substrate where the original substrate is removed before or after the union. In most cases an intermediate material, such as a metal, solder, or epoxy, is used to facilitate a complete and uniform junction. A deposited process means that the new substrate is actually made right on the epitaxial layers such as in vacuum evaporation or electroplating. In any of these above cases, careful attention must be paid to the material properties and a trade-off between the coefficient of thermal expansion (CTE) and thermal conductivity is often the issue. Figure 1 shows the CTE and thermal conductivities for the semiconductors and metals considered here [6,7]. Comparing the CTE for the InP-based films to that of most pure metals we see that there is a large mismatch. There are a few refractory metals like tungsten and molybdenum (not shown in figure) that have much closer CTE's, but their thermal conductivity is not as great as gold or copper. The CVD Diamond with a CTE of 2.5x10$^{-6}$ K$^{-1}$ and a thermal conductivity of 1200 W/mK seems to be a good compromise between the two, however it is a much more expensive material and it is difficult to get highly polished surfaces.

## EXPERIMENTAL RESULTS & DISCUSSION

The first substrate transfer process that was investigated was to a silicon substrate by Au-Au fusion. This process was attractive since bonding parameters had already been determined from prior familiarity with this process [8]. Characterization samples were used to determine the feasibility of the process for later thermionic cooler processing. Figure 2 shows the steps used in the Au-Au bonding. After sample cleaning, successive metal depositions of 500Å – Ti, 1000Å – Pt, and 15000Å – Au were performed in an e-beam evaporation system. The purpose of the titanium layer was for good adhesion, while the platinum layer blocked any spiking of the gold during the temperature cycling of the fusion process. The samples were then brought into contact and held under pressure using a rubber-boot vacuum fixture on a hot plate. The temperature was ramped up at 1°C/min. to a temperature of 350 °C, held for five minutes, and then ramped down at the same rate. The slow ramping was to reduce stress caused by the CTE mismatch between the wafer and the gold. After the fusion the InP substrate was then etched off in a solution of $3HCL:1H_2O$, and the remaining epi layers were examined under an optical microscope. Of the two samples bonded, only one appeared to have mostly fused however there were bubbles present in several places on the sample. It was concluded that the process was not reliable or robust enough to be worth pursuing for an increase in thermal conductivity of only a factor of two. Evaporating a layer of tin after the gold evaporation is expected to help with the reliability of this process since the solder can actually reach its melting temperature and reflow to fill in any voids. However it is unknown as to whether the large CTE mismatch would cause the epitaxial layers to crack.

Au-Au fusion using a diamond substrate (300μm thick) was briefly attempted, however it became evident early on that the CVD-grown substrates used were not planar enough and showed a bowing across the substrate of 3 μm and a maximum surface roughness of 1.2 μm. Highly planar

samples and crystallographic surfaces are necessary for quality Au-Au fusions. The use of tin was instead employed in order to planarize the surface. When the sample reaches a temperature nearing 300°C, the Au and Sn diffuse into each other and form a Au-Sn eutectic that has a higher thermal conductivity and melting temperature than the pure tin. Single epitaxial layers have been somewhat successfully bonded in this manner. No indications of the epi layer cracking have yet to be observed.

The last procedure discussed involves the transfer of a 2 μm thick epitaxial grown thermionic cooler structure to a thermally evaporated 10 μm thick copper substrate. The thin film cooler structure was grown by metal organic chemical vapor deposition (MOCVD) and consists of a 2 μm thick superlattice barrier (80 periods of 18 nm InGaAs and 7 nm InP) surrounded by n+ InGaAs cathode and anode layers that were 0.3 μm and 0.5 μm thick respectively and doped to $8x10^{18}$ $cm^{-3}$. A blanket evaporation of Ti/Pt/Au (100/500/5000Å) was performed to make an ohmic contact to the topmost InGaAs layer. Three successive runs in a thermal evaporator were executed to deposit a total of 10 μm of Cu. Before the first deposition of Cu, and each time the system was vented to replenish the Cu source, a 500Å layer of Cr was deposited as a sticking layer. After the desired copper thickness was reached, a 1 μm thick layer of tin was thermally evaporated for later use in the device packaging. The processing procedure from this point is outlined in figure 3. The sample is now mounted Cu-side down onto a larger piece of silicon using wax. The InP substrate is then removed with the same wet etching solution, exposing the epitaxial layers. Ti/Pt/Au ohmic contacts were patterned on the surface and mesas were defined by dry etching techniques. The devices were then diced into rows with a diamond saw and the wax was removed with acetone. The individual rows of devices were then attached to the package using the already deposited tin. Figure 4 shows an SEM of a packaged device. While about 75% of the sample survived all of the processing steps up to the dicing, most of the sample was lost due to the large mechanical stress associated with dicing. Future processing runs will use a wet chemical

etching of the copper to separate the devices in to sizes that are manageable with vacuum tweezers. The maximum cooling achieved with this device was only 0.1°C, compared to the same structure processed on the growth substrate which cooled by 0.7°C. Therefore even with the large thermal resistance of the InP substrate, a 0.7 degree gradient was held across a 2 μm thin film corresponding to a cooling power density of several hundred W/cm$^2$. The Cu-substrate device had a cooling power that was almost an order of magnitude worse. We believe the reason for this is a large thermal resistance at the interface between the copper and the package, namely the solder layer is not performing correctly. The SEM photo in figure 4 indicates that there is indeed an air gap in this region. Better methods for packaging are currently being examined.

While the packaging continues to be a challenge for the Cu-substrate samples, the process itself appears to work adequately. No cracking or bowing of the epitaxial layer was observed, even though film stress values have been reported in the range of 50 Mpa for sputtered Au[9]. Electroplating is known to result in thin metal films with much less stress on the order of 1 MPa in plated Cu[10]. Electroplating was not considered in this work due to the small size of the samples and the foreseen difficulties with obtaining uniform robust metal layers, however there has been reports of success on 2" diameter wafers with this process for HBT integrated circuits [11].

## 6. CONCLUSIONS

In this work we have examined several different processes for the transfer of InGaAsP-based thin films to better thermally conducting substrates such as silicon, copper, and diamond. Care should be taken in optimizing both the thermal conductivity of the replacement substrate as well as the CTE. The bonding to silicon substrates resulted in only mediocre quality bonds and was determined to not be worth continuing for only a factor of two improvement in thermal conductivity. The diamond substrate

transfer looks promising, but polishing the surfaces to an acceptable bowing and roughness has proven difficult. The 10μm Cu-substrate transfer process seems to work, but better packaging techniques are necessary. In either the thicker diamond or very thin copper, an order of magnitude improvement in thermal resistance is expected. This is expected to impact the maximum cooling power density of the thin film thermionic coolers on the order of the same amount.

## ACKNOWLEDGMENTS

This work was supported by the Army Research Office through the DARPA/HERETIC program and by the Office of Naval Research.

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**Figures:**

**Fig. 1** Thermal conductivity and coefficient of thermal expansion for considered materials [6,7]. Off axis is diamond thermal conductivity = 1200 W/mK and the epoxy CTE = $31 \times 10^{-6}$ $K^{-1}$

**Fig. 2** Au-Au fusion process for transferring epitaxial layers from the InP growth substrate to a Si substrate. The steps are (a) E-beam evaporation of Ti/Pt/Au metallization, (b) Au-Au fusion under pressure and temperature, and (c) InP substrate removal. The process can be generalized to any surrogate substrate.

**Fig. 3** Cu-substrate transfer process. The steps are (a) E-beam evaporate ohmic metal, copper substrate, and solder layers, and mount epi side down to a silicon carrier with wax. (b) Remove InP substrate with a wet etch and (c) deposit top metal to etch mesas. Dice samples and remove the wax. (d) Package and wire bond devices. (Tin layer not shown)

**Fig. 4** Scanning electron micrograph (SEM) of a packaged thin-film thermionic cooler on a 10 μm thick copper substrate. It is clear from the photo that there are large gaps that the solder did not spread to during packaging.

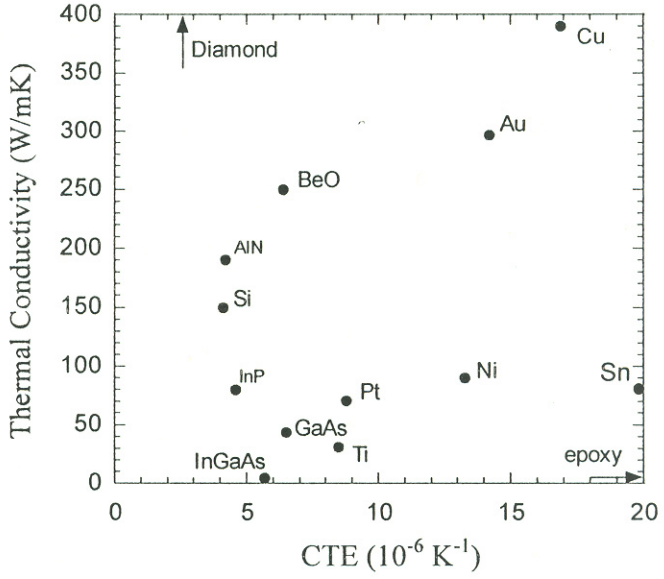
Thermal Conductivity (W/mK)
CTE ($10^{-6}$ $K^{-1}$)
Diamond
Cu
Au
BeO
AlN
Si
InP
Pt
Ni
Sn
GaAs
Ti
InGaAs
epoxy
0
50
100
150
200
250
300
350
400
0
5
10
15
20

**Fig. 1**

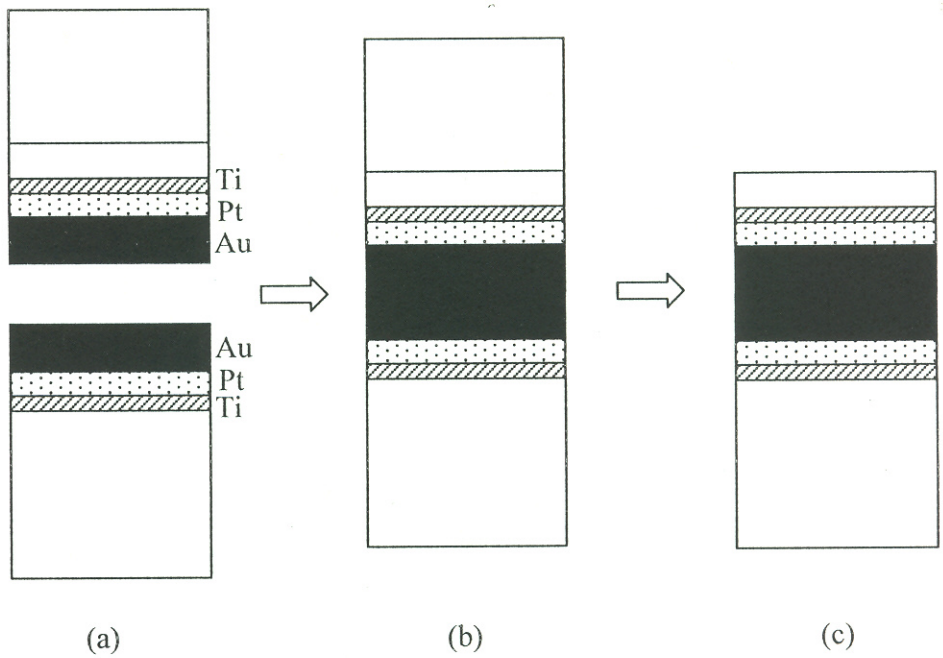


**Fig. 2**

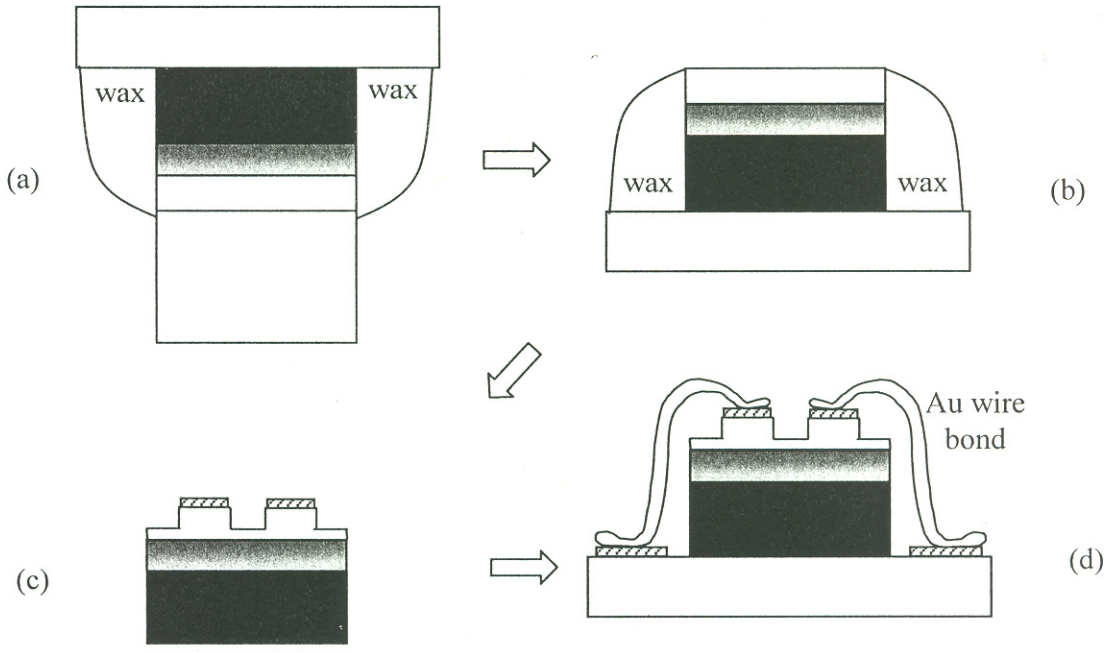


**Fig. 3**

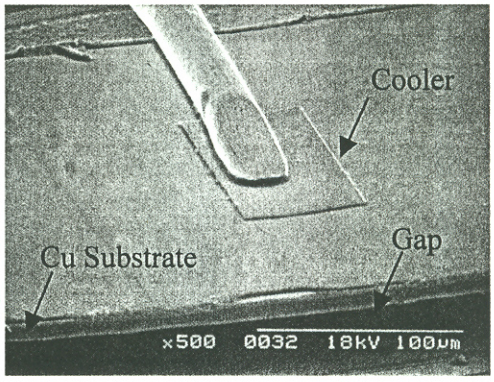


**Fig. 4**