Conclusions: A turbo TCM/FPM scheme has been proposed that can achieve considerable coding gains over turbo TCM 8PSK and conventional TCM/FPM schemes without sacrificing power and bandwidth efficiency. The performance of a DS/SSMA system using turbo TCM/FPM improves significantly over a multipath Rician fading channel. This scheme is attractive for power-limited and band-limited environments.

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Xiaoming Peng and E. Gunawan (*School of Electrical and Electronic Engineering, Blk. S1, Nanyang Technological University, Singapore 639798, Republic of Singapore*)

E-mail: egunawan@ntu.edu.sg

References

1 ROBERTSON, P., and WORZ, T.: 'Bandwidth-efficient turbo trellis-coded modulation using punctured component codes', *IEEE J. Sel. Areas Commun.*, 1998, **16**, (2)
2 PADOVANI, R., and WOLF, J.K.: 'Coded phase/frequency modulation', *IEEE Trans. Commun.*, 1986, **COM-34**, pp. 446–453
3 DU, JUN, VUCETIC, B., and ZHANG, LIN: 'Construction of new MPSK trellis coded modulation for fading channels', *IEEE Trans. Commun.*, 1995, **43**, (2), pp. 776–784

High cooling power density SiGe/Si micro-coolers

X. Fan, G. Zeng, E. Croke, C. LaBounty, C.C. Ahn, D. Vashaee, A. Shakouri and J.E. Bowers

SiGe/Si superlattice micro-coolers are investigated experimentally. They can be monolithically integrated with Si-based microelectronic devices to achieve localised cooling and temperature control. Cooling by as much as 4.2K at 25°C and 12K at 200°C was measured on 3μm thick, 60 × 60μm² devices. This corresponds to maximum cooling power densities approaching kW/cm².

Thermoelectric (TE) refrigeration is an active solid-state cooling method with high reliability. TE coolers have been widely used in cooling and temperature stabilisation of microelectronic and opto-electronic devices to achieve precise operational characteristics. Conventional TE coolers are discrete devices with dimensions of the order of millimetres to centimetres, and they generally cool an entire packaged chip. Micro-coolers monolithically integrated with microelectronic and optoelectronic devices provide a more efficient way of temperature regulation by selectively cooling critical components. Compared with traditional TE coolers, integrated coolers are more compact, consume less power, and have a faster response. They can also be used to construct multiple independently temperature-controlled regions on a single chip.

For monolithic integration, conventional semiconductor materials with good TE properties are required. SiGe alloy is one of the best TE materials for high temperature applications. At room temperature, based on the TE properties of bulk SiGe [1], it can give a maximum cooling of over 10K. Although this cooling is less than that of Bi_2Te_3 coolers, SiGe coolers can be monolithically integrated with Si-based microelectronic devices and have many potential applications. Recently, superlattice structures have been proposed to increase the thermoelectric figure of merit ZT beyond that of alloy materials by quantum confinement [2], thermionic emission [3] and carrier pocket engineering [4]. SiGe/Si micro-coolers were first demonstrated on *n*-type samples [5]. In this Letter, we report our experimental work on *p*-type SiGe/Si superlattice micro-coolers with improved performance. This paves the road to fabricate an array of *n*- and *p*-type coolers electrically in series and thermally in parallel and thus achieve larger amounts of cooling.

The micro-cooler structure uses cross-plane electrical transport as shown in Fig. 1. The main part of the cooler is a 3μm strain compensated SiGe/Si superlattice. It consists of 200 periods of (12nm $Si_{0.75}Ge_{0.25}$/3nm Si), doped with boron to about $6 \times 10^{19}cm^{-3}$. The $Si_{0.75}Ge_{0.25}$/Si superlattice has a valence band offset of about 0.16eV [6], and hot holes going over this barrier can produce thermionic cooling [3]. This superlattice was grown using molecular beam epitaxy (MBE). Its average lattice constant is that of $Si_{0.8}Ge_{0.2}$, and a buffer layer is required for it to be grown on a Si substrate. To reduce the material growth time in the MBE system, the buffer layer was grown on a p^+ (001) Si substrate by chemical vapour deposition (CVD) in the form of a graded SiGe structure. The boron doping in the buffer layer is $5 \times 10^{19}cm^{-3}$. Following the superlattice growth, a 0.3μm $Si_{0.8}Ge_{0.2}$ cap layer was grown with a boron doping of $2 \times 10^{20}cm^{-3}$ to allow for a good ohmic contact to the device. Fig. 2 shows a cross-section transmission electron microscopy (TEM) image of the MBE grown SiGe/Si superlattice.

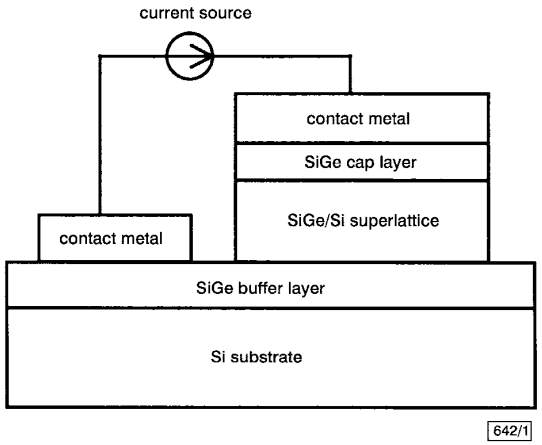

Fig. 1 *Structure of SiGe/Si micro-cooler*

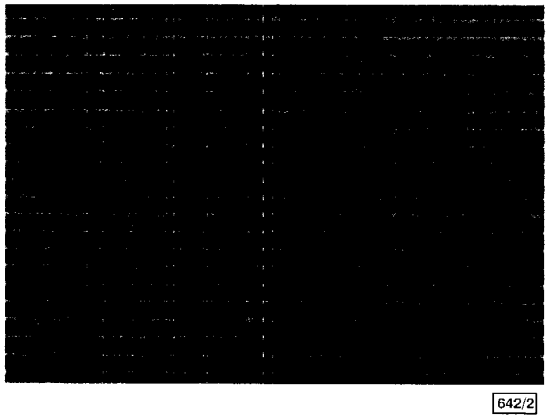

Fig. 2 *TEM image of SiGe/Si superlattice*
Dark lines are 12nm $Si_{0.75}Ge_{0.25}$ layers, light lines are 3nm Si layers

The SiGe/Si micro-coolers are fabricated with standard silicon integrated circuit technology. The cooler device areas were defined by etching mesas down to the SiGe buffer layer. Ti/Al metallisation was made on top of the mesa and on the SiGe buffer layer next to the mesa for top and bottom contacts respectively. SiGe/Si superlattice coolers with mesa sizes ranging from $30 \times 30\mu m^2$ to $150 \times 150\mu m^2$ were fabricated on the same wafer. For comparison, bulk Si micro-coolers were also fabricated on p^+ Si substrates with similar device structures and processing.

The coolers were tested on a heat sink stage. Micro-thermocouples were used to measure the temperature on top of the mesa, and the cooling is relative to the value at zero current. The results for $60 \times 60\mu m^2$ devices are shown in Fig. 3 for both SiGe/Si superlattice and Si coolers at a heat sink temperature of 25°C. Cooling by as much as 4.2K was measured on SiGe/Si superlattice coolers. This is over four-fold improvement compared to the bulk Si coolers.

The SiGe/Si micro-coolers perform better at higher temperatures. Fig. 4 shows the measured cooling on $60 \times 60\mu m^2$ SiGe/Si coolers at various heat sink temperatures. The maximum cooling increased from 4.2K at 25°C to over 12K at 200°C. Since most of

the cooling happens over the 3μm superlattice layer, the corresponding maximum cooling power density is of the order of kW/cm^2. This is much larger than that of conventional bulk TE coolers because of the thin film cooler structure of our devices. The improved cooling at higher temperatures agrees with the thermoelectric properties of SiGe alloy, the TE figure of merit of which, ZT, increases with temperature up to 900°C [1]. The high temperature results of the SiGe/Si micro-coolers suggest potential applications beyond the upper temperature limits of conventional Bi_2Te_3 TE coolers.

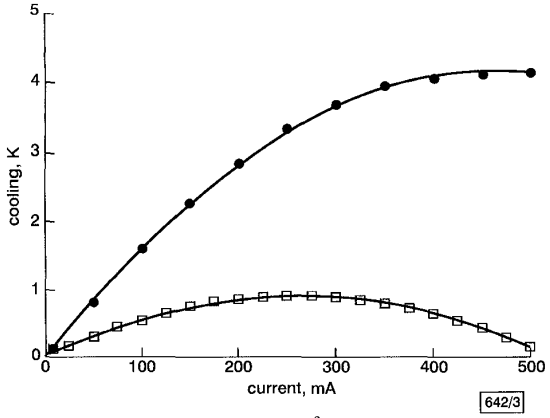

Fig. 3 *Cooling measured on 60 × 60μm² coolers at heat sink temperature of 25°C*

—●— SiGe/Si superlattice
—□— Si

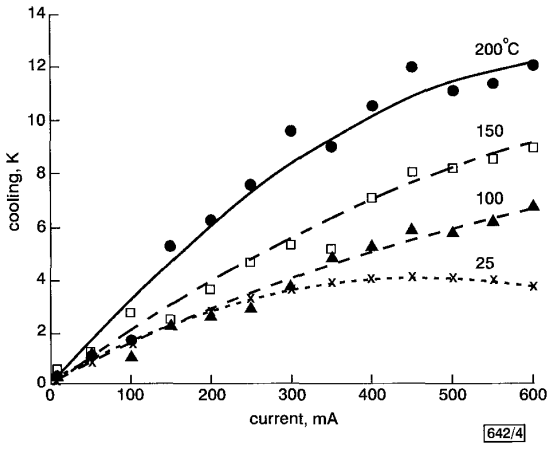

Fig. 4 *Cooling measured on 60 × 60μm² SiGe/Si superlattice coolers at various heat sink temperatures*

Device simulations show that the performance of the micro-coolers can be improved by reducing the contact resistance, reducing the Joule heating and heat conduction from the metal wire connected to the cold junction of the cooler, thinning or removing the Si substrate, and improving the material properties of the superlattice. With optimised device and material deign, cooling up to tens of degree at room temperature is possible. Furthermore, SiGe/Si micro-coolers can be monolithically integrated with Si and SiGe microelectronic devices to achieve compact and reliable localised cooling and active temperature control.

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X. Fan, G. Zeng, C. LaBounty and J.E. Bowers (*Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA*)

E-mail: fan@opto.ucsb.edu

E. Croke (*HRL Laboratories, LLC, Malibu, CA 90265, USA*)

C.C. Ahn (*California Institute of Technology, Pasadena, CA 91125, USA*)

D. Vashaee and A. Shakouri (*Baskin School of Engineering, University of California, Santa Cruz, CA 95064, USA*)

References

1 ROWE, D.M.: 'CRC handbook of thermoeletronics' (CRC Press, New York, 1995)

2 HICKS, L.K., and DRESSELHAUS, M.S.: 'Effect of quantum-well structures on the thermoelectric figure of merit', *Phys. Rev. B*, 1993, **47**, (16), pp. 12727–12731

3 SHAKOURI, A., and BOWERS, J.E.: 'Heterostructure integrated thermionic coolers', *Appl. Phys. Lett.*, 1997, **71**, (9), pp. 1234–1236

4 KOGA, T., SUN, X., CRONIN, S.B., and DRESSELHAUS, M.S.: 'Carrier pocket engineering applied to "strained" Si/Ge superlattices to design useful thermoelectric materials', *Appl. Phys. Lett.*, 1999, **75**, (16), pp. 2438–2440

5 ZENG, G., SHAKOURI, A., LABOUNTY, C., ROBINSON, G., CROKE, E., ABRAHAM, P., FAN, X., REESE, H., and BOWERS, J.E.: 'SiGe micro-cooler', *Electron. Lett.*, 1999, **35**, (24), pp. 2146–2147

6 PEOPLE, R., and BEAN, J.C.: 'Band alignments of coherently strained Ge_xSi_{1-x}/Si heterostructures on ⟨001⟩ Ge_ySi_{1-y} substrates', *Appl. Phys. Lett.*, 1986, **48**, (8), pp. 538–540

Low level and reflection phase noise measurements on a FET

O. Llopis, J.B. Juraver, G. Cibiel and J. Graffeuil

The residual phase noise of a PHEMT device is studied in two unusual configurations: in transmission mode with a low input microwave power on the device, and in reflection mode. Measurements clearly reveal some fundamental aspects of the phase noise generation in this device: the phase noise is a modulation mechanism which still exists in the linear regime and in which the gate reactance fluctuations play an important role.

Introduction: The phase noise generation in an active device has always been a complex and not well understood process. Over past years there have been different, competing, modelling approaches to determine which transistor noise model [1 – 4] or which noise conversion process [5] should be considered. In this Letter, residual phase noise (or open loop phase noise) investigations are shown to be an efficient approach to identify the main noise conversion processes in a microwave field effect transistor (FET). The emphasis is put on low level and reflection mode measurements. The first experiment demonstrates the modulation process involved in the phase noise generation, while the other is the proof of the importance of the gate reactance fluctuations in this mechanism.

Residual phase noise measurement for phase noise modelling: As shown by Leeson in 1966 [6], the active device phase fluctuations $\Delta\phi$ in an oscillator loop are directly converted into frequency fluctuations Δf. Therefore, investigations on Δf can be substituted for investigations on $\Delta\phi$, which feature two strong advantages. The first one deals with the simulation domain: the analysis of a driven circuit (an amplifier) is easier and quicker than the analysis of an autonomous circuit (an oscillator). The second one deals with the experimental domain: the amplifier is a simpler device than an oscillator and its characterisation can be performed in a very precise way, since only two experimental parameters have to be considered, i.e. the bias conditions and the microwave input power. Moreover, phase noise investigations are possible down to the linear regime, in contrast to the oscillator case which is intrinsically nonlinear. The only difficulty is due to the low phase noise levels that must be measured: a low noise phase detector and an appropriate cancellation of the source AM and FM noise contributions are required. Our measurement bench makes use of a two mixer technique, which allows the cancellation of the mixer noise through a cross-correlation process. The input source is a battery-biased 10GHz dielectric resonator oscillator (DRO). The noise floor of the experiment is about –175dBc/Hz at 10kHz offset from