Experimental Characterization and Modeling of InP-based Microcoolers

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ABSTRACT

We present experimental and theoretical characterization of InP-based heterostructure integrated thermionic (HIT) coolers. In particular, the effect of doping on overall device performance is characterized. Several thin-film cooler devices have been fabricated and analyzed. The coolers consist of a 1μm thick superlattice structure composed of 25 periods of InGaAs well and InGaAsP ($\lambda_{gap} \approx 1.3\mu m$) barrier layers 10 and 30nm thick, respectively. The superlattice is surrounded by highly-doped InGaAs layers that serve as the cathode and anode. All layers are lattice-matched to the n-type InP substrate. N-type doping of the well layers varies from $1.5\times10^{18}cm^{-3}$ to $8\times10^{18}cm^{-3}$ between devices, while the barrier layers are undoped. Device cooling performance was measured at room-temperature. Device current-versus-voltage relationships were measured from 45K to room-temperature. Detailed models of electron transport in superlattice structures were used to simulate device performance. Experimental results indicate that low-temperature electron transport is a strong function of well layer doping and that maximum cooling will decrease as this doping is increased. Theoretical models of both I-V curves and maximum cooling agree well with experimental results. The findings indicate that low-temperature electron transport is useful to characterize potential barriers and energy filtering in HIT coolers.

INTRODUCTION

Modern electronic and optoelectronic components require active temperature stabilization for optimum performance. Most optoelectronic devices used in communication systems are composed of InP-based materials. Conventional thermoelectric (TE) coolers can satisfy cooling requirements, but they are prohibitively large and expensive due to difficulties in integration with the devices to be cooled [1]. Heterostructure integrated thermionic (HIT) microcoolers have been proposed to be monolithically integrated with optoelectronic devices, thereby considerably reducing size and cost constraints [2, 3].

TE coolers utilize the Peltier effect for heat transfer. In addition to exploiting the Peltier effect for cooling, HIT microcoolers employ thermionic (TI) emission to increase the cooling power of standard TE coolers. In TI emission, electrons are emitted from the cathode over a potential barrier to the anode. This emission process is useful in heat transfer because electrons with higher energies (hot electrons) are able to traverse the potential barrier to the anode while electrons with lower energies (cold electrons) remain confined by the potential barrier to the cathode. This is an evaporative cooling of the electron gas at the cathode. At low biases and in the linear transport regime, an "effective" Seebeck coefficient and electrical conductivity for the device can be defined that have been modified by the thermionic emission of electrons. The overall performance of TE materials is given by the effective figure-of-merit

	Anode		Superlattice (25 periods)				Cathode				Contact			
	InGaAs		InGaAsP (λ_{gap}≈1.3μm)		InGaAs		InGaAs				Ni	AuGe	Ni	Au
Device	t (μm)	N_D ($\times 10^{18}cm^{-3}$)	t (nm)	N_D ($\times 10^{18}cm^{-3}$)	t (nm)	N_D ($\times 10^{18}cm^{-3}$)	t (μm)	N_D ($\times 10^{18}cm^{-3}$)	t (μm)	N_D ($\times 10^{19}cm^{-3}$)	t (nm)	t (nm)	t (nm)	t (μm)
LL1	0.3	1.5	10	undoped	30	1.5	0.2	1.5	0.1	2	5	10	100	1
LL2	"	3	"	"	"	3	"	3	"	2	"	"	"	"
LL3	"	5	"	"	"	5	"	5	"	2	"	"	"	"
LL4	"	8	"	"	"	8	"	8	"	2	"	"	"	"

Table 1: HIT cooler device layer and contact detail

$$ZT = S^2\sigma T\beta^{-1}$$

where S, σ and β are the Seebeck coefficient, electrical conductivity, and thermal conductivity respectively of the material and T is the ambient temperature. The ZT of HIT coolers can be optimized at various temperatures by adjusting the dopant concentration in the wells and the thickness and height of the potential barriers [4, 5]. A ZT increase of an order of magnitude over bulk Peltier values is possible using TI emission in heterostructures [6, 7].

Study of electronic properties of highly-degenerate semiconducting superlattice structures at low-temperature reveals important information regarding the energy filtering of electrons near the Fermi energy E_F by the potential barriers. It is in this regime that electron transport is strongly dependent upon barrier height E_b. Low-temperature I-V measurements were taken on HIT coolers consisting of InGaAs/InGaAsP superlattice structures of different quantum well layer dopant concentrations to determine how changes in E_F affect device characteristics. We have determined experimentally that as E_F increases into the conduction band, the affect of the potential barrier layers on low-temperature electron transport decreases, resulting in decreased device resistance. The measured resistance values agree well with calculations based on a modified linear Boltzmann transport equation that takes into account the quantum mechanical transmission coefficient in the superlattice. Decreased room-temperature cooling of HIT devices as well doping is increased is also predicted in theory and verified experimentally.

EXPERIMENT and THEORETICAL MODELS

Device details

N-type devices were grown lattice-matched to InP using metal organic chemical vapor deposition (MOCVD). The devices consist of superlattice structures 1μm thick surrounded by InGaAs anode and cathode layers. The cathode layer was highly doped to reduce contact resistance. N-type substrate was used to minimize Joule heating. Four devices of different well layer dopant concentrations were fabricated. 120×120μm mesas were reactive-ion etched down to the InGaAs anode layer. Anode and cathode ohmic contacts were formed by electron-beam evaporation. Detailed layer and contact information is listed in Table 1. A 300nm layer of SiN electrically isolated the cathode contact from the substrate. Finally, the substrate was

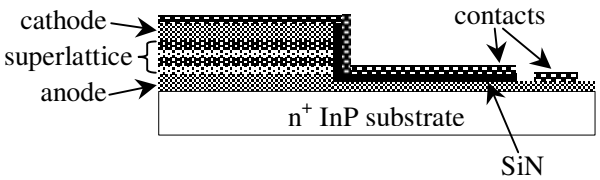

Figure 1: Diagram of HIT cooler

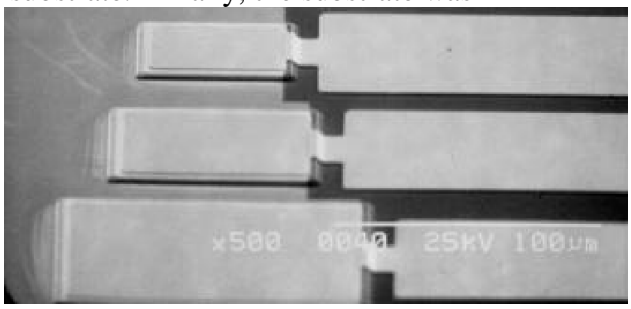

Figure 2: SEM image of HIT coolers

mechanically lapped to a thickness of 125μm to reduce the thermal resistance between the anode and the backside of the substrate. Figure 1 above is a cross-sectional diagram of the HIT cooler. Figure 2 above is a scanning electron microscopy (SEM) image of HIT devices of various sizes.

Low-temperature I-V measurement

Devices were mounted, using silver paste, to a chip-carrier of good thermal conductivity and wire-bonded to package leads. The chip-carrier was then mounted to the cryostat cold-stage using silver paste. A thermocouple was mounted on the chip-carrier near the device to monitor the device temperature relative to the cold-stage temperature. The reference thermocouple was placed adjacent to a diode temperature sensor that controlled the cold-stage temperature in feedback with the stage heater. The experimental arrangement is diagrammed in Figure 3. The cryostat was evacuated to a pressure down to the 10^{-5} Torr range. A continuous flow of liquid helium was used to cool the cold-stage down to a temperature as low as 10K. Due to ambient radiation and the thermal resistance between the device and the cold-stage, a temperature difference existed between the device and the cold-stage. The lowest device temperature achieved was approximately 45K. Four-wire I-V measurements were taken at various temperatures at currents increasing logarithmically from 1μA to approximately 105mA. Low currents were necessary to minimize Joule heating in the devices (as measured by the thermocouple mounted to the chip-carrier) that could adversely affect the measurements.

Room-temperature cooling measurement

Devices were mounted to a massive copper stage using thermally-conductive paste. The temperature of the stage was stabilized using a thermoelectric cooler (TEC) in feedback with a thermistor placed beneath the surface of the stage near the device substrate. Two micro-thermocouples of 2mil diameter leads were used to measure the surface temperature of the metal contact directly above the cathode. The reference thermocouple was placed on the surface of the stage near the substrate. Thermal compound was used to improve the thermal contact of both thermocouples. The reference temperature was assumed to be the temperature of the anode. Due to the small diameter of the thermocouple leads, the thermal load on the device by the thermocouple was assumed to be negligible. Two microprobes were used to drive currents up to approximately 150mA through the device. The cathode probe was placed as far from the cathode as possible to reduce its thermal load, which was also assumed to be negligible. The cooling measurement arrangement is presented in Figure 4.

Electron transport models

A linear Boltzmann transport equation was used to calculate the I-V characteristics of the HIT device. Conventional bulk transport was modified taking into account 2D states in the well and 3D states above the well and in the barrier. In addition, the quantum mechanical

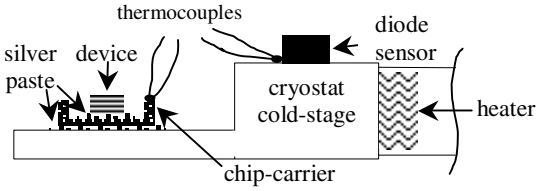

Figure 3: Diagram of low-temperature measurement

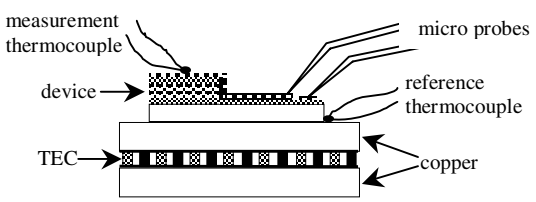

Figure 4: Diagram of cooling measurement

Device	E_F (meV)	E_b (meV)	m_{eff}/m_0 (barrier)	m_{eff}/m_0 (well)	μ ($cm^2V^{-1}s^{-1}$)	v_s ($cm\,s^{-1}$)	α (eV^{-1})
LL1	66.3	90	0.07	0.041	10^3	10^7	2.2
LL2	77.1	95	"	"	"	"	"
LL3	93.4	105	"	"	"	"	"

Table 2: Superlattice electron transport model parameters

transmission coefficient for electron transport between wells was introduced in the Boltzmann equation. This takes into account both tunneling and thermionic emission. Since the barrier layer thickness is large enough for miniband transport to be negligible, transmission probability is calculated using the Wentzel-Kramer-Brillouin (WKB) approximation. Finally, Fermi-Dirac statistics was used to account for the number of available empty states in the neighboring wells for tunneling and thermionic emission calculations. The only energy level calculated in the well is 30.2meV. Parameters used in the simulations are listed in Table 2, where μ is electron mobility, v_s is the saturation velocity, and α is the conduction band non-parabolicity. The superlattice conduction band diagram at different well dopings was calculated using self-consistent Poisson and Schrodinger equations. This resulted in an effective barrier height that changes with doping as indicated in Table 2. Details of these simulations are described in reference [8].

RESULTS

Experimental

Device resistance-versus-temperature is shown in Figure 5. At low temperatures (< 150K), device resistance is dominated by the superlattice and other contributions can be neglected. In this temperature range, the resistance of the superlattice decreases as well doping increases. This is due to a decreased affect of the barrier as doping is increased. At higher temperatures, the superlattice's affect on electron transport is minimal for all well dopings and the contributions of substrate and contact resistance become significant. This can be seen in the "crossover" of the curves at higher temperatures where substrate resistance and wire-bond placement significantly affect measurements. The resistance of the device of highest well doping (LL4) increases with temperature as in metals and degenerate semiconductors. E_F at this doping is approximately 129.6meV, which is higher than the effective barrier height ($E_b \approx$ 100meV). Device

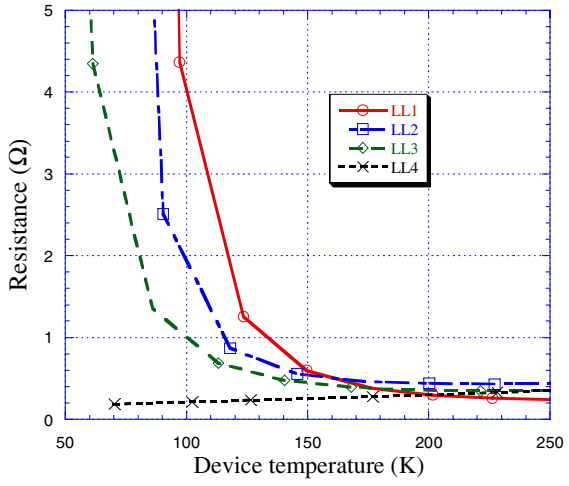

Figure 5: Experimental HIT cooler resistance versus temperature

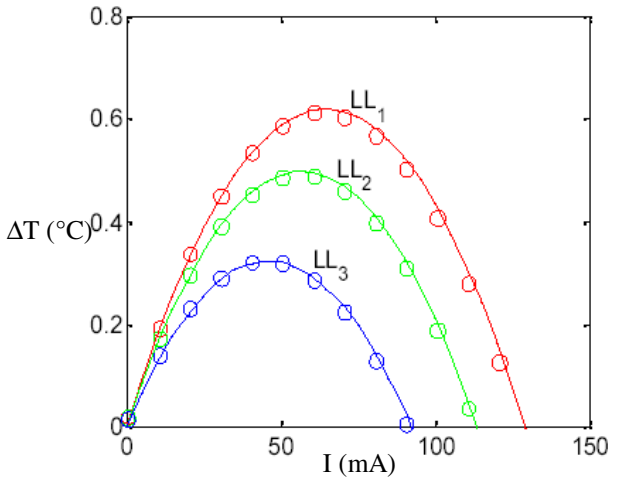

Figure 6: Experimental (circles) and modeled (curves) HIT cooling versus current

	S (μV/K)		σ (Ω^{-1}cm^{-1})			β (W/mK)		
Device	superlattice	substrate	superlattice	bulk	substrate	superlattice	bulk	substrate
LL1	316.01	44.64	22.52	337	167	5	5	68
LL2	286.08	44.64	32.48	595.3	167	5	5	68
LL3	267.97	44.64	40	728	167	5	5	68

Table 3: HIT cooling model device parameters

characteristics at this doping are not presented as the cooling performance was poor. In addition, it was not possible to obtain an accurate value of the superlattice resistance for sample LL4 as it was on the same order as the substrate and lead resistances that were dependent upon the experimental configuration and the location of the anode contact on the substrate. Experimental room-temperature cooling results are presented in Figure 6 above. Maximum cooling decreases as well layer doping is increased. The maximum cooling observed is 0.6°C for the sample of lowest well doping (LL1). A significant limitation of cooling is due to Joule heating of the metal-semiconductor interface at the cathode.

Device modeling

S and σ of the superlattices are calculated at room-temperature using the transport model that predicts device I-V characteristics in a wide temperature range. The values of *S* and σ along with other material properties used in the electro-thermal model of the device are listed in Table 3. An effective 1D model was used to take into account the 3D thermal resistance of the substrate and the Joule heating of and heat conduction through the top metal layer [9]. The modeled cooling versus current results agree well with experimental data as shown in Figure 6 above. The main limitation of device cooling performance is due to heat conduction through the cathode metal contact and Joule heating at the cathode due to metal-semiconductor contact resistance which was assumed to be $3\times10^{-6}\Omega\cdot cm^2$. By removing these two non-ideal factors, cooling can be improved to 3°C as shown in Figure 7.

Thermionic emission in these planar superlattice structures is limited mainly by the conservation of lateral momentum when electrons are transmitted above the barrier. When lateral momentum is not conserved and device non-idealities are removed, cooling as high as approximately 7°C is predicted as shown in Figure 7 [10]. Power factor versus well layer doping

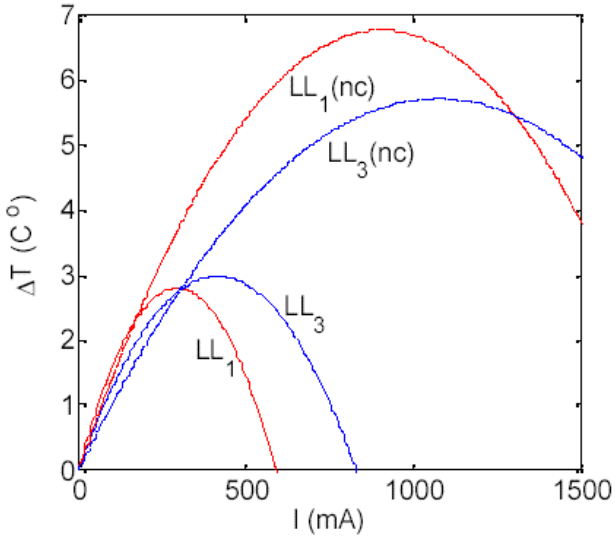

Figure 7: Theoretical HIT cooling curves without non-idealities and when momentum is not conserved

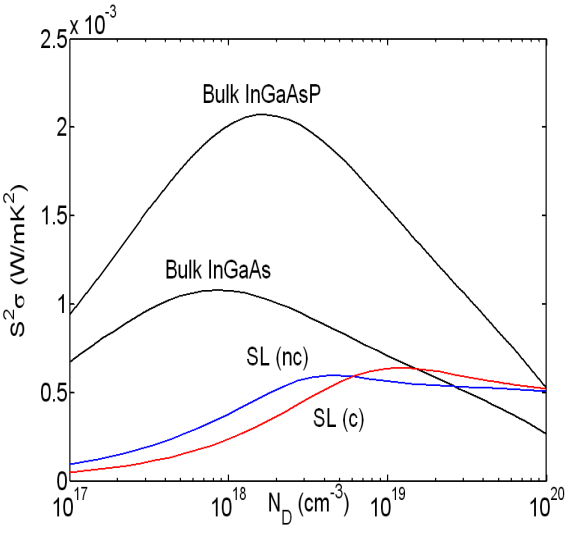

Figure 8: Theoretical power factor vs. doping for bulk material and for InGaAs/InGaAsP superlattice

is calculated in Figure 8 above for bulk materials and for the superlattice (E_b = 90meV) in both cases of conserved and non-conserved momentum. Power factor curves for the case of conserved momentum (as in these planar barrier superlattices) do not agree with room-temperature device cooling performance. In fact, measured cooling decreases while power factor increases for superlattice well dopings between 10^{18}cm^{-3} and 10^{19}cm^{-3}. This is due to the fact that the contact resistance at the cathode dominates over the device resistance. Because the increase of superlattice σ at higher well layer dopings does not significantly affect Joule heating of the cathode at room-temperature, cooling performance is actually higher at lower dopings due to the increase in superlattice *S*. This is reflected in overall device performance which agrees well with modeling.

CONCLUSIONS

HIT microcooler samples consisting of InGaAs/InGaAsP superlattice structures lattice-matched to InP of four different well layer dopant concentrations have been fabricated and analyzed. Low-temperature device I-V measurements were taken from 45K to room-temperature. Room-temperature cooling measurements show that device cooling decreases as well layer doping is increased. The maximum room-temperature device cooling observed is 0.6°C at the lowest superlattice well layer doping. Detailed electron transport equations were used to calculate the electrical characteristics of the superlattice structures. The calculations agree well with experimental data. Electro-thermal models were then used along with models that take into account non-ideal device characteristics such as the thermal resistance of the substrate and Joule heating at the cathode-contact interface to predict device cooling performance at room-temperature. These results also agree well with experimental values. Additional calculations predict that cooling performance will improve to 3°C in the absence of device non-idealities and increase to 7°C when momentum is non-conserved. Therefore, the factors that limit the InP-based HIT microcooler performance are the limitation of device σ due the metal-semiconductor junction at the cathode and the conservation of lateral momentum in the heterostructure. Detailed characterization and modeling have confirmed that the benefit of thermionic emission in superlattices cannot be realized with small barrier structures and that tall barriers (much larger than *kT*) are required to obtain an order of magnitude improvement of ZT [8,10]. This work was supported by DARPA Heretic and the Packard Fellowship.

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