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3D ELECTROTHERMAL SIMULATION OF HETEROSTRUCTURE THIN FILM MICRO-COOLERS

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ABSTRACT

A 3D electrothermal model is used to simulate and optimize Si/SiGe superlattice heterostructure micro-coolers. The model considers thermoelectric/thermionic cooling, heat conduction and Joule heating. It also includes non-ideal effects, such as contact resistance between metal and semiconductor, substrate/heatsink thermal resistance, the side contact resistance. The simulated results match very well with the experimental cooling curves for various device sizes ranging from $60x60\mu m^2$ up to $150x150\mu m^2$. It is found that the key factor limiting maximum cooling is metal-semiconductor contact resistance. The maximum cooling could be doubled if we remove the metal-semiconductor contact resistance.

The thin film Si/SiGe superlattice micro-coolers can provide cooling power density over 500 W/cm^2 as compared with a few W/cm^2 of bulk Bi_2Te_3 themoelectric coolers. This micro-cooler experimentally demonstrated a maximum cooling of 4.5ºC at room temperature and 7ºC of cooling at 100ºC ambient temperature. It is a promising candidate for microprocessor spot cooling.

KEYWORDS

Electrothermal, Si/SiGe superlattice, micro-cooler, heterostructure, thermoelectric/thermionic cooling, modeling, optimization

INTRODUCTION

The ever-increasing integrated circuits (IC) performance has been accompanied by smaller device size higher lever of integration and faster switching frequency (Atluri *et al.* 2003, Viswanath *et al.* 2000, and Chrysler 2002). On-chip cooling and hot spot removal are beyond the capability of the conventional Bi_2Te_3 thermoelectric (TE) coolers, because of their small cooling power density on the order of a few W/cm^2, slow transient response on the order of a few seconds and bulk manufacturing process (Zhang *et al.* 2003). At the same time, conventional bulk Bi_2Te_3 TE coolers require significant electrical power for their operation, which results in a significant heat load as well. Thus there has been a renewed interest in developing high efficiency thermoelectric (TE) materials and micro-coolers for microprocessor spot cooling solutions (Simons and Chu 2000).

We focus our research on Si/SiGe microcoolers because of the relatively easy integration with most microprocessors based on Si materials. Si/SiGe superlattice thin film micro-coolers benefit from thermionic emission in heterostructures. In the thermionic emission process, hot electrons from a cathode layer are selectively emitted over a barrier to the anode junction. Since the energy distribution of emitted electrons is almost exclusively on one side of Femi-energy, when current flows, strong carrier-carrier and carrier-lattice scatterings tend to restore the quasi-equilibrium Femi-distribution in the cathode by absorbing energy from the lattice, thus it cools the emitter junction.

The cooling efficiency of a thermoelectronic cooler could be characterized by the figure-of-merit, ZT, where $ZT = S^2\sigma T/K$ and S is the Seebeck coefficient, σ is the electrical conductivity, T is the cold side temperature and K is the thermal conductivity (Rowe, 1995). There are several ways to increase figure-of-merit (Hikes and Ure, Jr. 1961, Chandari and Rowe 1988, White and Klements 1992, and Hicks and

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Dresslhaus 1993). One widely used technique (Hicks and Dresslhaus 1993) is to create a superlattice structure. A superlattice structure can improve the electron energy distribution during transport and thus increase the Seebeck coefficient, S, and electrical conductivity, σ. Meanwhile, the superlattice also can invoke phonon blocking and density states changing, which results in a reduced thermal conductivity. The increase of $S^2\sigma$ combined with reduced thermal conductivity enhances the figure-of-merit and allows more efficient cooling to be achieved. Experimental results have shown that the maximum cooling temperature increases by a factor of four for the Si/SiGe superlattice micro-coolers as compared with bulk Silicon micro-coolers (Fan *et al.* 2001).

Figure of merit, ZT, is a dimensionless material property. However, experimentally we still find that the cooling is strongly geometry dependent. This is because the cooling of the current device is limited by many non-ideal effects, such as: side contact resistance, substrate resistance, etc. The parasitic Joule heating is also strongly geometry dependent. To understand the impact of geometry, contact resistance, thermal conductivity, and electrical conductivity on device cooling, it is important to build a reliable electrothermal model. Over the past few years several thin film coolers based on InP (LaBounty *et al.* 2000), SiGe (Yang *et al.* 2001 and Zeng *et al.* 1999), SiGeC (Fa *et al.* 2001), polycrystalline silicon (Jacquot *et al.* 2002) and BiTe (Venkatasubramanian *et al.* 2001) have been experimentally demonstrated. There are, however, very few detailed theoretical models available to study the limiting factors of these coolers and to compare them with experimental results. Labounty et al. have shown some preliminary studies of InP-based thin film coolers by using a 3D ANSYS™ finite element model (LaBounty *et al.* 2000 and LaBounty *et al.* 2001). Vashaee et al. (2001) analyzed SiGe thin-film microcoolers using a 1D effective model in order to address some of the optimization issues. With complicated 3D device geometry, it is very useful to have a 3D electrothermal model that takes into account all of the limiting factors.

NOMENCLATURE

- S: Seebeck Coefficient, V/K
- T: Temperature, K
- K: Thermal conductance, W/K
- β: Thermal conductivity, W/mK
- R: Electrical resistance, ohm
- I: Supplied current, A
- Q: Cooling Power, W

EXPERIMENTAL

a. Sample Preparation

Microcooler samples consisted of a 3µm thick superlattice layer with the structure of 200 × (3nm Si/12nm $Si_{0.75}Ge_{0.25}$) and doping concentration of 5e19cm^{-3}, a 1µm $Si_{0.8}Ge_{0.2}$ buffer layer with the same doping concentration as the superlattice; and a 0.3µm $Si_{0.8}Ge_{0.2}$ cap layer with doping concentration of 1.9e20 cm^{-3}. The most important part of the device is the superlattice layer. In addition to thermionic emission, it can also reduce the thermal conductivity to prevent the backflow of heat from substrate to cold junction. The buffer layer on top of the Si substrate was included in order to reduce strain due to lattice mismatch between the substrate and the superlattice. The cap layer with higher doping concentration was included in order to improve the ohmic contact between the metal and semiconductor. The samples were grown with a molecular beam epitaxy (MBE) machine on five inch diameter (001)-oriented Si substrates, p-type doped to 0.003 ~ 0.007 Ω-cm with Boron. A Ti/Al/Ti/Au layer was evaporated on top of the samples for electrical contact.

Figure 1a shows commercial bulk thermoelectric Bi2Te3 coolers as compared with a dime; Figure 1b shows the picture of Si/SiGe superlattice microcooler as compared with a nickel. From these two pictures, it is clear that the size of our thin film superlattice micro-cooler is orders of magnitudes smaller than the bulk thermoelectric coolers. Figure 1c shows a scanning electron microscopic (SEM) picture of micro-cooler devices with different device size ranging from 60x60μm^2 to 150x150μm^2.

b. Cooling Characterization -- Temperature measurements

The cooling of the devices was measured by standard E-type micro-thermocouple with a tip size of 50µm. The ILX Lightwave LDX3220 current source was used to supply the stable current to the cooler through probes. The thermocouple tips were placed on top of the sample and the substrate. HP 34420A Nanovoltage/microohm meter was used to measure the voltage difference between the two-thermocouple tips. A LabView™ program was developed to automatically control measurements and convert the voltage difference to temperature using temperature calibration data offered by the manufacturer. A schematic drawing of experimental set-up is illustrated in Figure 2.

DEVICE MODELING

We developed a 3D electrothermal model by using ANSYS™ software, a widely used finite element analysis software package (ANSYS Corp. 2003). Figure 3 shows a finite element model of micro-cooler device. The meshing of the device was challenging because of the incompatible geometry: a large substrate as compared with the small superlattice layers.

In this cooler model, there are two sources of cooling at both metal-superlattice and superlattice-substrate junctions because of the different Seebeck coefficients, S, over the junctions. The cooling power could be expressed by $\Delta Q = (S1 - S2) \cdot T \cdot I$, where S1, S2 are the effective Seebeck coefficients for materials on the two sides of the junctions: for the metal-superlattice interface, $S1=S_{metal}$, $S2=S_{superlattice}$; for superlattice-substrate interface, $S1=S_{superlattice}$, $S2=S_{si}$. T is the ambient temperature and I the supplied current. In the case of 1D thermoelectric elements with inclusion of Joule heating and heat conduction, the total cooling power is expressed as:

$$\Delta Q = (S1 - S2) \cdot T \cdot I - \frac{1}{2} I^2 R - K \cdot \Delta T$$ where, R is the element resistance, K is its thermal conductivity, and ΔT is the generated temperature difference. In a 3D device geometry, the electrical resistance, R and thermal conductivity K will be hard to calculate because of the three-dimensional heat and current spreading. In our ANSYS™ model, bulk Joule heating and heat conduction are automatically calculated by solving current continuity and heat conduction equations and the thermoelectric cooling/heating is added as an interface effect.

Results and Discussions

In order to verify some material parameters of the micro-coolers and test the methodology of this model, a simple Si-substrate with exactly the same geometry as the superlattice devices was fabricated and characterized. This sample consisted of only a metal pad deposited on a piece of silicon and therefore exhibits no thermionic emission process but a thermoelectric effect at the metal-Si interface only. Figure 4 shows the device geometry (a) and compares the experimental results (b) with the simulated results (c). For the Si micro-cooler, the optimized device size is 40x40μm^2, it could achieve about 1ºC cooling with the supplied 200mA current. For a device size larger than 50x50μm^2, the cooling will be less than 0.8ºC. The Silicon has a low thermoelectric figure-of-merit.

Table 1 Material parameters for Silicon micro-cooler

Thermal Conductivity				
Unit	Metal layer	SiNx	Si Substrate	Contact layer
W/mK	31.9	1	125	125
Resistivity				
Ohm-cm	1.00E-05	1000	0.003	0.1

The material parameters listed in Table 1 for Si micro-cooler are either experimentally measured or from the literature. The Seebeck coefficient of metal is ~ 0 and the Seebeck coefficient of bulk Si is 325 μV/K, obtained from literature value according to the doping concentration (Geballe and Hull 1955). The metal-semiconductor contact resistance is 1e-6 ohm-cm^2, which has been included in the contact layer. It is interesting to find that the metal thermal conductivity is only about one-fifth of the bulk gold value. The reason is that the evaporated metal contact is gold alloy, Ti/Al/Ti/Au, and with very thin layers, electrical and thermal conduction are different from pure bulk gold material.

Table 2 Materials parameters for Si/SiGe superlattice micro-cooler

Thermal Conductivity						
Unit	Metal layer	SiNx	Si Substrate	Buffer layer	SL Layer	Cap Layer
W/mK	200	1	125	6.5	6.5	8
Resistivity						
Ohm-cm	1.00e-06	1000	0.003	0.0016	0.0016	0.02

(Notes: The buffer layer was used to lattice match between the Silicon substrate and Si/SiGe superlattice, which is only 1μm in thickness and has the same doping as superlattice layer. To simplify the simulation geometry, the buffer layer was treated as the superlattice layer. The cap layer was a highly doped SiGe alloy layer, used to achieve better metal-semiconductor contact. It was only 0.3μm and also treated as part of the superlattice structure. The superlattice thermal conductivity is in the cross-plane direction.)

After we achieved a successful model for the Si micro-coolers, we only need to add the buffer layer and superlattice layer to the previous model. Table 2 lists material parameters for Si/SiGe superlattice micro-coolers. In the micro-cooler geometry, the temperature gradient is perpendicular to the superlattice, thus the superlattice thermal conductivity is referred to as the cross-plan value. It was measured by the 3ω method with variable width heaters by our collaborators at UC Berkeley (Huxtable *et al.* 2002). The effective Seebeck coefficient of the superlattice was 200μv/K, which was experimentally measured by integrating a thin film heater on top the cooler device. The thin film heater could create temperature difference between the substrate and top of the superlattice layer, thus Seebeck coefficient could be measured: $S = \frac{\Delta V}{\Delta T}$ (Zhang *et al.* 2002). The metal-semiconductor contact resistance is 6e-7 ohm-cm^2, which was included in the cap layer. The contact resistance between metal and semiconductor varies from one device to another and is mainly dependent on the cleanliness of the sample surface and processing conditions.

Figure 5 illustrates the 3D electrothermal model of Si/SiGe hetersostructure micro-cooler device (a), the simulated cooling curve versus supplied current (b) and the experimental results (c). With the Si/SiGe superlattice structure, the cooling was significantly improved as compared to the bulk Si micro-cooler. The optimized geometry device size 60x60μm^2 could achieve the maximum cooling of 4.5ºC at 600mA with a cooling power density of ~600W/cm^2. Even the larger cooler sizes (e.g., the 100x100 μm^2 and 150x150 μm^2 devices whose cooling were too small to be observed for bulk Si device) could achieve 3.5ºC and 2.5ºC cooling, respectively. From the cooling curves, we could see that the current 3D electrothermal model had considered all the major non-ideal factors of the real device; such as: contact resistance between metal and semiconductor, substrate thermal resistance, side contacts etc. Thus it shows a good match between the simulations and experiments for all size devices and can be used for further device optimizations.

Figure 6(a) illustrates the 3D temperature contour plot of a 70x70μm^2 device. With the supplied 0.6mA current, the device could achieve ~4ºC cooling. From the figure, we see that the cooling is localized at the micro-cooler region. This agrees with thermo-reflectance images, as shown in Figure 6(b).

Figure 7 illustrates the electrical potential distribution of Si/SiGe superlattice micro-cooler devices for a bias of 0.18V (I=0.6A). We see the equi-potential on top of the metal contact surface, and it drops radically into the substrate. This figure could be used to verify the correct current injection in the model.

It was predicted that the main constraints of the micro-cooler device resided on the parasitic metal-semiconductor contact resistance (Vashaee *et al.* 2001). Thus, we removed this contact resistance in our 3D electrothermal model and determined that the maximum cooling could be doubled, as shown in Figure 8. For the device size 60x60μm^2, the maximum cooling could reach over 9ºC at room temperature without contact resistance.

CONCLUSION/FUTURE WORK

A 3D electrothermal model was developed for Si and Si/SiGe superlattice micro-coolers. The simulated results of this model compare well with experimental results for all-size devices. The bottleneck that limits the cooling obtained from current devices was found to be the metal-semiconductor contact resistance. If the parasitic contact resistance could be removed, the maximum cooling could reach over 9ºC at room temperature. Other non-ideal factors such as side contact and a non-ideal heat sink (substrate thermal resistance and Joule heating from substrate) will be further investigated to see how they affect the device cooling. This information will help to optimize the Si/SiGe superlattice micro-cooler devices, and allow them to be integrated within integrated circuits.

ACKNOWLEDGMENTS

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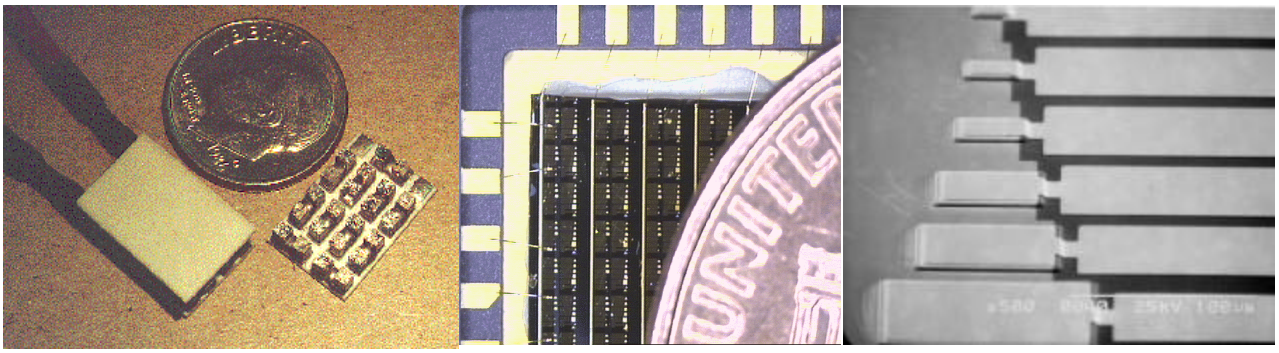


(a) (b) (c)

Figure 1 (a) Conventional bulk Bi_2Te_3 thermoelectronic coolers as compared with a dime

(b) HIT microcoolers as compared with a Penny (c) Scanning Electron Microscopic (SEM) picture of Heterostructure Integerated Thermonic (HIT) micro-coolers

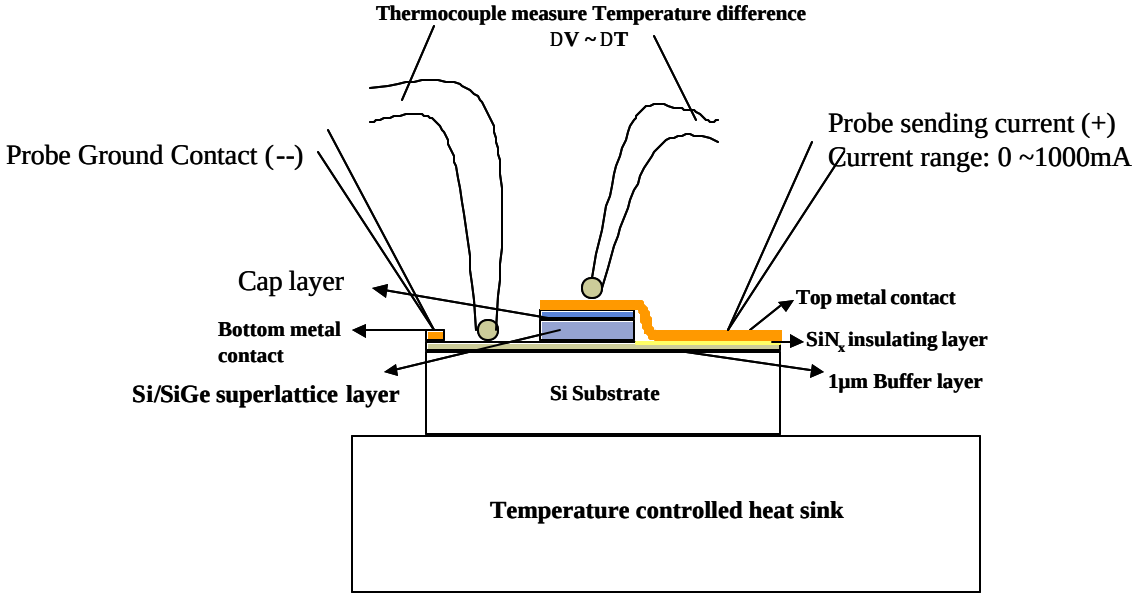


Figure 2 Micro-cooler cooling temperature characterization by thermocouple measurements

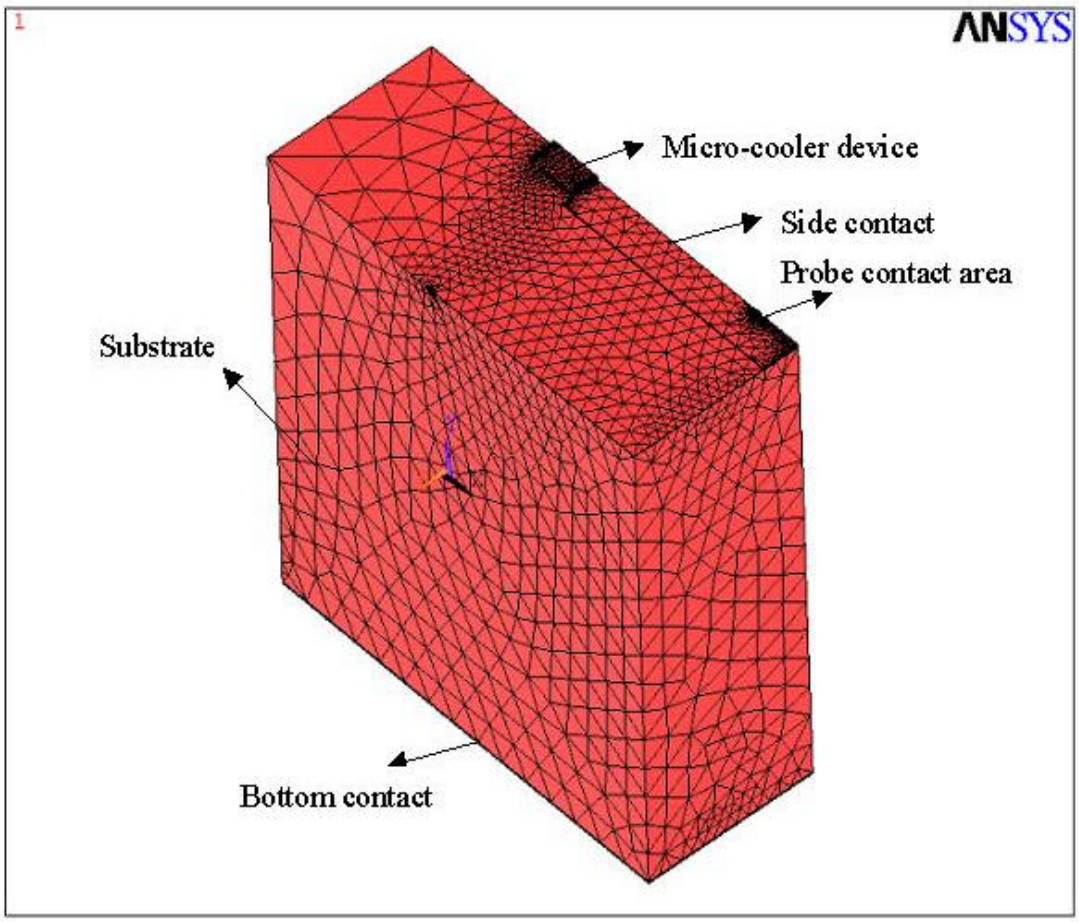
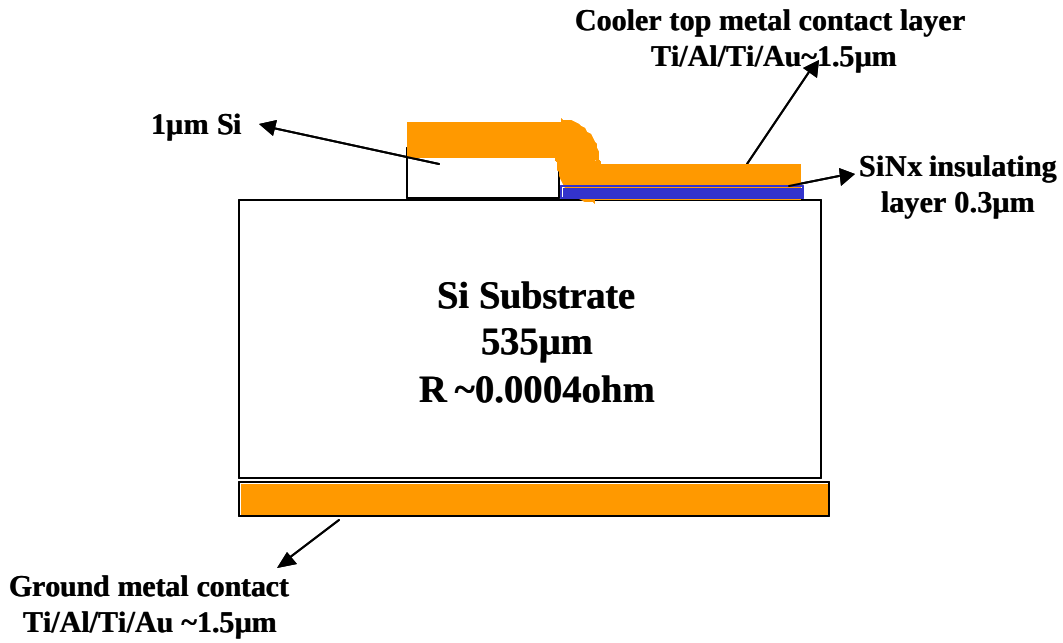
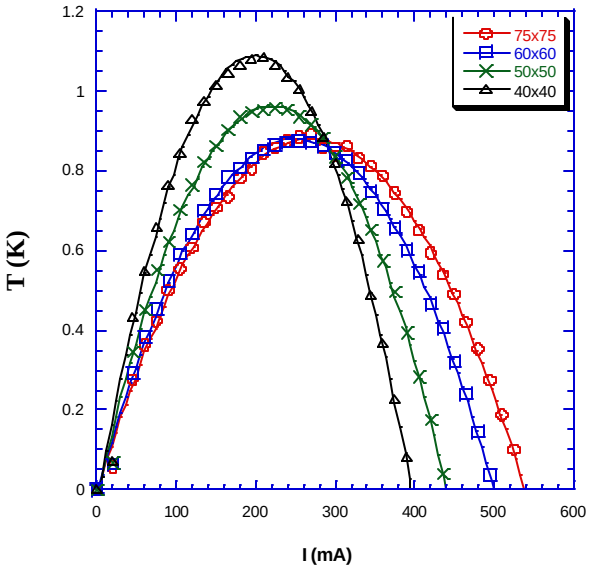


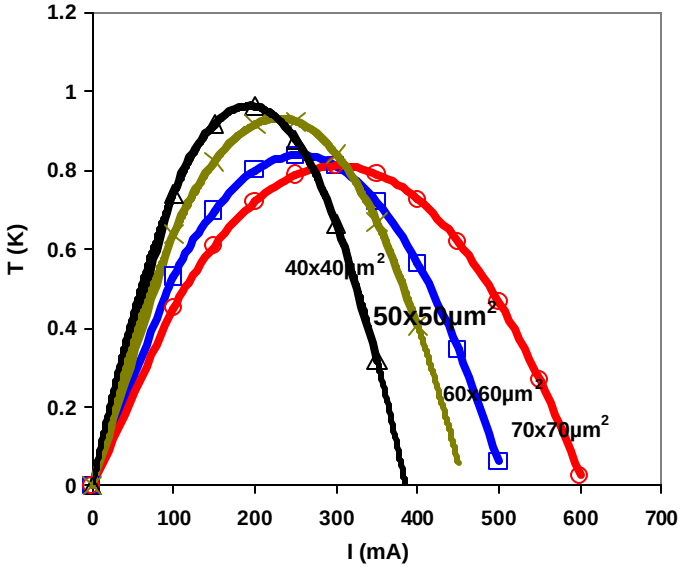
Figure 3 A finite element model of micro-cooler device



a) Silicon single leg thermoelectric cooler model

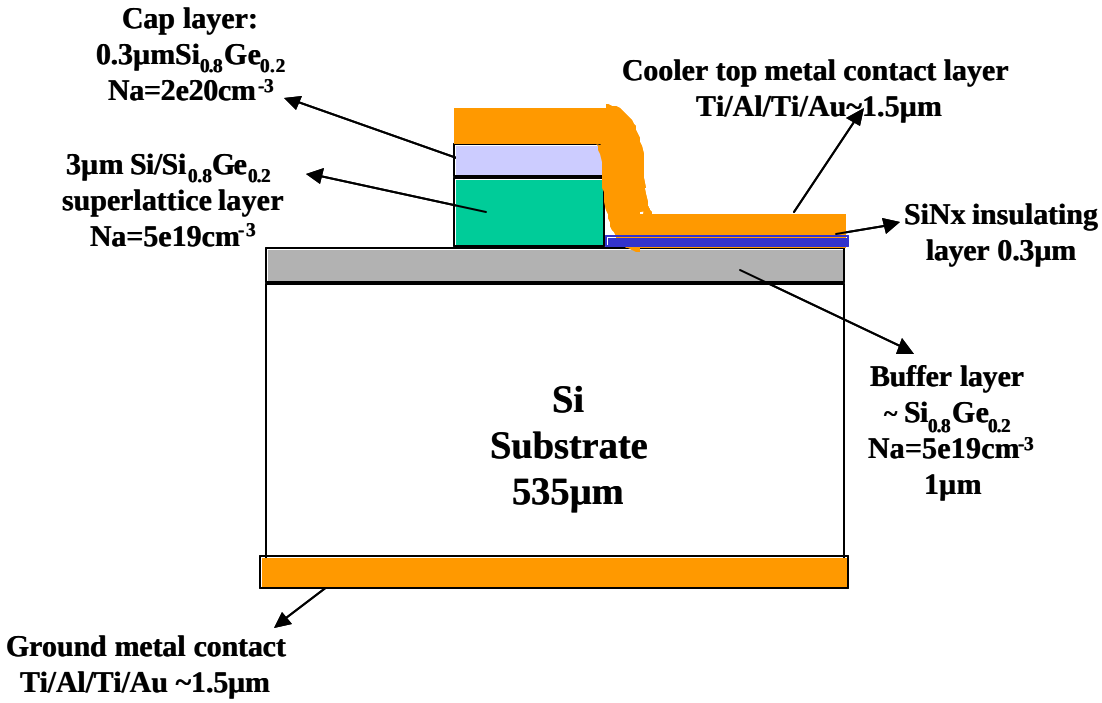


b) Si micro-cooler measurement results

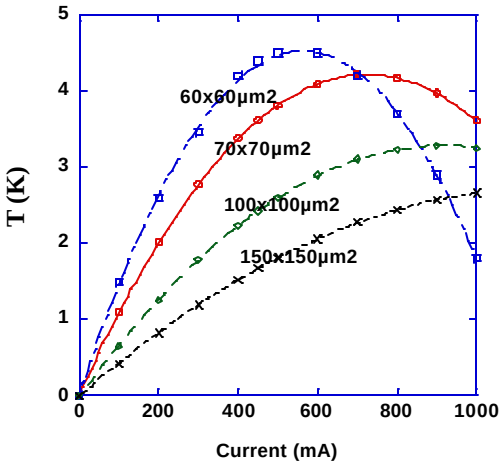


c) Si micro-cooler simulated results

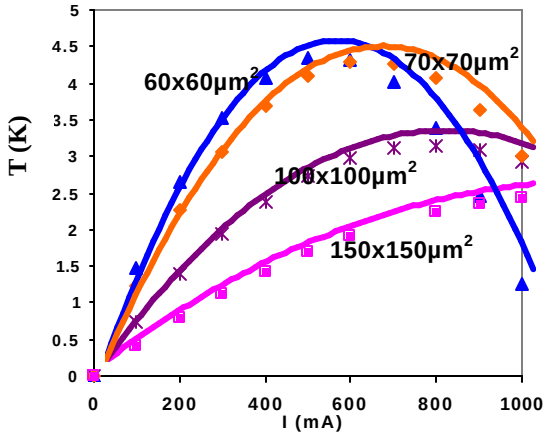
Figure 4 Bulk Silicon micro-cooler a) 3D electrothermal simulation model; b) experimentally measured cooling versus current results; c) Simulated cooling curve versus supplied temperature



a) P-type Si/SiGe superlattice micro-coolers simulation model



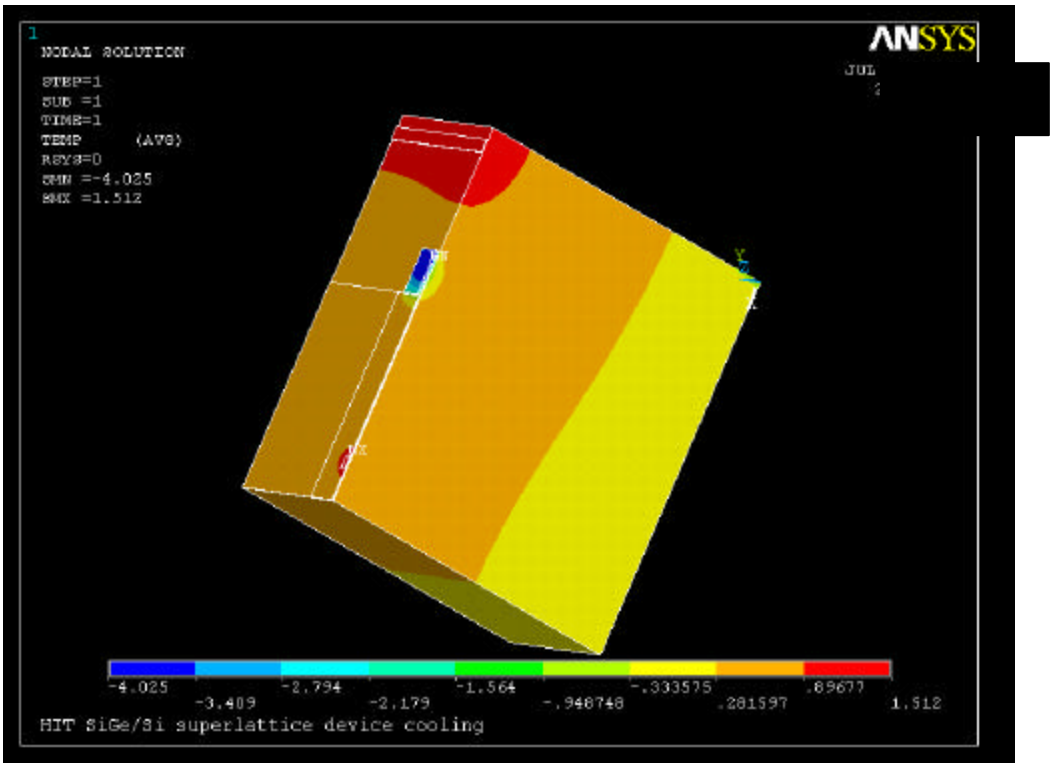
b) Experimental Results



c) Simulated results

Figure 5 P-type Si/SiGe superlattice micro-cooler a) 3D electrothermal simulation model; b) experimentally measured cooling versus current results; c) Simulated cooling curve versus supplied temperature

a



b

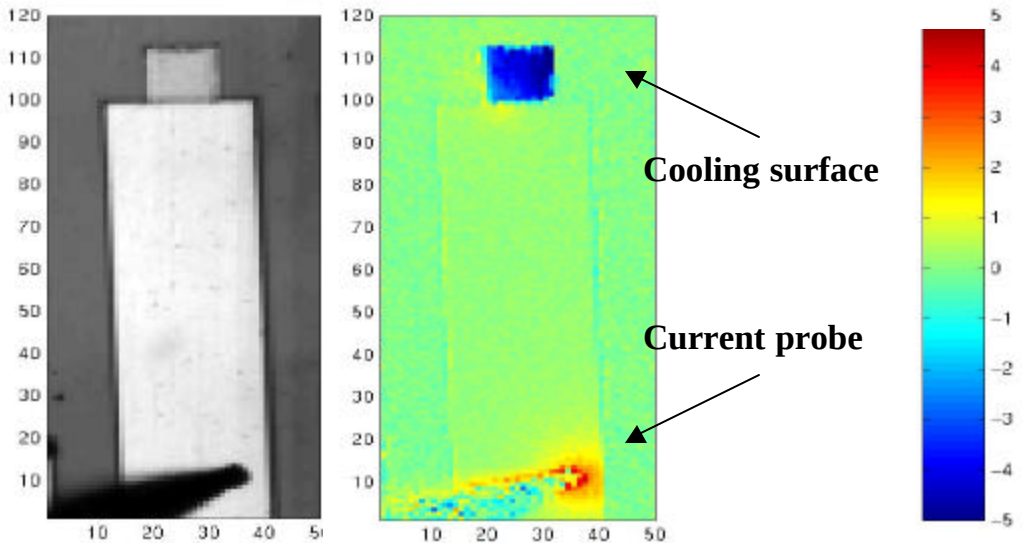


Figure 6 a) Temperature contour plot of an operating micro-cooler. b) Top-side Thermoreflectance image of Si/SiGe micro-cooler

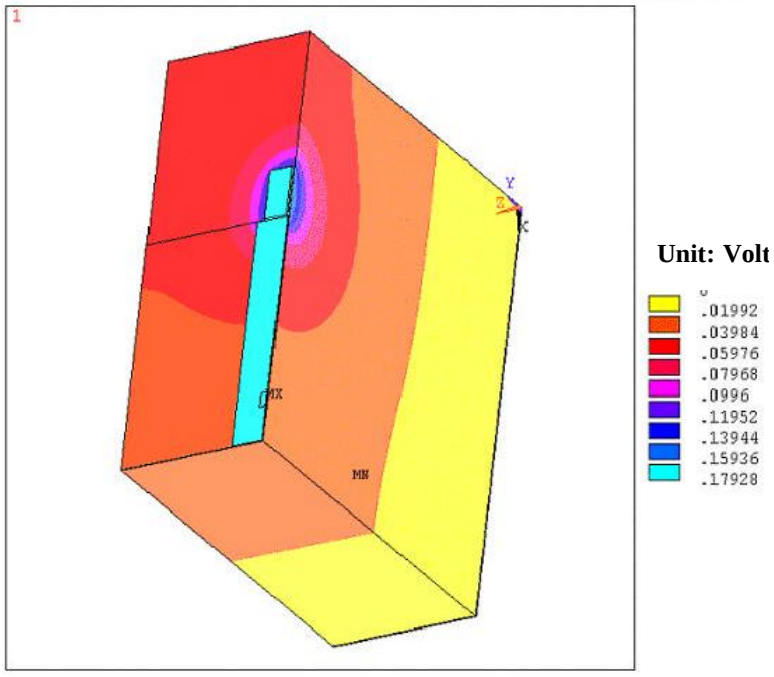


Figure 7 Potential distribution of an operating Si/SiGe superlattice micro-cooler

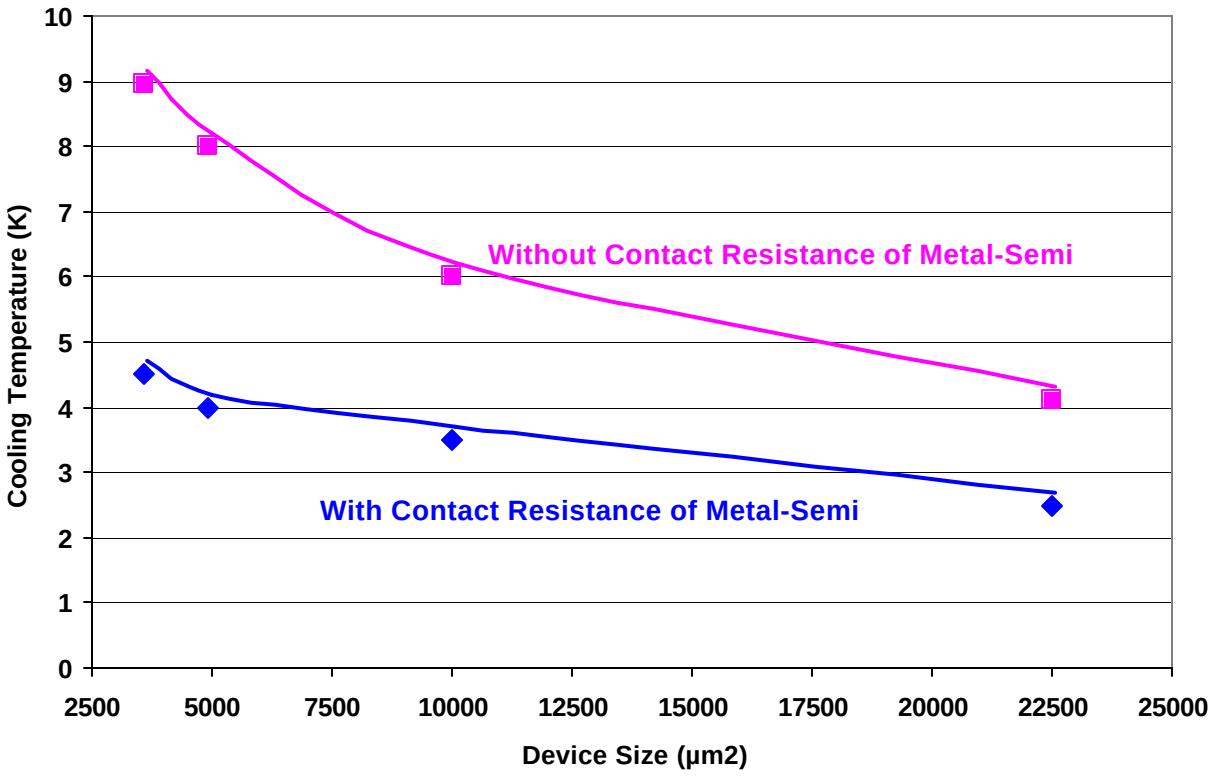


Figure 8 Maximum cooling comparisons for Si/SiGe micro-cooler with metal-semiconductor contact resistance (1e-6 ohmcm2) and without parasitic metal-semiconductor contact resistance. (Size ranging from 60x60μm^2 ~150x150μm^2)