SYNOPSYS®

DATASHEET

Sentaurus TCAD

Industry Standard Process and Device Simulators

Key Applications: CMOS, FinFET, Memory, Power Devices, RF Devices, Optoelectronics, BEoL Reliability

Overview

Sentaurus™ is a suite of TCAD tools that simulate semiconductor device fabrication, operation, and reliability. The Sentaurus simulators use physical models to represent the wafer fabrication steps and device operation, allowing for the exploration and optimization of new semiconductor devices.

The Sentaurus TCAD tools work seamlessly and can be combined into complete simulation flows in 2-D and 3-D, and supports silicon and compound semiconductor technologies, covering a broad range of semiconductor applications.

Value of Sentaurus TCAD in Technology Development and Optimization

Semiconductor manufacturers face the challenge of developing process technologies within strict time and cost constraints. One key factor impacting development time and cost is the number of engineering wafers needed to complete the development of the new process. By simulating the process flow and device operation before any wafers are processed and during wafer-based process optimization, TCAD reduces the number of engineering wafers, saving time and money. Moreover, Sentaurus TCAD simulations provide engineers with important insights into the behavior of semiconductor devices which can lead to new device concepts.

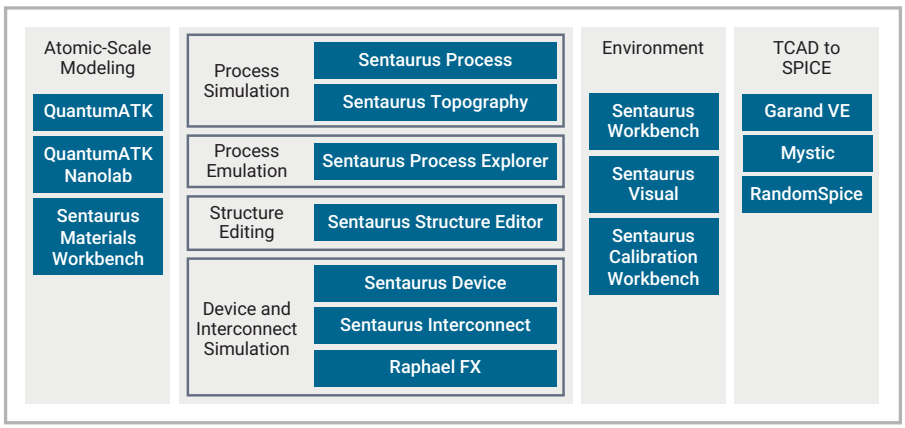

Figure 1: Sentaurus™ TCAD Family

Atomic-Scale Modeling

QuantumATK® simulates the properties and transport mechanisms of novel materials and device structures, enabling the down-selection of promising materials for further exploration and the TCAD-level simulation of advanced devices before wafer-based data is available. Sentaurus Materials Workbench provides a link between QuantumATK output and TCAD models implemented in Sentaurus simulators.

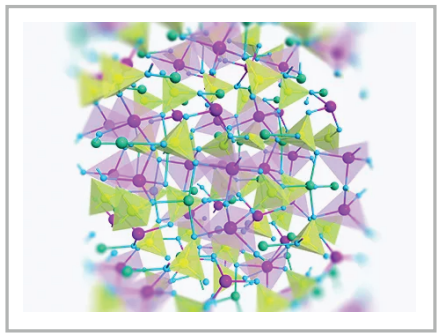

Figure 2: Atomistic Simulation with QuantumATK

Process Simulation Solutions

Sentaurus Process is a process simulator that simulates the fabrication steps in silicon process technologies in 2-D and 3-D. Equipped with a set of advanced process models, which include default parameters calibrated with data from equipment vendors, Sentaurus Process provides a predictive framework to simulate a broad spectrum of technologies, ranging from nanoscale CMOS to high-voltage power devices.

With Sentaurus Process, users can easily simulate process modules and integrate them into the complete front end of the line (FEoL) process flows. An advanced set of oxidation, diffusion, implantation, and mechanics models, combined with robust mesh generation and structure-editing capabilities, cover important process modules such as ultra-shallow junction formation, high-kl metal gate, and strained silicon. A choice of advanced implantation and diffusion models are available in Sentaurus Process.

To handle these process conditions, Sentaurus Process includes a five-stream diffusion model as well as models for {311} defects, small interstitial clusters (SMICs), dopant-defect clusters, and transient dopant activation.

Sentaurus Process also offers a kinetic Monte Carlo (KMC) simulator for atomistic simulations of the interactions of dopants with point defects and extended defects in silicon.

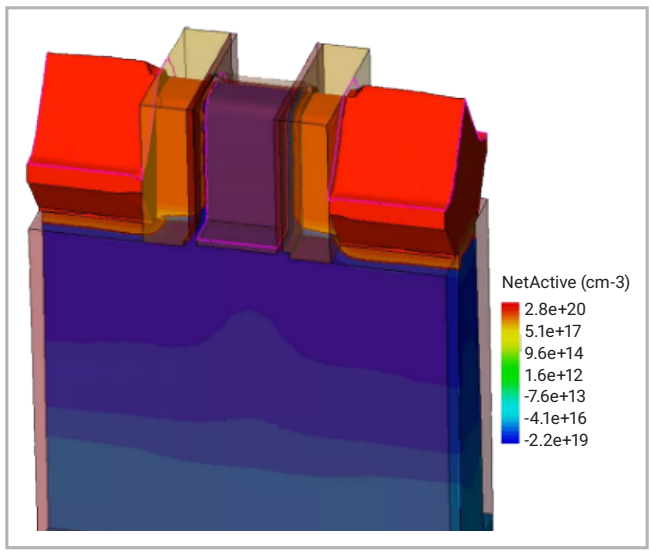

Figure 3: FinFET device created with Sentaurus Process

Sentaurus Topography is a physical topography simulator that simulates topography modifying process steps such as deposition, etching, spin-on glass, reflow, and chemical-mechanical polishing in 2-D and 3-D.

Sentaurus Topography includes models for Physical vapor deposition (PVD), Chemical vapor deposition (CVD), Plasma-enhanced chemical vapor deposition (PECVD), Low-pressure chemical vapor deposition (LPCVD), High-density plasma (HDP) deposition, Atmospheric pressure chemical vapor deposition (APCVD), and Spin coating and reflow.

Etching processes that can also be simulated in Sentaurus Topography include Wet etch, Hemispherical etch, Reactive ion etch (RIE), Ion-enhanced etch, Ion milling, High-density plasma (HDP) etching, and Chemical- mechanical polishing (CMP).

In addition, the interface between Sentaurus Topography and Sentaurus Process allows users to combine front-end thermal and topography simulations in one environment.

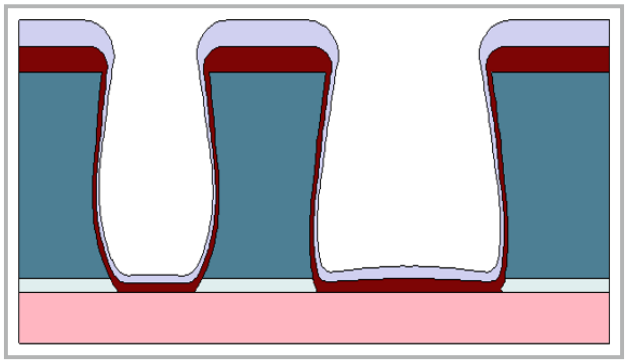

Figure 4: Physical vapor deposition (PVD) model with Sentaurus Topography

Process Emulation Solution

Sentaurus Process Explorer is a fast 3D process emulator used to identify and correct process integration issues during technology development. Sentaurus Process Explorer produces highly realistic 3D representations of process structures using GDSII mask data and a process recipe as input.

Sentaurus Process Explorer is linked to the Synopsys TCAD simulators, such as Raphael FX, to enable the high accuracy RC extraction in Design Technology Co-Optimization (DTCO) applications, an area where deposition process complexities are required but often with limited budget resources.

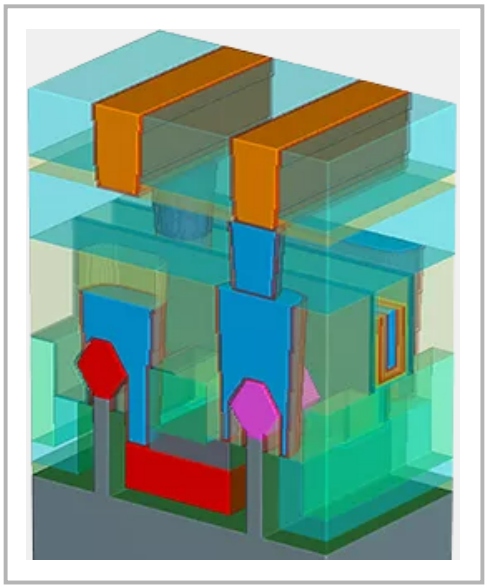

Figure 5: Sample process structure with Sentaurus Process Explorer

Structure Editing Solution

Sentaurus Structure Editor is a device structure editor used to create structures for device simulation when process simulation is not required. Sentaurus Structure Editor uses geometric primitives powered by the ACIS® geometry kernel to render complex device shapes. A graphical user interface serves as the front end for mesh generation engines available in Sentaurus Process and Sentaurus Device. The Sentaurus Structure Editor command language recreates the device structure in batch mode as part of a simulation flow.

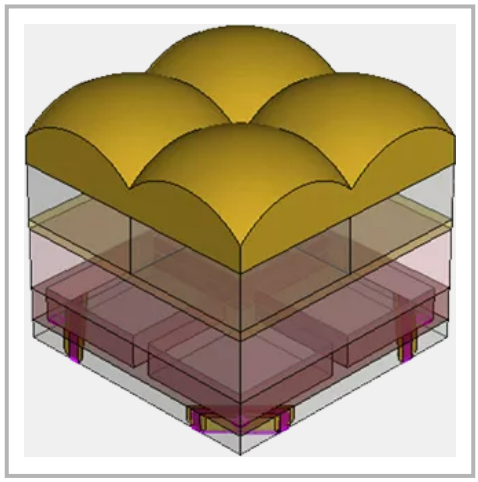

Figure 6: CIS device created with Sentaurus Structure Editor

Device and Interconnect Simulation Solutions

Sentaurus Device is a semiconductor device simulator that simulates the electrical, thermal, and optical characteristics of silicon and compound semiconductor devices in 2-D and 3-D. Sentaurus Device supports the design and optimization of current and future semiconductor technologies including nanoscale CMOS, FinFET, thin film transistors (TFTs), flash memory, SiGe heterojunction bipolar transistors (HBTs), large-scale power devices, compound semiconductors, CMOS image sensors, and solar cells. In addition, Sentaurus Device enables the analysis of complex integrated circuit phenomena such as electrostatic discharge, latch- up, and single-event upset.

Sentaurus Device has an extensive set of models and parameters to support compound semiconductor device development, including spatially varying mole fractions, heterointerfaces, bulk and surface trapping, polarization effects in GaN, anisotropic effects in SiC, and spatial quantization in 2-D electron gases. In addition, proprietary models can be implemented with a flexible physical model interface (PMI).

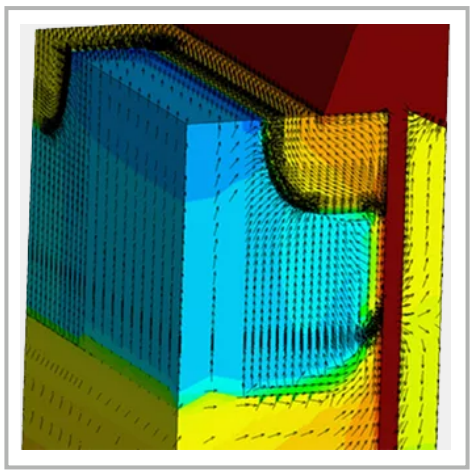

Figure 7: Electric Field lines in a FET using Sentaurus Device

Sentaurus Interconnect is a Back-End-of-Line reliability simulator that performs simulation jobs across a computer network. Sentaurus Interconnect simulates physical phenomena concerned with back-end-of-line (BEoL) reliability. It comprises capabilities for simulating delamination, crack propagation, and other reliability issues related to mechanical stress, Joule heating, electromigration, and stress migration.

Sentaurus Interconnect is designed specifically for semiconductor applications, featuring an easy-to-use GDSII interface, full stress history, support for common BEol semiconductor materials and global-local sub modeling to support chip-packaging interactions (CPI).

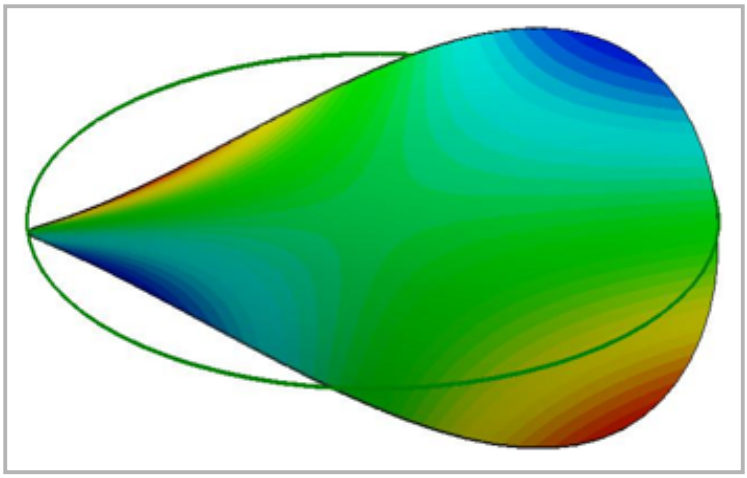

Figure 8: Wafer warpage analysis with Sentaurus Interconnect

Raphael™ FX is the gold-standard field solver for resistance and capacitance extraction, designed to simulate the electrical and thermal effects of today's complex on-chip interconnect. Through Raphael's easy-to-use graphical user interface (GUI), process technology data are entered, and the interconnect structures are automatically generated and characterized for capacitance.

An alternative simulation flow allows the generation of structures from mask (GDSII) and interconnect technology format (ITF) files. Raphael includes support for conformal dielectrics, trapezoidal conductors, and other advanced process effects.

Raphael can also extract resistance and capacitance on structures generated with Sentaurus Structure Editor and Sentaurus Interconnect.

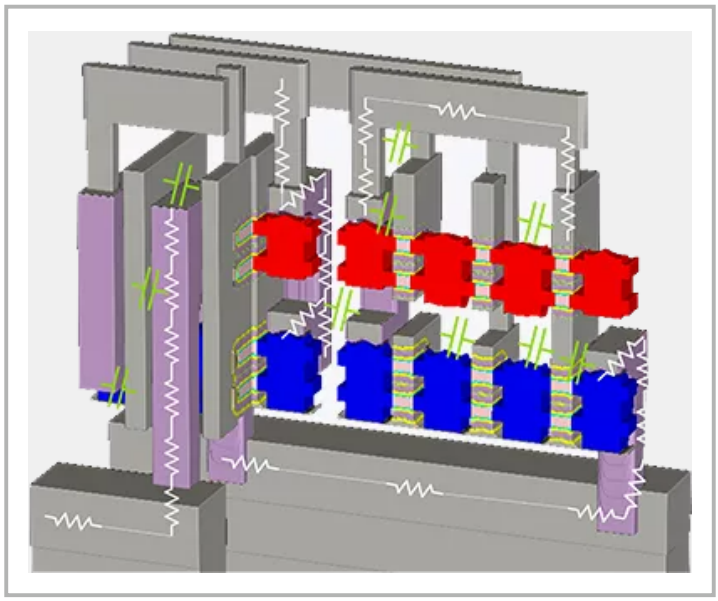

Figure 9: Interconnect structures with Rafael FX

Environment Solutions

Sentaurus Workbench is based on the TCAD framework. It is a complete graphical environment for creating, managing, executing, and analyzing TCAD simulations. Its intuitive graphical user interface allows users to navigate and automate the typical tasks associated with running TCAD simulations such as managing the information flow, including preprocessing of user input files, parameterizing projects, setting up and executing tool instances, and visualizing results with appropriate viewers.

With Sentaurus Workbench, users can automatically generate design-of experiments splits and can distribute simulation jobs across a computer network.

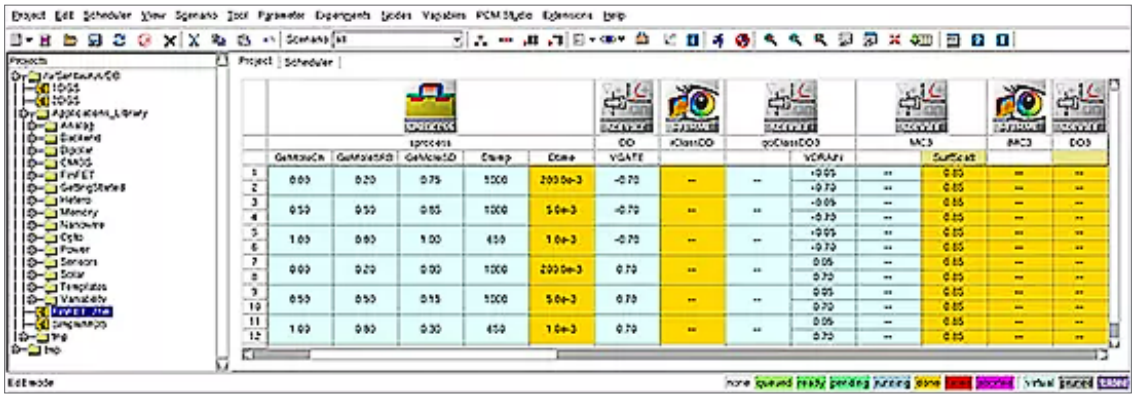

Figure 10: Sentaurus Workbench user-friendly GUI

Sentaurus Visual provides users with a state-of-the-art interactive 1-D, 2-D, and 3-D visualization and data exploration environment. Sentaurus Visual supports TCL scripting, enabling the postprocessing of output data to generate new curves and extracted parameters.

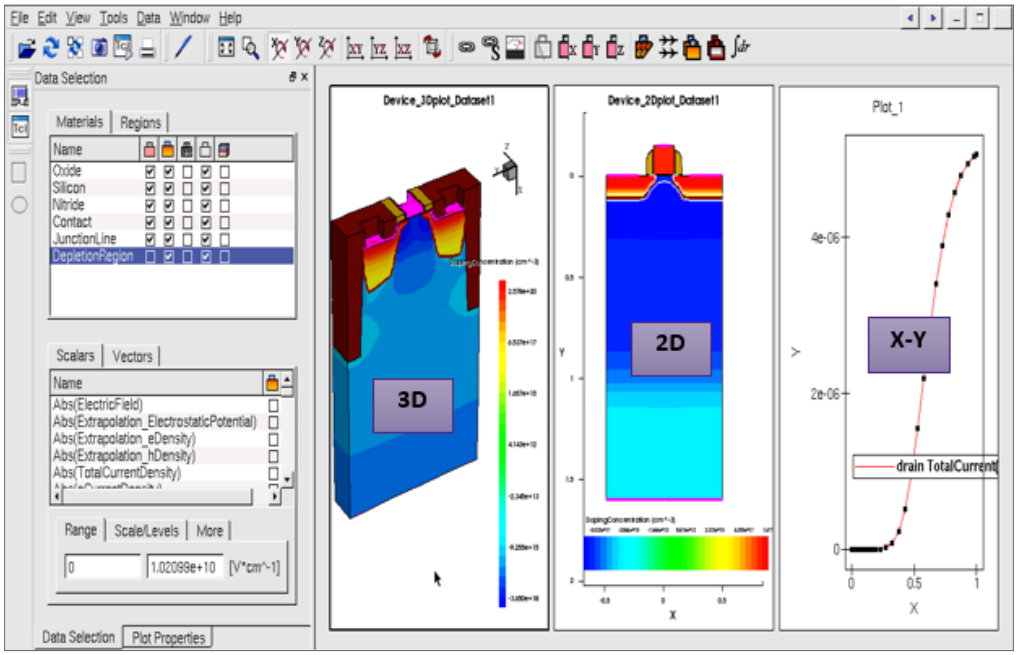

Figure 11: Sentaurus Visual TCAD data visualizer GUI

Sentaurus Calibration Workbench is built for automated workflow-oriented calibration of TCAD models, based on innovative machine learning (ML) capabilities. It is designed to leverage TCAD technology to the next level by enabling users to calibrate process and device simulation models rapidly and systematically for maximum accuracy and predictivity, and thus, reduce the need for expensive experimental wafers in the technology/device development and optimization phases.

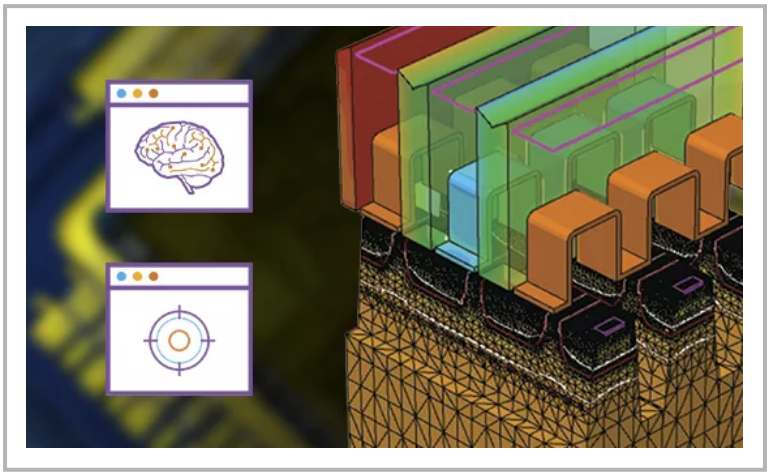

Figure 12: Structure created using Sentaurus Calibration Workbench with ML capabilities

TCAD-to-SPICE Solution

SPICE Model Extraction Mystic extracts compact model parameters (standard SPICE models, macro models, Verilog-A models) from Sentaurus TCAD output, enabling technology development and DTCO teams to simulate the impact of new transistor designs using circuit-level metrics before wafers are available. The TCAD-to-SPICE flow also supports the simulation of the impact of process variability at the circuit-level through the extraction of variation-aware compact models using the variability engine Garand VE and the model card generator RandomSpice.

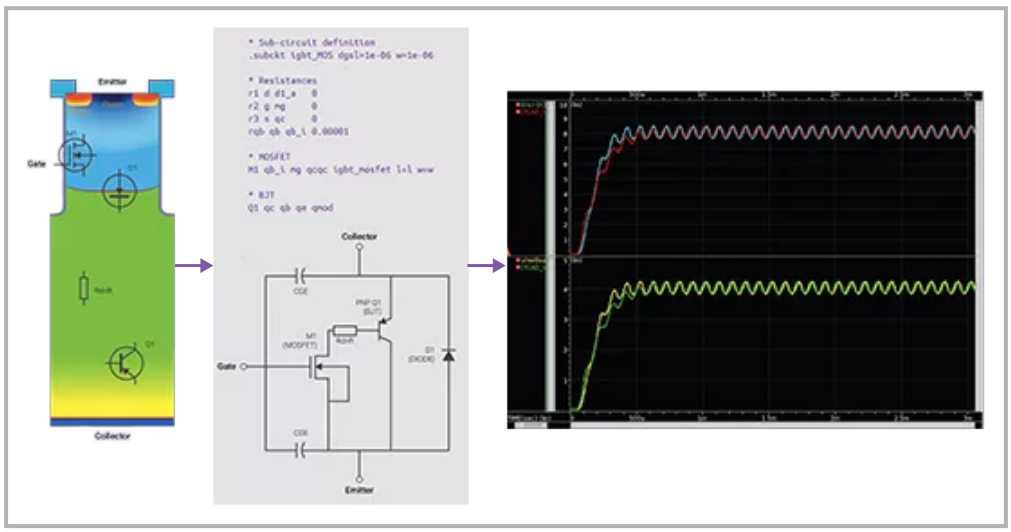

Figure 13: TCAD-To-SPICE Sub-Flow extracts SPICE Model from TCAD before wafers are available

For more information about Sentaurus products and other Synopsys TCAD solutions, please goto www.synopsys.com/tcad, or contact your local Synopsys representative or email tcad_team@synopsys.com