An Ambipolar Virtual-Source-Based Charge-Current Compact Model for Graphene Field-Effect Transistors

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Contents

1 Package Contents

The package for ambipolar virtual source (AVS) model version 1.0.0 for graphene field-effect transistors (GFETs) contains the following files:

Component	Associated Files	Comments
MATLAB	avs_1_0_0.m; extract_main.m; optimize_data.m; model_exerciser.m	MATLAB-related files contain model file, extraction routine, and model exerciser.
Verilog-A	avs_1_0_0.va; dc_gfet.scs; tran_freq_doubler_single.scs; tran_freq_doubler_diff.scs; pac_freq_doubler_single.scs; pac_freq_doubler_diff.scs	Verilog-A related files include the model file and SPECTRE test-benches for simulating the dc response of the GFET and frequency doublers implemented with GFETs.
Experimental data-set	Epitaxial GFET output data from IBM with gate lengths of 650 nm, 300 nm, and 140 nm.	Both output and transfer curve data can be included; however, data must be formatted carefully as explained in Section 5.
Model documentation	PDF file	Must explain the physics of the model and parameter extraction, show basic simulation results, and include appropriate references.

2 Terminals and Voltage Definitions

Figure 1 shows a GFET with its terminal voltages labeled as **d** (drain), **g** (gate), and **s** (source). The internal and external gate terminals are the same, while the internal drain and source terminals are labeled as **di** and **si**, respectively. Also labeled are the source and the drain channel-access resistances as **Rs** and **Rd**, respectively.

2.1 Voltage definitions

Vds = abs(Vd-Vs)
Vgs = max(Vg-Vs, Vg-Vd)
Vgd = min(Vg-Vs, Vg-Vd)

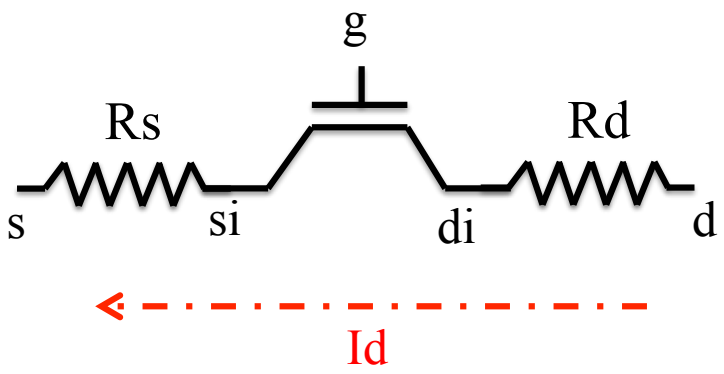

Figure 1: Schematic of the GFET with various terminals labeled. The current in the channel is labeled as Id. Id is positive when it flows from d to s terminal, while it is negative when it flows from s to d terminal.

Vdsi = abs(Vdi-Vsi)
Vgsi = max(Vg-Vsi, Vg-Vdi)
Vgdi = min(Vg-Vsi, Vg-Vdi)

Vgsraw = Vg-Vsi
Vgdraw = Vg-Vdi

2.2 User-defined variables [Not optimized]

There are eleven user-defined variables that are not optimized in AVS. These are listed in Table 1. In AVS 1.0.0, the values of **n0** and **alpha** are not optimized. These are fixed as 2.0 and 6.0, respectively.

2.3 Extracted variables [Optimized]

There are eight parameters in AVS 1.0.0 that are optimized upon calibration with experimental data. These are listed in Table 2.

Even though the parameter **beta** is added to the list of the optimized parameters, it is fixed as 1.8 for the experimental data set included in the release. The methodology for extraction is explained in Section 5.

Table 1: Table showing the fixed parameters in the AVS v1.0.0 model.

Variable	Meaning
W	Device width [m]
Lg	Device length [m]
Cg	Gate capacitance [F/m^2]
n0	Non-ideality factor [unit-less]
alpha	Shift in threshold volatge in sub-threshold and strong inversion [unit-less]
Tjun	Junction temperature [K]
zeta	Channel ballisticity parameter [unit-less]
mc	Relative effective mass of carriers [Kg]
CTM_ select	If **CTM_select** = 1, DD-NVSAT charge-transport model is selected, otherwise blended DD-NVSAT and ballistic charge-transport model is selected. Default is 1. This parameter in no way affects the static transport model.
Cofs	Outer-fringing capacitance for the source-terminal [F/m]
Cofd	Outer-fringing capacitance for the drain-terminal [F/m]

3 Static Transport Model

Most of the previous transport ($I-V$) modeling efforts in GFETs have relied on the drift-diffusion (DD) theory of electron transport with density-dependent saturation velocity [1], [2], [3], [4], [5]. As such the validity of DD-based models may be limited to long channel devices.

At MIT, an alternate transport model based on the concept of virtual source (VS) charge/velocity has been developed for GFETs in both unipolar and ambipolar regimes of operation. The model is also supplemented with channel-charge partitioning that is valid from the drift diffuive to the ballistic transport regimes, where the gradual channel approximation (GCA) is no longer valid.

Table 2: Table showing parameters in the AVS v1.0.0 model that are extracted upon calibration with experimental data.

Variable	Meaning
Rc_elec	Electron branch channel-access resistance [$\Omega - \mu m$]
Rc_hole	Hole branch channel-access resistance [$\Omega - \mu m$]
beta	Saturation parameter in **Fsat** [unitless]
Qmin	Minimum background doping [C/m^2]
mu	Carrier mobility. Assumed equal for both electrons and holes. [m^2/Vs]
vxo	VS injection velocity of carriers. Assumed equal for electrons and holes. [m/s]
delta_tr	Shift in threshold voltage for charge trapping [V]
Vmin0	Dirac-point voltage [V]

3.1 Drain current model

In the VS model, the FET current in saturation is given as the product of the areal charge density, **Qx0**, at the VS and the carrier injection velocity, **vxo**, at the VS. Single-layer graphene, being a gapless material, has two virtual sources – one for electrons and another for holes – at opposite ends of the channel. The net current, therefore, is a superposition of the injected electron and hole currents and is given as

$$\frac{\mathbf{Id}}{\mathbf{W}} = (\mathbf{Qelec}+\mathbf{Qhole})\,\mathbf{vx0} \times \mathbf{Fsat}, \tag{1}$$

where **W** is the channel width and **Qelec** and **Qhole** are the electron and hole concentrations, respectively, at the VS. **Fsat** is an empirical function to produce the transition from the linear to the saturation regimes of transport. **Fsat** is given as

$$\mathbf{Fsat} = \frac{\mathbf{Vdsi/Vdsat}}{\left(\mathbf{1}+(\mathbf{Vdsi/Vdsat})^{\mathbf{beta}}\right)^{\frac{1}{\mathbf{beta}}}}, \tag{2}$$

$$\mathbf{Vdsat} = \frac{\mathbf{vxo} \times \mathbf{LG}}{\mathbf{mu}}. \tag{3}$$

The carier densities are computed as

$$\mathbf{Qelec} = \mathbf{Cg} \times \mathbf{nphit} \times ln(\mathbf{1+exp(etae)}), \quad (4)$$

$$\mathbf{Qhole} = \mathbf{Cg} \times \mathbf{nphit} \times ln(\mathbf{1+exp(etah)}), \quad (5)$$

$$\mathbf{etae} = \frac{\mathbf{Vgsi\text{-}Vtn}}{\mathbf{nphit}}, \quad (6)$$

$$\mathbf{etah} = \frac{\mathbf{Vdgi+Vtp}}{\mathbf{nphit}}, \quad (7)$$

$$\mathbf{Vtn} = \mathbf{Vmin0+delta\_tr\text{-}aphit} \times \mathbf{FFSe}, \quad (8)$$

$$\mathbf{Vtp} = \mathbf{Vmin0\text{-}delta\_tr+aphit} \times \mathbf{FFSh}, \quad (9)$$

$$\mathbf{FFSe} = \frac{\mathbf{1}}{\mathbf{1+exp(etae1)}}, \quad (10)$$

$$\mathbf{FFSh} = \frac{\mathbf{1}}{\mathbf{1+exp(etah1)}}, \quad (11)$$

$$\mathbf{etae1} = \frac{\mathbf{Vgsi\text{-}Vtn+aphit/2}}{\mathbf{aphit/2}}, \quad (12)$$

$$\mathbf{etah1} = \frac{\mathbf{Vdgi+Vtp\text{-}aphit/2}}{\mathbf{aphit/2}}. \quad (13)$$

In the above equations, **aphit** = **alpha**×**phit**; **nphit** = **n0**×**phit**, where **phit (= kB**×**TJun/q)** is the thermal voltage.

3.2 Channel-access resistance modeling

Due to the symmetric energy-dispersion relationship for conduction and valence bands in graphene, the intrinsic mobility and injection velocity of electrons and holes in graphene must be identical [6]. Hence, it is expected that asymmetry in the electron and hole branches of current conduction should result from an asymmetry in the channel-access resistance for electron and hole conduction. Graphene underneath the metal contacts has an altered energy-dispersion relation and may be either p- or n-doped. For contact metals such as Palladium, graphene under the contact gets p-doped [7]. Hence, a p-n junction is formed between the contact and the channel when the channel is n-type. In this case, the p-n junction limits the current for the electron branch resulting in **Relec** > **Rhole**, where **Relec** and **Rhole** are the channel-access resistance for the electron- and hole-branch, respectively.

A phenomenological circuit model to capture the asymmetry is shown in Fig. 2. It must be noted that the resistances **Rs** and **Rd** in Fig. 1 are non-linear voltage-dependent resistances.

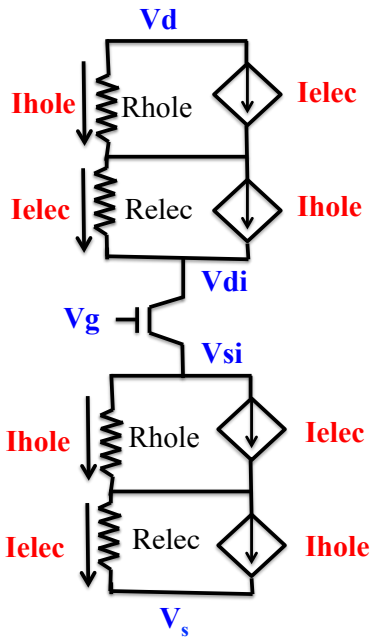

Figure 2: A phenomenological circuit model to capture asymmetry in the electron and hole branches of current conduction in graphene.

4 Dynamic Model

The complete device model must also include terminal charges as functions of terminal voltages to simulate the device dynamic behavior. According to the Ward-Dutton charge partitioning, the terminal charges **QS** and **QD** at the source and drain terminals, respectively, in quasi-static conditions of device operation are given as

$$\mathbf{QS} = \int_0^{\mathbf{LG}} \mathbf{(1\text{-}x/LG)Qc(x)dx}, \tag{14}$$

$$\mathbf{QD} = \int_0^{\mathbf{LG}} \mathbf{(x/LG)Qc(x)dx}, \tag{15}$$

where **Qc(x)** is the position-dependent channel charge. Equations (14) and (15) are universally true irrespective of the ballistic or drift-diffusive transport in the channel as long as the device operates under quasi-static conditions. In the case of graphene, **Qc(x) = (Qhole(x)-Qelec(x))**, where **Qhole(x)** and **Qelec(x)** are the position-dependent hole and electron charges, respectively, in the channel.

4.1 Ballistic charge model

If the device operates in the ballistic regime, the channel charge cannot be given by the gradual-channel approximation (GCA) (see appendix of Ref. [8]). Rather, the more appropriate conditions are current continuity and energy balance for obtaining **Qc(x)** at all locations within the channel [8]. For both electron and hole branches of current conduction, the current continuity yields,

$$\mathbf{Qelec} \times \mathbf{vxo} = \mathbf{Qelecx(x)} \times \mathbf{vex(x)}, \tag{16}$$

$$\mathbf{Qhole} \times \mathbf{vxo} = \mathbf{Qholex(x)} \times \mathbf{vhx(x)}, \tag{17}$$

$$\tag{18}$$

Assuming a linear potential profile within the channel and allowing for a fraction **zeta** of **Vds** energy gained by carriers as they travel along the channel (**zeta** < 1 for quasi-ballistic transport), the carrier velocity as a function of position for both electron and hole branches in the channel is given as

$$\mathbf{vex(x)} = \mathbf{vx0}\sqrt{\mathbf{1+kx/LG}}, \tag{19}$$

$$\mathbf{vhx(x)} = \mathbf{vx0}\sqrt{\mathbf{1+k(1-x/LG)}}, \tag{20}$$

$$\mathbf{k} = \frac{2\mathbf{q} \times \mathbf{zeta\ Vdsi}}{\mathbf{me} \times \mathbf{vxo}^2}. \tag{21}$$

The source and the drain charges in the ballistic region are given as

$$\mathbf{QSB} = \mathbf{WLG(-Qelec} \times \mathbf{F1+Qhole} \times \mathbf{F2)}, \tag{22}$$

$$\mathbf{QDB} = \mathbf{WLG(-Qelec} \times \mathbf{F2+Qhole} \times \mathbf{F1)}, \tag{23}$$

where **F1** and **F2** are given as

$$\mathbf{F1} = \frac{\mathbf{2}}{\mathbf{3k}^2}(\mathbf{(2k+2)}\sqrt{\mathbf{(k+1)}} - \mathbf{(2+3k)}), \tag{24}$$

$$\mathbf{F2} = \frac{\mathbf{2}}{\mathbf{3k}^2}(\mathbf{(k-2)}\sqrt{\mathbf{(k+1)}}\mathbf{+2}), \tag{25}$$

where **k** is given as in Eq. (21).

4.2 Drift-Diffusion non-velocity-saturated (DD-NVSAT) charge model

At low **Vds**, quasi-ballistic devices can be considered as operating in the nearly drift-diffusive non-velocity saturated (DD-NVSAT) regime, where the GCA can be used to estimate channel charge at every location within the channel (see

Chap. 7 in [9]). The DD-NVSAT terminal charges are mathematically given as

$$\mathbf{QSNVSAT} = \mathbf{WLG(\text{-}Qelec \times F1'(te)+Qhole \times F2'(th))}, \tag{26}$$

$$\mathbf{QDNVSAT} = \mathbf{WLG(\text{-}Qelec \times F2'(te)+Qhole \times F1'(th))}, \tag{27}$$

$$\mathbf{te} = \mathbf{1\text{-}Fsatqe}, \tag{28}$$

$$\mathbf{th} = \mathbf{1\text{-}Fsatqh}. \tag{29}$$

The empirical functions **Fsatqe** and **Fsatqh** are similar to the **Fsat** function used in transport formulation with **Vdsat** replaced with **Vdsate = |Vgsi-Vtn|/n0** and **Vdsath = |Vdgi+Vtp|/n0** for electrons and holes, respectively. The functions **F1'** and **F2'** in Eqs. (26) and (27) are given as [9]

$$\mathbf{F1'(x)} = \frac{\mathbf{6+12x+8x^2+4x^3}}{\mathbf{15(1+x)^2}}, \tag{30}$$

$$\mathbf{F2'(x)} = \frac{\mathbf{4+8x+12x^2+6x^3}}{\mathbf{15(1+x)^2}}. \tag{31}$$

4.3 Blended quasi-ballistic and capacitance model

Blending of ballistic and DD-NVSAT charges is considered only when the parameter **CTM_select** $\neq$ **1**, otherwise only DD_NVSAT charges are considered. It must be noted that the parameter **CTM_select** is no way affects the static transport model, based on the charges at the virtual-source points. The virtual-source charges are, in fact, the starting point for the charge partitioning model.

Blending of charges is accomplished through the empirical function **Fsat**, where **Fsat** is the same function used for the transition from linear to saturation regimes of transport in the current equation (see Eq. (2)). Therefore, the net terminal charges valid in all regions of operation are given as

$$\mathbf{QS} = \mathbf{(1\text{-}Fsat)QSNVSAT+(Fsat)QSB+QSOF}, \tag{32}$$

$$\mathbf{QD} = \mathbf{(1\text{-}Fsat)QDNVSAT+(Fsat)QDB+QDOF}, \tag{33}$$

$$\mathbf{QG} = -\mathbf{(QS+QD)}, \tag{34}$$

where **QSOF** and **QDOF** are the outer fringing charges associated with the source and the drain terminals, respectively. The outer fringing charges are given as

$$\mathbf{QSOF} = \mathbf{Cofs} \times \mathbf{Vgsraw}, \tag{35}$$

$$\mathbf{QDOF} = \mathbf{Cofd} \times \mathbf{Vgdraw}. \tag{36}$$

$$\tag{37}$$

The inter-nodal capacitance between terminals i and j is given as

$$\mathbf{Cjj} = \frac{\partial \mathbf{Qj}}{\partial \mathbf{Vj}}, \tag{38}$$

$$\mathbf{Cij} = -\frac{\partial \mathbf{Qi}}{\partial \mathbf{Vj}}, \mathbf{if\ i} \neq \mathbf{j}. \tag{39}$$

Once the nodal charges are obtained, the inter-nodal capacitances can be evaluated using expressions given in Eqs. (38) and (39).

Rferences [10] and [11] explain the model physics in more detail.

5 Parameter Extraction

In the AVS v1.0.0 model, a total eight parameters can be optimized as discussed in Section 1.3. However, for the experimental data set included with this model release, the parameter **beta** is chosen as 1.8. In order for the parameters to be extracted in a realistic and physically meaningful way, it is important to assign proper lower and upper bounds to all the parameters including a robust initial guess. The following table shows the extracted parameters with their lower and upper bounds and initial guess values used in the non-linear parameter extraction routine. In case **beta** is also optimized, we suggest limiting it between 1.4 and 2.2 and assigning it an initial value of 1.8.

Variable	Lower bound	Upper bound	Initial guess
Rc_elec [$\Omega\mu$m]	100	2000	200
Rc_hole [$\Omega\mu$m]	100	2000	200
Qmin [C/m^2]	10^{-4}	3×10^{-4}	2×10^{-4}
mu [m^2/Vs]	500	3000	1500
vxo [m/s]	10^5	8×10^5	5×10^5
delta_tr [V]	0	0.5	0.2
Vmin0 [V]	–	–	–

Above numbers are hard-coded in the extraction routine and it is recommended that they not be tweaked to guarantee the convergence of the code. There are two files that are related with the extraction routine in AVS v1.0.0. These are:

- extract_main.m
- optimize_data.m

The file **extract_main.m** uses experimental data files provided in the package. The user can also use their own experimental data, in which case the data must be formatted in 3-column format. The first column corresponds to the drain-source bias (**Vds**), the second column corresponds to the gate-source bias (**Vgs**), while the third column is the measured drain-source current (**Id/W**) in Amperes per meter of the device width. The file **optimize_data.m** uses MATLAB's built-in routine *lsqcurvefit* to optimize the parameters in the AVS model. Please see the MATLAB product help for the use of *lsqcurvefit*.

5.1 Simulation results using parameter extraction tool

Next we present simulation results from three experimental data sets (**LG** = 650 nm, 300 nm, and 140 nm from IBM [12]). Following table shows extracted parameters for the devices. Figures 3-5 show the output characteristics of the devices.

Table 3: Table showing extracted parameters for the AVS model for experimental data in [12]. For all channel lengths, **Cg** = 3.6×10^{-7} F/cm^2, **beta** = 1.8, **n0** = 2.0, and **alpha** = 6.0.

Variable	LG = 650 nm	LG = 300 nm	LG = 140 nm
Rc_elec [$\Omega\mu$m]	486.8	449.9	373.8
Rc_hole [$\Omega\mu$m]	1092.3	761.4	586.7
Qmin [C/m^2]	10^{-4}	3×10^{-4}	3×10^{-4}
mu [m^2/Vs]	2221	1721.3	1130.7
vxo [m/s]	3×10^5	4.5×10^5	5.4×10^5
delta_tr [V]	0.2564	0.2363	0.0
Vmin0 [V]	-1.06	-0.87	-0.64

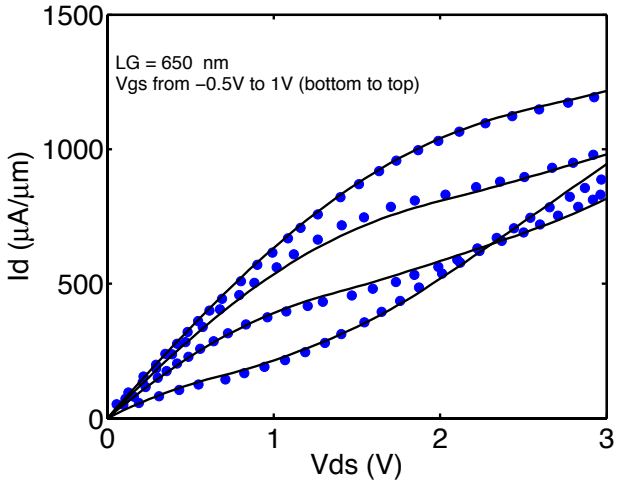

Figure 3: Output characteristics of 650 nm device. Experimental data is shown in symbols, while solid lines show the model fits.

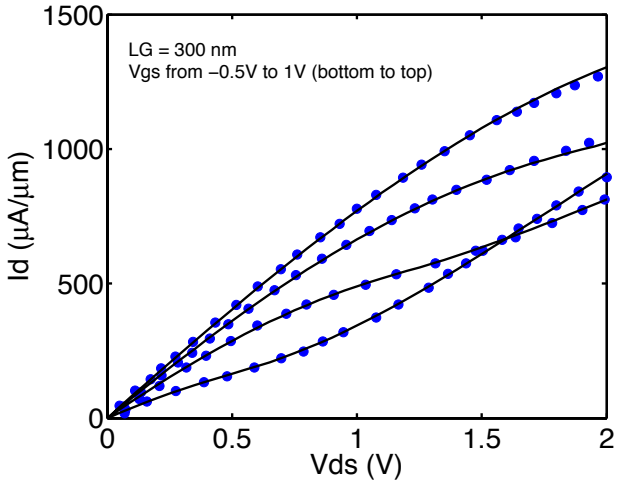

Figure 4: Output characteristics of 300 nm device. Experimental data is shown in symbols, while solid lines show the model fits.

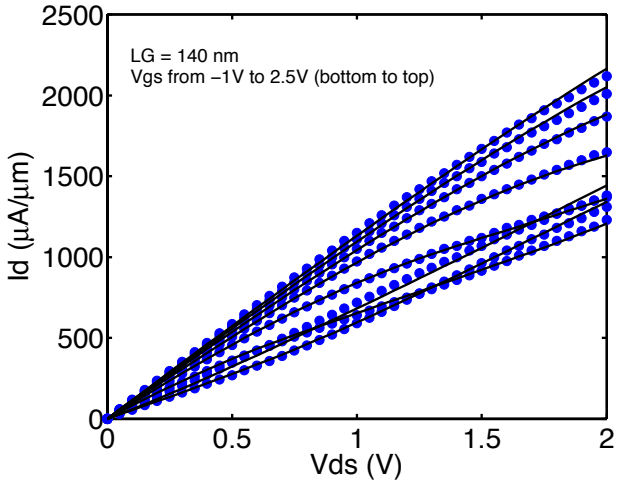

Figure 5: Output characteristics of 140 nm device. Experimental data is shown in symbols, while solid lines show the model fits.

6 Model Exerciser

The purpose of the model exerciser file is to plot various physical quantities such as currents, charges and their derivatives as functions of terminal voltages. The model exerciser can be run with any data set of choice. However, here we show results on charges and capacitances using the parameters extracted for 650-nm data set as tabulated in Table 3.

Figure 6 shows the first and the second derivatives of current with respect to **Vds** and **Vgs** for two values of **Vgs**. There is a bigger discontinuity in the second derivative of the current with respect to **Vds** at **Vds** = 0V for **Vgs** = -0.5V.

Figure 7 shows the various terminal charges plotted with respect to **Vds** using both the DD-NVSAT (**CTM_select = 1**) and the blended QB (**CTM_select = 2**) charge models. The DD-NVSAT charge model has higher terminal charges for the same terminal voltages as expected. Various inter-nodal capacitances are plotted with respect to **Vds** in Fig. 8. The discontinuity in capacitances at **Vds** = 0V increases when the blended QB charge model is used.

The discontinuities at **Vds** = 0V in the current and charge derivatives as shown in Figures 6 and 8 exist because of the terminal swapping when the drain-source voltage changes polarity. The discontinuity in the first derivative of charges (i.e. capacitances) at **Vds** = 0 V can be treated by appropriately smoothing **Vds** as **Vds** → 0V, and will be released as an update in the next version of the model.

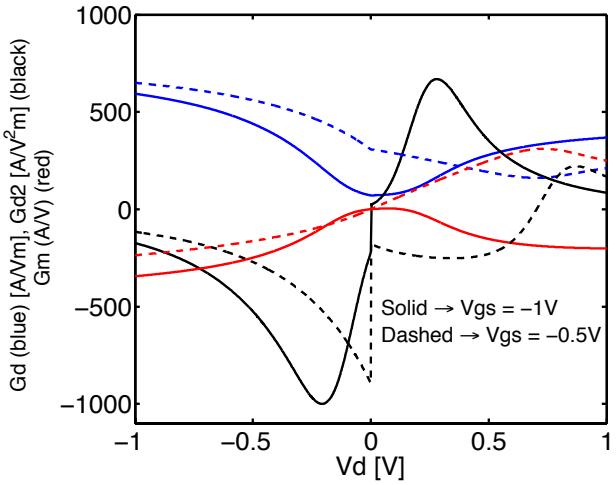

Figure 6: Gd = $\partial I_D/\partial V_d$, Gd2 = $\partial^2 I_D/\partial V_d^2$, and Gm = $\partial I_D/\partial V_g$ versus drain bias for **Vgs** = -0.5V and -1.0V.

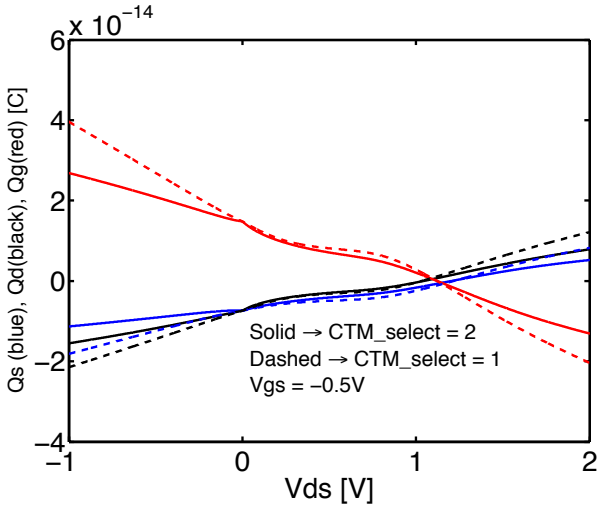

Figure 7: Charges versus **Vds** for the 650 nm GFET.

Figure 9 shows various terminal capacitances of the GFET as functions of **Vgs** using both the DD-NVSAT and blended QB charge models. Clearly, the pure DD-NVSAT model overestimates capacitances. The gate capacitance versus **Vgs** is symmetric about the Dirac point and also exhibits a maximum at the

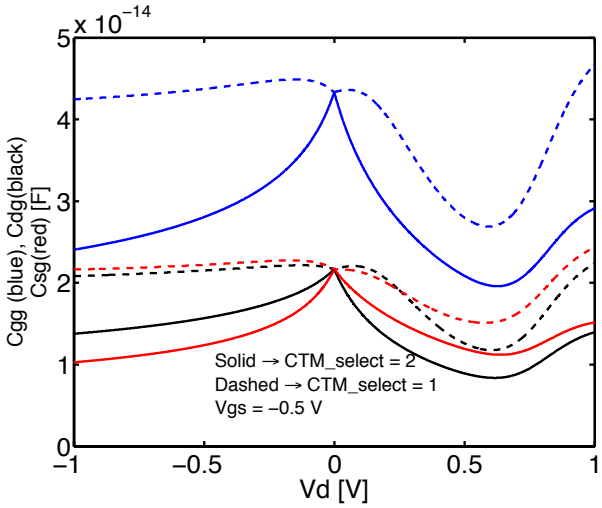

Figure 8: Capacitances versus **Vds** for the 650 nm GFET.

Dirac point. This is because the gate capacitance in GFETs is contributed by both electrons and holes. That is, **Cgg = Cgg,elec+Cgg,hole**. Hence, a bump appears in **Cgg** when there is ambipolar conduction in the channel. Further, with **CTM_select** = 2, blended QB charge model is used, hence the capacitances are lower than those in the case of **CTM_select** = 2.

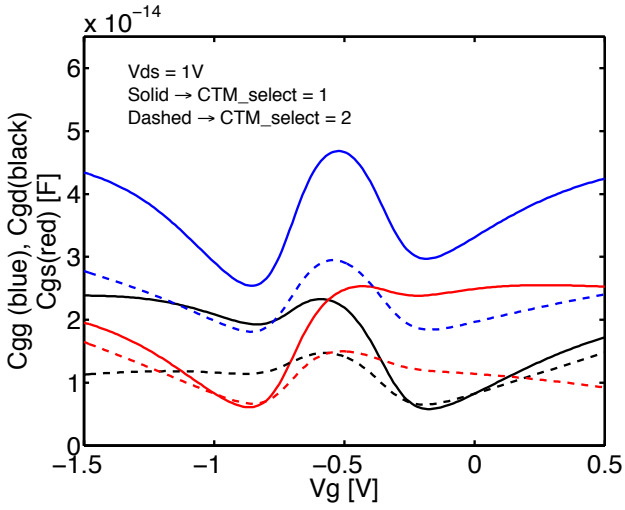

Figure 9: Capacitances versus **Vgs** for **Vds** = 1V.

7 Frequency Doubler Simulations

SPECTRE version *12.1.1.246.isr19 32bit* was used to simulate both the time domain and periodic AC (PAC) response of single-ended and differential-ended frequency doubler circuits shown in Fig. 10. In both the circuits, the gates of the transistors are biased at the minimum conduction point, **Vmin0**. The differential-ended topology suppresses feed-forward of the undesirable fundamental component in the output.

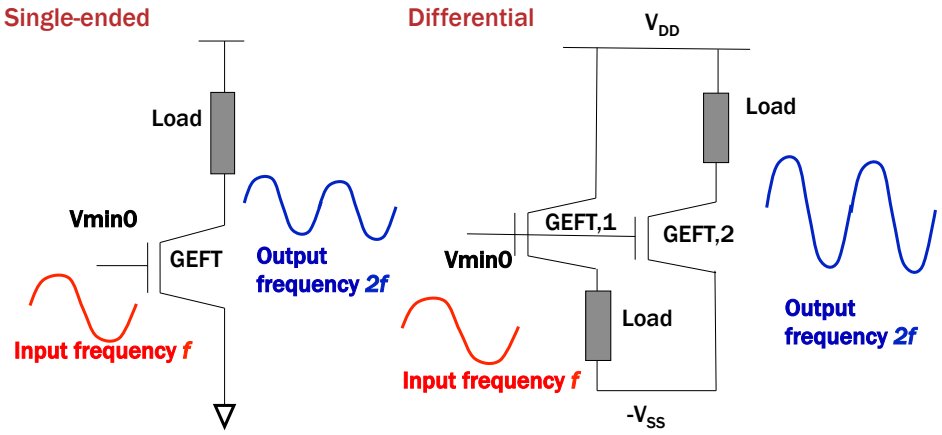

Figure 10: Frequency doubler circuits implemented with GFETs.

The netlist for the frequency doubler circuits are given below.

```
//Time-domain testbench for single-ended frequency doubler implemented with GFETs
simulator lang=spectre
ahdl_include "avs_1_0_0.va"
format options rawfmt=psfascii

parameters vdi=2.0

M1 (d1 g1 s1) avs_1_0_0 Lg=650e-9 Cg=3.63e-3 W=1e-6 Vmin0 = 0.95 Rc_elec=100e-6 Rc_hole=100e-6
CTM_select=1 mu=2209e-4 zeta=0.3
R1 (d1 d2) resistor r=2200


Vpos (d2 0) vsource dc=vdi // positive supply voltage
Vneg (s1 0) vsource dc=0  // negative supply voltage

Vin1 (g1 0) vsource type=sine dc=0.95 ampl=2 freq=1e8


trandiff tran start=0 stop=50n step=1p skipdc=no save=all method=trap
opt options diagnose=yes
```

Figure 11: SPECTRE netlist for time-domain simulation of GFET single-ended frequency doubler.

```
//Time domain testbench for differential-ended frequency doubler implemented with GFET
simulator lang=spectre
ahdl_include "avs_1_0_0.va"
format options rawfmt=psfascii

parameters vdi=1

M1 (d1 g1 s1) avs_1_0_0 Lg=650e-9 Cg=3.63e-3 W=1e-6 Vmin0 = 0.95 Rc_elec=100e-6 Rc_hole=100e-6
CTM_select=1 mu=2209e-4 zeta=0.3
M2 (d2 g1 s2) avs_1_0_0 Lg=650e-9 Cg=3.63e-3 W= 1e-6 Vmin0 = 0.95 Rc_elec=100e-6 Rc_hole=100e-6
CTM_select=1 mu=2209e-4 zeta=0.3

R1 (s1 s2) resistor r=2200
R2 (d1 d2) resistor r=2200


Vpos (d2 0) vsource dc=vdi // positive supply voltage
Vneg (s1 0) vsource dc=-vdi // negative supply voltage

Vin1 (g1 0) vsource type=sine dc=0.95 ampl=2 freq=1e8

port1 (d1,s2) port r=1e9
trandiff tran start=0 stop=50n step=1p skipdc=no save=all method=trap
opt options diagnose=yes
```

Figure 12: SPECTRE netlist for time-domain simulation of GFET differential-ended frequency doubler.

The time-domain response of both frequency doubler circuits is shown in Fig. 13. The input signal is sinusoidal with a frequency of 100 MHz. Clearly the output signal has a frequency of 200 MHz for both the circuits. The device parameters for simulation are given in the netlists. For the same simulation parameters, the amplitude of the output signal of the differential-ended topology is better than that of the single-ended topology.

The netlists correspondig to periodic steady state (PSS) and periodic ac (PAC) simulation of frequency doublers are shown in Figs. 14 and 15. The PSS simulation computes the periodic steady-state response of a circuit at a specified fundamental frequency, with a simulation time independent of the time-constants of the circuit. The PSS analysis also determines the circuit's periodic operating point which is the required starting point for the PAC simulation, which is periodic time-varying small-signal analysis. The PSS simulation results for both frequency doubler circuits are shown in Fig. 16. It can be seen from these figures that the differential-ended frequency doubler suppresses undesirable frequency components in the output.

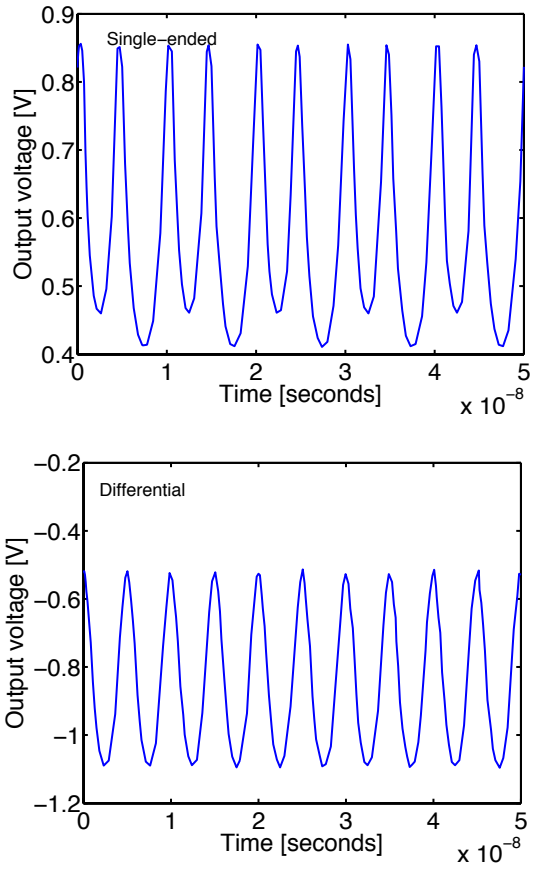

Figure 13: Time domain response of GFET frequency doubler circuits. The supply voltage is 2.0V for single-ended and ±1 V for differential-ended circuit, and the peak-to-peak swing of the input signal on the gate terminal is 4.0V.

```
//Testbench for periodic ac (PAC) simulation of single-ended frequency doubler circuit

ahdl_include "avs_1_0_0.va"
format options rawfmt=psfascii

parameters vdi=2.0

M1 (d2 g1 0) avs_1_0_0 Lg=650e-9 Cg=3.63e-3 W=1e-6 Vmin0 = 0.95 Rc_elec=100e-6 Rc_hole=100e-6
CTM_select=1 mu=2209e-4 zeta=0.3
R1 (d1 d2) resistor r=2200

Vsup d1 0 vsource dc=vdi // supply voltage

Vin1 (g1 0) vsource type=sine dc=0.95 ampl=2 freq=1e8 pacmag=1.0

simulator lang=spectre

pss_sim pss fund=1e8 skipdc=no outputtype=frequency harms=5 save=all maxacfreq=2.1e10 method=trap
errpreset=moderate finitediff=no
pac_sim pac start=1e8 stop=1e11 dec=10 maxsideband = 2 freqaxis=in outputperiod=1n
```

Figure 14: SPECTRE netlist for periodic ac simulation of single-ended frequency doubler.

```
//Testbench for periodic ac (PAC) simulation of differential-ended frequency doubler circuit

ahdl_include "avs_1_0_0.va"
format options rawfmt=psfascii

parameters vdi=1.0

M1 (d1 g1 s1) avs_1_0_0 Lg=650e-9 Cg=3.63e-3 W=1e-6 Vmin0 = 0.95 Rc_elec=100e-6 Rc_hole=100e-6
CTM_select=1 mu=2209e-4 zeta=0.3
M2 (d2 g1 s2) avs_1_0_0 Lg=650e-9 Cg=3.63e-3 W= 1e-6 Vmin0 = 0.95 Rc_elec=100e-6 Rc_hole=100e-6
CTM_select=1 mu=2209e-4 zeta=0.3

R1 (s1 s2) resistor r=2200
R2 (d1 d2) resistor r=2200

Vpos (d2 0) vsource dc=vdi // supply voltage
Vneg (s1 0) vsource dc=-vdi // supply voltage

parameters vg1=2.0

Vin1 (g1 0) vsource type=sine dc=0.95 ampl=vg1 freq=1e9 pacmag=1.0

e1 (out1 0 d1 s2) vcvs gain=1
simulator lang=spectre
pss_sim pss fund=1e9 skipdc=no outputtype=frequency harms=5 save=all maxacfreq=2.1e11 method=trap
errpreset=moderate finitediff=no
pac_sim pac start=100e6 stop=1e11 dec=10 maxsideband = 3 freqaxis=in outputperiod=1n
```

Figure 15: SPECTRE netlist for periodic ac simulation of differential-ended frequency doubler.

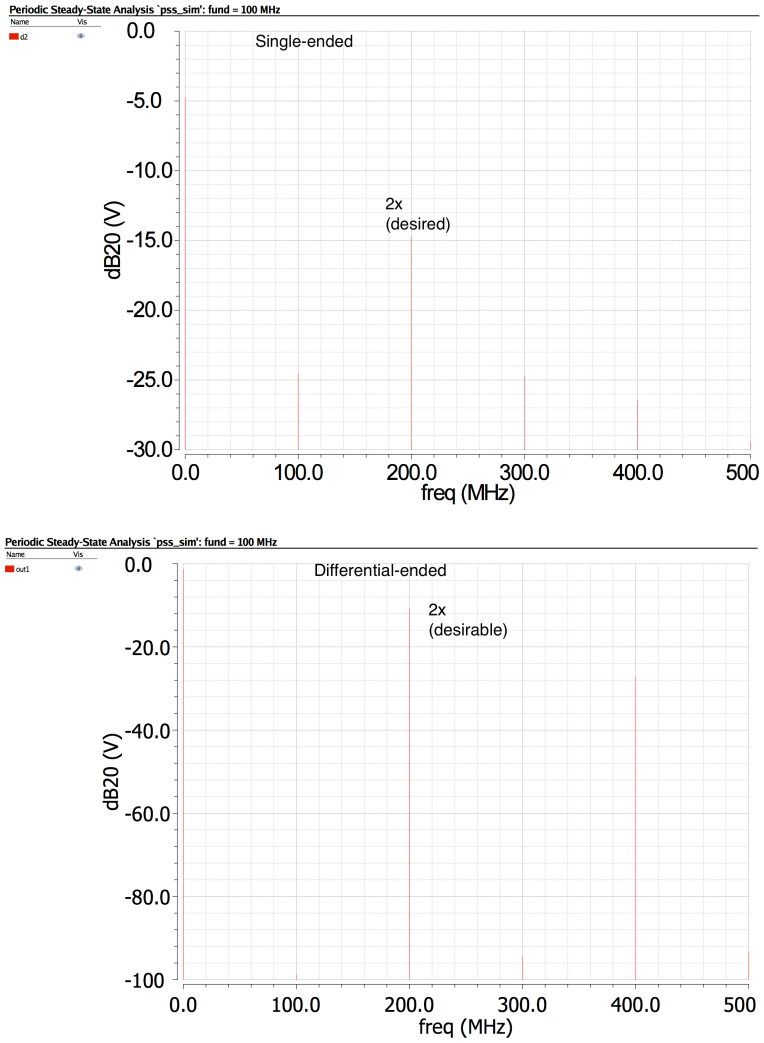

Figure 16: Amplitude of various harmonics in the output of GFET frequency doubler circuits.

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