Universal TFET model
implementation in Verilog-A

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1 Model definitions

General form:

* Verilog-A file of ND TFET model
.hdl 'ndtfet.va'

* Model cards
.lib 'ndtfet.lib' inas_tfet

xXXXXXXXX D G S MNAME <L(VALUE) <W(VALUE>

Example:

x1 7 2 3 ntfet L=20n W=300n

D, G and S are the drain, gate and source nodes, respectively. MNAME is the model name. Use ntfet for n-type tunnel field-effect transistors (TFETs) and ptfet for p-type TFETs. L is the gate length, W is the gate width. Default values for length and width are L = 20 nm and W = 1 µm. Model parameters are in bold text.

TFET Model Parameters:

The model parameters are defined in the file 'ndtfet.lib'. There are two example parameter sets: one for an InAs double-gate TFET (inas_tfet) and one for a single-gate AlGaSb/InAs in-line TFET (algasb_inas_tfet).
The default model parameters are listed below.

<table>
<thead>
<tr>
<th>Name</th>
<th>Name in [1]</th>
<th>Parameter description</th>
<th>Unit</th>
<th>Default</th>
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<tbody>
<tr>
<td><strong>Drain Current Parameters</strong></td>
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<td>DELTA</td>
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<td>Transition width parameter</td>
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<td>E0</td>
<td>( \xi_0 )</td>
<td>Built-in electric field</td>
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<td>( J_0 )</td>
<td>( p-n ) junction saturation current density</td>
<td>A/m(^2)</td>
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<td>JP</td>
<td>( J_P )</td>
<td>NDR current density parameter</td>
<td>A/m(^2)</td>
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<td>MR</td>
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<td>Reduced effective mass</td>
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<tr>
<td>N1</td>
<td>( n )</td>
<td>Sub-threshold ideality factor</td>
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<td>( \gamma_2 )</td>
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<td>Drain access resistance per unit width</td>
<td>( \Omega\mu\text{m} )</td>
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<td>RGWL</td>
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<td>Gate access resistance per gate square</td>
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<td>RSW</td>
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<td>Drain access resistance per unit width</td>
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<td>S</td>
<td>( s )</td>
<td>Ambipolar current attenuation</td>
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<td>( t_{CH} )</td>
<td>Channel thickness</td>
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<td>VP</td>
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<td><strong>Capacitance parameters</strong></td>
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<td>Equivalent oxide thickness</td>
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<td>Gate insulator dielectric constant</td>
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<td>MC</td>
<td>( m )</td>
<td>( C_{gd} ) knee-shape parameter</td>
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## Physical constants

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<tr>
<th>Symbol</th>
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<th>Unit</th>
<th>Value</th>
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<tbody>
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<td>$\hbar$</td>
<td>Planck’s constant</td>
<td>J$\cdot$s</td>
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<td>$k_B$</td>
<td>Boltzmann’s constant</td>
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<td>$m_0$</td>
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<tr>
<td>$q$</td>
<td>Elementary charge</td>
<td>C</td>
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2 Introduction

In the quest for transistors that can replace CMOS as the power horse of the semiconductor industry, steep slope devices such as tunnel field-effect transistors (TFETs) have emerged as the leading contender because of their capability to keep scaling the supply voltage and lowering the power consumption. TFETs utilize interband tunneling as the current conduction mechanism, thus avoiding the Boltzmann-limited subthreshold swing of 60 mV/decade.

To gain more insights into the benefits of tunnel FETs in low power circuit applications and make performance projections, a universal analytical TFET SPICE model that captures the essential features of the tunneling process has been developed [1, 2]. The model is valid in all four operating quadrants of the TFET. Based on the Kane-Sze formula for tunneling, the model captures the distinctive features of TFETs such as bias-dependent subthreshold swing, superlinear drain current onset, ambipolar conduction, and negative differential resistance (NDR). A simple analytic capacitance model of the gate drain capacitance has also been developed and validated on two different TFET structures: a planar InAs double-gate TFET and an AlGaSb/InAs in-line TFET, and good agreement is observed between the model and published simulations. The model is implemented in SPICE simulators using Verilog-A and in native AIM-Spice, available on Mac, Windows, Android, and iOS.
3 Working principle of TFETs

Tunnel FETs utilize a MOS gate to control the band-to-band tunneling across a degenerate $p$-$n$ junction. The schematic cross-section and energy band diagrams of $n$-channel TFET in OFF and ON states are shown in Figure 1a and b. The device is normally off. When zero bias is applied to the gate, the conduction band minimum of the channel is above the valence band maximum of the source, so band-to-band tunneling is suppressed. A tunneling window, $qV_{tw}$, opens up as the conduction band of the channel is shifted below the valence band of the source. Electrons in the valence band with energy in this tunneling window tunnel into empty states in the channel and the transistor is ON. The principle of operation is the same for the $p$-channel TFET with source, channel and drain conductivity types switched.

In the conventional mode of operation, the $n$-channel TFET tunnel current is suppressed when $V_{gs}$ is low and the tunnel window at the source junction is opened with positive $V_{gs}$. However the TFET can turn on at the channel drain junction when the gate bias is sufficiently negative. As shown in Figure 1c when the gate bias is negative, the valence band maximum of the channel can be shifted above the conduction band minimum of the drain leading to electron tunneling from the channel into the drain. Therefore, the tunneling window opens up again, with the tunnel junction shifted from the source-channel junction to the drain-channel junction. When this happens the channel conduction changes from one carrier type to another and the transfer characteristic is said to be ambipolar. This behavior is generally universal across TFET geometries.

When the gate bias is still positive and the drain bias becomes negative, TFET behaves like an Esaki diode, with the signature NDR behavior appearing in the output characteristics.
Figure 1. Schematic cross-section and energy band diagram of an n-channel TFET when the device is biased in (a) OFF (b) ON and (c) ambipolar state where the symbols are defined as follows: $E_C$, conduction band, $E_V$, valence band, $V_{gs}$, gate-source voltage, $V_{ds}$, drain-source voltage, and $V_{tw}$, tunneling window.
4 TFET model

Equivalent circuit
The equivalent circuit of TFET (three terminal device, shown below in Figure 2) includes a voltage controlled current source $I_d$ to model the drain current, capacitors $C_{gs}$ and $C_{gd}$, and source and drain series resistors $R_s$ and $R_d$.

![TFET equivalent circuit](image)

Figure 2. TFET equivalent circuit.

Total drain current
The asymmetric source/drain junction results in asymmetric characteristics both as a function of drain-source bias $V_{ds}$ and gate-source bias $V_{gs}$. In the negative drain-source bias polarity, $V_{ds} < 0$ with positive $V_{gs}$, band-to-band tunneling current first increases toward a current maxima, followed by a region of NDR or a current plateau, followed by an exponentially-increasing diffusion current. When the gate-bias becomes negative, with positive drain-source bias, the tunnel junction can shift from the source-channel junction to the drain-channel junction as discussed with respect to Fig. 1c. The drain current is therefore modeled by summing three currents, as indicated in the following equation:

$$I_d = I_{dt} + I_{da} + I_{de}$$

where $I_{dt}$, $I_{da}$, and $I_{de}$ are defined as:

- $I_{dt}$: drain-source tunneling current (Q1)
- $I_{da}$: ambipolar current (Q2)
- $I_{de}$: Esaki drain source tunneling current and diode current (Q3 and Q4)
The quadrants are defined in Figure 3. The Kane-Sze tunneling current, \( I_{ds} \), is only nonzero in Q1. The ambipolar current \( I_{da} \) is nonzero only in Q2. The Esaki current \( I_{de} \) is the sum of the Esaki tunneling current and diode current, with the Esaki tunneling current being nonzero only in Q4 and the diode current being valid in both Q3 and Q4. The individual currents are defined in the following sections.

![Figure 3. The definition of quadrants.](image)

4.1 Drain-source tunneling current \( I_{dt} \)

The central expression in the TFET model is an experimentally well-established equation for band-to-band, Zener tunneling in planar \( p-n \) junctions [3, 4], the primary transport mechanism in tunnel transistors [5, 6]. The two-terminal Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias-dependent tunneling window \( V_{tw} \) and a dimensionless factor \( f \), which accounts for the superlinear current onset in the output characteristic.

\[
I_{dt}(V_{gs}, V_{ds}) = a \cdot f \cdot E \cdot V_{tw} \cdot e^{-b/E}
\]

where coefficients \( a \) and \( b \) are defined as
\[ a = \frac{W \cdot TCH \cdot q^3}{8 \pi^2 \hbar^2} \sqrt{\frac{2m_r^*}{E_g}} \]

\[ b = \frac{4\sqrt{2m_r^* E_g^{3/2}}}{3q\hbar} \]

where \( m_r^* = (1/m_e^* + 1/m_h^*)^{-1} \) is the reduced effective mass, which is the sum of the reciprocal of the electron, \( m_e^* \), and hole, \( m_h^* \), effective masses, \( E_g \) is the semiconductor band gap, and \( \hbar \) is the reduced Planck’s constant.

\[ m_r^* = MR \cdot m_0 \]

\[ E_g = EG \cdot q \]

The \( f \) factor is given by

\[ f = \frac{1 - e^{-V_{dse}/\text{GAMMA}}}{1 + e^{(V_{thds} - V_{dse})/\text{GAMMA}}} \]

where

\[ V_{dse} = V_{dsm} \left( \frac{V_{ds}}{2V_{dsm}} + \sqrt{\Delta^2 + \left( \frac{V_{ds}}{2V_{dsm}} - 1 \right)^2} \right) \]

\[ V_{dsm} = 10^{-15} \]

\[ V_{thds} = \text{LAMBDA} \cdot \tanh(V_{go}) \]

\[ V_{go} = V_{gs} \]

The parameter \( V_{dse} \) approaches zero as \( V_{ds} \) becomes negative.

The electric field in the tunneling junction is given by

\[ E = E_0 \cdot (1 + R_1 \cdot V_{ds} + R_2 \cdot V_{goe}) \]

where \( V_{goe} \) also approaches zero as \( V_{go} \) becomes negative,

\[ V_{goe} = V_{min} \left( 1 + \frac{V_{go}}{2V_{min}} + \sqrt{\Delta^2 + \left( \frac{V_{go}}{2V_{min}} - 1 \right)^2} \right) \]

\[ V_{min} = 0.0001 \]
The tunneling window is given by

\[ V_{tw} = \ln(1 + e^{V_g t / U}) \]

The Urbach factor, \( U \), is taken to be a linear function of gate source voltage

\[ V_{gt} = V_{gs} - V_{TH} \]

\[ U = R_0 \cdot U_0 + (1 - R_0) U_0 V_{goen} \]

\[ U_0 = V_t \cdot N_1 \]

where

\[ V_t = \frac{k_B (\text{TEMP} + 273.15)}{q} \]

\[ V_{goen} = \frac{V_{goe}}{V_{TH}} \]

4.2 Ambipolar drain-source tunneling current \( I_{da} \)

The ambipolar current is added to the model by copying the current for \( V_{gs} > 0 \) to \( V_{gs} < 0 \) and multiplying the current by a scaling factor, \( s \). The ambipolar drain current is given by

\[ I_{da} = s \cdot I_{dt} (-V_{gs}, V_{ds}) \]

4.3 Esaki drain-source current \( I_{de} \)

When the drain-source bias, \( V_{ds} \), is negative, the source-channel junction is forward biased and behaves like a forward-biased tunnel diode. The NDR is included by modifying a model for the tunnel diode from Sze and Ng [7] to

\[ I_{dr} = -W \cdot TCH \cdot \left( JD \frac{V_{sde}}{V_P} K V_{goe} \frac{e^{1 + V_{sde} - \eta V_{gs}}}{V_P} + J_0 \left( e^{V_{sde} / N_2 V_t} - 1 \right) \right) \]

where \( V_{sde} \) is
\[ V_{sd} = V_{dsmin} \left( \frac{V_{sd}}{2V_{dsmin}} + \sqrt{\Delta^2 + \left( \frac{V_{sd}}{2V_{dsmin}} - 1 \right)^2} - \sqrt{\Delta^2 + 1} \right) \]

and approaches zero as \( V_{sd} \) becomes negative.

### 4.4 Capacitance model

Generally in TFETs \( C_{gs} \) is much smaller compared to \( C_{gd} \) in the TFET and MOSFET [8]. Gate-to-source fringe capacitances due to interconnect can be approximately 1 to 2\( \times \)\( C_{gs} \) in scaled transistor geometries [9].

In the universal SPICE model the TFET gate-source capacitance is set as a constant.

\[ C_{gs} = CGS0 \cdot W \]

The gate drain capacitance, \( C_{gd} \) is modeled as

\[ C_{gd} = C_{gdmin} + (C_{gdmax} - C_{gdmin}) a_{ce} \]

where \( C_{gdmin} \) and \( C_{gdmax} \) are the approximate minimum and maximum values of \( C_{gd} \),

\[ C_{gdmin} = 0.13C_i \]

and

\[ C_{gdmax} = 0.9C_i \]

where \( C_i \) is the intrinsic gate oxide capacitance

\[ C_i = \frac{L \cdot W \cdot \epsilon_{PSI} \cdot \epsilon_0}{EOT} \]

and \( a_{ce} \) is a limiting equation that equals \( a_c \) when \( a_c > 0 \) and approximately 0 when \( a_c < 0 \).

\[ a_{ce} = a_{min} \left( 1 + \frac{a_c}{2a_{min}} + \sqrt{\Delta^2 + \left( \frac{a_c}{2a_{min}} - 1 \right)^2} \right) \]

\[ a_{min} = 0.0001 \]

\( a_c \) is the main equation that sets the shape of \( C_{gd} \).

\[ a_c = \frac{1 + \text{BETA} \cdot V_{gse}^{MC} - e^{-V_{gse}/\text{GAMMAC}}}{1 + e^{(V_{TH} + \text{ALPHA} \cdot (V_{ds} - V_{gse})/\text{GAMMAC})}} \]
\[ V_{gse} = V_{\text{min}} \left( 1 + \frac{V_{gs}}{2V_{\text{min}}} + \sqrt{\text{DELTA}^2 + \left( \frac{V_{gs}}{2V_{\text{min}}} - 1 \right)^2} \right) \]

The model does not conserve charge. A charge-based model is under development.
5 Parameter extraction in Q1

The fitting methodology used to select the parameters in table 1 is outlined as follows. First note that the parameters in the table can be grouped between physical (from EG to TCH) and adjustable (from VTH to LAMBDA). It is straightforward to set the material parameters for a homojunction TFET. For a heterojunction TFET, the material parameters for the channel material may be the best first choice. The adjustable parameters are obtained by fitting within the ranges given in the table manually or using the Curve Fitting Toolbox in MATLAB.

Table 1. Summary and Range of Parameters in the First Quadrant DC Model [1].

<table>
<thead>
<tr>
<th></th>
<th>Range</th>
<th>InAs DG</th>
<th>AlGaSb/InAs SG inline</th>
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<tbody>
<tr>
<td>EG</td>
<td>–</td>
<td>0.354</td>
<td>0.354</td>
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<tr>
<td>MR</td>
<td>–</td>
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<td>0.0218</td>
</tr>
<tr>
<td>TCH</td>
<td>–</td>
<td>5</td>
<td>10</td>
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<td>VTH</td>
<td>0 – $V_{dd}$</td>
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<td>E0</td>
<td>0.5 – 5</td>
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<td>0.839</td>
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<td>0 – 2</td>
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<td>R1</td>
<td>0 – 1</td>
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<tr>
<td>LAMBDA</td>
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<td>0.19</td>
<td>0.33</td>
</tr>
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</table>

Blue: material parameters
Orange: $V_{gs}$ dependence
Green: $V_{ds}$ dependence

5.1 Manual fitting

The selection of VTH is essential to a good overall fit. It can be set roughly in the middle of the knee region of the transfer characteristic and then fine-tuned as needed. The rest of the adjustable parameters can be further divided into 3 groups: in the above-threshold region, E0 and R2; in the subthreshold region, N1 and R0; and for the output
characteristic, \textbf{GAMMA}, \textbf{R1}, and \textbf{LAMBDA}. A good starting point for \textbf{E0}, the internal field, is 1 MV/cm. Then \textbf{R2} is adjusted to get the desired slope in the above-threshold region. The value of \textbf{R2} is not limited to 0−1, because the impact of the gate bias on the electric field is two-fold. It increases the internal field by increasing the tunnel junction barrier and narrowing the barrier. For the subthreshold region, \textbf{R0} and \textbf{N1} are adjusted at the same time to get the slope right. Adjusting \textbf{R2} is effective for \textit{Vgs} less than \textbf{VTH}, and adjusting \textbf{N1} will affect the transition region between the below and above threshold region too. For the output characteristic, the \textbf{LAMBDA} parameter controls the superlinear current onset, \textbf{GAMMA} controls the range over which the drain current saturates with respect to the drain bias, and \textbf{R1} sets how abruptly the drain current increases with drain bias once the current is saturated.

5.2 Automated fitting using MATLAB Curve Fitting Toolbox.

The fitting methodology described above can be automated using functions from the MATLAB curve fitting toolbox. To help the fitting process converge, a rough manual fitting is recommended to find the starting points. With some rough adjustments, the values given in Table 1 can also be used as starting points. As illustrated in Figure 4, the fitting process is two-step, \textit{I_d-V_{gs}} fitting and \textit{I_d-V_{ds}} fitting. In the first step, all fitting parameters are evaluated by fitting the \textit{I_d-V_{gs}} curve at \textit{V_{DD}} within the range given in Table 1 (only two variables \textit{V_{gs}} and \textit{I_d}, line fitting). Then the new values of all the fitted parameters are ported to the second fitting process as the new starting points. In the second step, parameters \textbf{VTH}, \textbf{N1}, and \textbf{R0} are fixed and parameters \textbf{E0}, \textbf{GAMMA}, \textbf{R1}, \textbf{R2}, and \textbf{LAMBDA} are the new fitting parameters. In this step, the family \textit{I_d-V_{ds}} curves are used to get a better overall fitting (three variables, \textit{V_{ds}}, \textit{V_{gs}}, and \textit{I_d}, surface fitting). The fitting method is robust nonlinear least squares. The fitting works by minimizing the least absolute residuals (LAR). The Trust-Region algorithm is used for the fitting procedure. If fitting is not successful at first, parameters such as maximum number of model evaluations (MaxFunEvals) and maximum number of fit iterations allowed (MaxIter) can be adjusted to find a better solution. Tolerances such as TolFun (termination tolerance used on stopping conditions involving the function/model value) and TolX (termination tolerance used on stopping conditions involving the coefficients) can be increased to
relax the constraints and find a better overall fitting. After the two-step fitting, the parameters should be optimized.
6 Simulation results

6.1 Model vs. simulation

In order to test the ability of the model to represent TFET physics, the model is fitted to two very different TFET embodiments. The first is a double-gate $p$-$i$-$n$ InAs TFET [10] with characteristics predicted by an atomistic quantum-mechanical device simulator, and the second is a single-gate in-line broken-gap AlGaSb/InAs TFET [11] as predicted by Synopsis technology computer-aided design (TCAD). The results are shown in Figs. 4 and 5. The model parameters are included in file ‘ndtfet.lib’. The channel length and width are 20 nm and 1 µm, respectively. The model shows good agreement to the simulations. Excellent representation of the superlinear current onset is shown in Figs. 4b and 5b. Close inspection of the bias dependence of the transconductances and conductances obtained by the model shows that the terminal dependences are not matched precisely owing to the generic nature of the tunneling description.

![Figure 4. Modeled and simulated transfer and output characteristics of a 20 nm InAs double-gate TFET. Atomistic simulation data are from [10].](image-url)
Figure 5. Modeled and simulated transfer and output characteristics of a 20 nm broken-gap AlGaSb/InAs single-gate inline TFET. Numerical simulation data are from [11].

6.2 Capacitance model vs. simulation

Figure 6 shows the modeled gate drain capacitance plotted against TCAD data from [8].

Figure 6. Modeled gate drain capacitance, $C_{gg}/C_i$, vs. $V_{gs}$ plotted against TCAD simulation data from [8] with $V_{ds}$ increasing from 0 to 1 V in steps of 0.2 V.
6.3 N-channel TFET $I_d-V_{ds}$ characteristics in Q1 and Q4

In Figures 7 and 8, the $I_d-V_{ds}$ characteristics for -0.5 V < $V_{ds}$ < 0.5 V of the 20 nm InAs double gate TFET are plotted on linear and logarithmic scale.

Figure 7. Output characteristics of 20 nm InAs double gate TFET on linear scale.

Figure 8. Output characteristics of 20 nm InAs double gate TFET on logarithmic scale with NDR at $V_{ds} < 0$. 
6.4 N-channel TFET $I_d - V_{gs}$ characteristics in Q1 and Q2

In Figures 9 and 10, the $I_d - V_{gs}$ characteristics for $-0.5 \, V < V_{gs} < 0.5 \, V$ of the same device are plotted on linear and logarithmic scale. The scale factor for the ambipolar current, S, is set at $10^{-3}$.

Figure 9. Transfer characteristics of a 20 nm InAs double gate TFET plotted on a linear scale.

Figure 10. Transfer characteristics of a 20 nm InAs double gate TFET plotted on a logarithmic scale.
7 References


