A Compact Current–Voltage Model for 2D Semiconductor Based Field-Effect Transistors Considering Interface Traps, Mobility Degradation, and Inefficient Doping Effect
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Abstract—This paper presents an analytical current–voltage model specifically formulated for 2-dimensional (2D) transition metal dichalcogenide (TMD) semiconductor based field-effect transistors (FETs). The model is derived from the fundamentals considering the physics of 2D TMD crystals, and covers all regions of the FET operation (linear, saturation, and subthreshold) under a continuous function. Moreover, three issues of great importance in the emerging 2D FET arena: interface traps, mobility degradation, and inefficient doping have been carefully considered. The compact models are verified against 2-D device simulations as well as experimental results for state-of-the-art top-gated monolayer TMD FETs, and can be easily employed for efficient exploration of circuits based on 2D FETs as well as for evaluation and optimization of 2D TMD-channel FET design and performance.

Index Terms—2D field-effect transistor (FET), 2D semiconductors, compact modeling, interface trap, molybdenum disulphide (MoS2), transition metal dichalcogenide (TMD), tungsten diselenide (WSe2).

I. INTRODUCTION

RECENTLY, 2D semiconductors, primarily the monolayer TMDs schematically shown in Fig. 1(a), such as molybdenum disulphide (MoS2) and tungsten diselenide (WSe2), have gained broad interest as transistor channel materials [1]–[3] in digital applications due to their atomic scale thicknesses and suitable bandgaps [Fig. 1(b)] that are highly desirable properties for low-power field-effect transistors (FETs) in the future sub-10 nm technology nodes. They are also inherently suitable for display electronics [4] and FET-based bio/gas sensors [5], [6], due to their flexibility, transparency, nonzero bandgaps, and dangling-bond-free interfaces. To date, significant progress in this field has been achieved, such as large-scale chemical-vapor-deposition growth of monolayer/multilayer MoS2 [7], n-type multilayer MoS2 FETs with ultralow contact resistance [8], n-type monolayer WSe2 FETs with record ON-current [9], and p-type monolayer WSe2 FETs with subthreshold swing (SS) reaching the theoretical lower limit of 60 mV/dec [10] (although only achieved once so far in experimental works with conventional gate dielectric materials, most reported values are much larger). Moreover, a tremendous amount of efforts are being expended to address remaining practical issues, such as high contact resistances [8], [9], [11] to monolayer TMD FETs, low carrier mobility, high trap density, and lack of efficient doping method, as listed in Fig. 1(c).

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12D semiconductor in this paper specifically refers to 2D transition metal dichalcogenide (TMD) materials with nonzero bandgaps, and parabolic energy dispersions ($E - k$), thus excludes graphene.
In parallel with experimental and physical modeling efforts, compact modeling work is necessary to pave the way for circuit explorations and wide-scale applications of these 2D FETs. The only available work [12] on this topic to date, simply modeled the intrinsic device characteristics based on a lumped capacitance network, which implies that the model is not scalable. In addition, the concepts of drift and diffusion current, chemical or Fermi potential (or voltage), and electrostatic potential are not correctly defined and differentiated, which can be misleading. In general, from an application point of view, any 2D FET model that only considers the intrinsic characteristics is overidealistic, and hence rarely consistent with real device performance. Extrinsic effects that are critical for 2D materials should be considered, to make the models useful and relevant to integrated circuit designers. At present, a 2D FET compact model, which is rigorous and standardized in terms of the mathematical procedure, compatible with industry convention (based on surface potential), self-consistent in terms of the physics, comprehensive in terms of including practical concerns, and calibrated with experimental results, is still lacking. This paper is aimed at providing such a model.

This paper is organized as follows. First, a brief introduction to the unique physics of 2D TMD semiconductors is provided in Section II. Then, a differential system for modeling the 2D FET operation is established in Section III. Based on this differential system, intrinsic current–voltage ($I$–$V$) model as well as $I$–$V$ models that include the key effects of interface traps, mobility degradation, and inefficient source/drain (S/D) doping are derived in Sections IV–VII, respectively. Next, a discussion on modeling of short channel effect (SCE) in 2D FETs is provided in Section VIII. Finally, the conclusions are drawn in Section IX.

II. Fundamentals of 2D TMD Semiconductors

As schematically shown in Fig. 1(a), the in-plane lattice of TMDs has two types of atoms, M and X, which are arranged in a 2D honeycomb array within the TMD plane, and in an X-M-X sandwich form normal to the TMD plane. M stands for transition metal, such as Mo and W. X stands for chalcogen, including O, S, Se, and Te. As in graphite, atomically thin layers in bulk TMDs are held together by weak van der Waals bonds. Each TMD layer has a fixed and uniform thickness of ~0.65 nm. Fig. 1(b) shows the typical band structure of monolayer TMD semiconductors, in which the conduction band minima and valence band maxima separate, and are both at the high-symmetry $K$ point in the first Brillouin zone, i.e., monolayer TMDs have direct bandgaps (obtained by first-principle calculation) [13], in contrast with bulk TMDs that have indirect bandgaps. The indirect-to-direct bandgap transition from bulk TMDs to monolayer TMDs is due to valley transition induced by the spatial confinement along the thickness direction [14]. The energy dispersions near the band edges have classic parabolic shapes, indicating that carrier transport in monolayer TMDs can be described by the effective mass based transport equations. It has been found that the carrier effective masses in monolayer TMDs are generally larger than commonly used semiconductors, such as Si, Ge, and III-V, thus a large density of states (DOS) that is proportional to the effective mass can be expected. Dangling-bond-free monolayer TMDs can potentially achieve superior interface properties and high mobilities, but a perfect 2D crystal and layered gate dielectric material, such as hexagonal boron nitride (h-BN) that is also free of dangling bonds, are the two prerequisites [15]. However, such perfect 2D crystals are not achievable at present. In fact, traps in 2D FETs arising from the imperfection/contamination of the 2D crystals and the dangling bonds at the gate dielectric side in FETs have been recently reported [16], [17]. These traps remain a performance limiter for 2D TMD based electronic devices at the current technology stage of 2D TMD materials.

III. Differential System Establishment

For all electronic devices, there always exists a differential system that is responsible for their physics and operation, and also serves as the starting point for compact modeling. No such system has, so far, been explicitly established for 2D semiconductor FETs. Therefore, this naturally becomes the first step in this paper.

Fig. 1(d) shows a schematic diagram of a typical top-gated n-type 2D FET. Note that the model developed in this paper is transferable to p-type devices by replacing parameters for electrons with that for holes. Since the 2D semiconductor channel has an atomic-scale thickness $T_{2D}$ (~0.65 nm for TMDs), it is reasonable to consider that the electrostatic potential $\phi(x, y)$ inside it does not change in the direction vertical to the channel plane. An arbitrary enclosure along the channel, with a height of $T_{2D}$ and an infinitely small length $\Delta x$, is selected for the analysis, as shown by the zoomed-in-view inset in Fig. 1(d). By applying Gauss’s law to this enclosure, the relationship between the charge density inside the enclosure and electric field outside the enclosure can be obtained

$$\Delta Q = (\varepsilon_TOX\zeta_{TOX} + \varepsilon_BOX\zeta_{BOX})\Delta x + (\varepsilon_2D\zeta_2D(x) + \varepsilon_2D\zeta_2D(x + \Delta x))T_{2D}$$

where $\varepsilon_{TOX}/BOX, 2D$ are the dielectric permittivities of TOX/BOX/2D semiconductor, $\Delta Q = q \Delta x (N_{imp} - n_{2D})$. $q$ is the elementary charge. $N_{imp}$ and $n_{2D}$ are the area densities of impurity (net density = donor density – acceptor density) and electron, respectively. The four electric fields can be written as

$$\zeta_{TOX} = -\frac{V_{gb} - \Delta \psi_t - \phi(x)}{T_{TOX}}, \quad \zeta_{BOX} = -\frac{V_{gb} - \Delta \psi_b - \phi(x)}{T_{BOX}},$$

$$\zeta_2D(x) = \frac{d\phi(x)}{dx}, \quad \zeta_2D(x + \Delta x) = -\frac{d\phi(x + \Delta x)}{dx}$$

where $V_{gb}/b$ are top/bottom gate biases and $\Delta \psi_{t/b}$ are flat-band voltages (= the work function difference (divided by $q$) between the top/bottom gate electrodes and the TMD channel). Note that positive directions of these electric fields are assumed to point outward from the Gaussian enclosure. By substituting the expressions for the above four electric fields in (1) followed by some reorganization, a differential

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and the 2D DOS, DOS 2D, can be obtained as

\[ n_{2D} = \int_{E_e}^{\infty} \text{DOS}_{2D}(E) f(E - E_F) dE \approx N_{DOS} e^{\frac{\epsilon_E}{kT}} \]  

where

\[ N_{DOS} = \frac{g_s g_m m^*}{(2\pi\hbar^2)} T \epsilon_e + \frac{g_s g_m m^*}{(2\pi\hbar^2)} e^{\frac{\Delta E_e}{kT}} \]

which is the effective electron DOS for 2D semiconductors, and the 2D DOS, DOS 2D, is \( \sum_{i=1,2} g_s g_m m^*/(2\pi\hbar^2) \), conduction band minima \( E_e = -q\phi(x) \), Fermi level \( E_F = -qV \), \( T \) is temperature, \( k \) is Boltzmann’s constant, \( \hbar \) is the reduced Planck’s constant, \( g_s \) is spin degeneracy, \( g_{1,2} \) are valley degeneracy, \( m_{1,2} \) are effective masses, \( \Delta E_e \) is the energy difference between the two lowest valleys, and \( V \) is the Fermi potential. Due to the relatively large DOS (\( \sim 10^{14} \text{eV}^{-1} \text{cm}^{-2} \)) of TMDs, the primary 2D semiconductors, FETs based on them generally work in the nondegenerate condition (\( E_F < E_e \)) as verified in Appendix I, thus Boltzmann distribution has been used to simplify the Fermi–Dirac distribution function \( f(E - E_F) \) in (3). Note that the second lowest valley [Fig. 1(b)] for TMD materials is nonnegligible, since \( \Delta E_e \) is only around 2\( kT \), and its valley degeneracy is as large as 6 (there are 6 such valleys inside the first Brillouin zone), compared with 2 for the lowest valley. Other valleys are too high [13] to contribute to electrical conduction, and hence neglected.

Carrier transport is governed by drift–diffusion (DD) equation [18]

\[ I_{ds}(x) = q W n_{2D}(x) \mu(x) \frac{dV(x)}{dx} \]

where \( \mu \) is electron mobility, and \( W \) is device width. Both drift and diffusion components have been included in this equation. Due to the low mean free path (\( \sim 15 \text{nm} \)) [19] of carriers in 2D TMD devices, DD equations remain valid even for sub-100 nm channel lengths.

IV. INTRINSIC I–V MODEL

The channel electrostatics is determined by (2) in which the first and the rest of the terms on the left of the equality sign are responsible for lateral (along the channel) and vertical (toward the gate) electric fields, respectively. In the limit of long-channel condition, the lateral field is weak compared with the vertical, thus can be neglected, which is essentially the gradual channel approximation [18]. Hence, (2) is reduced to

\[ n_{2D} = \frac{\epsilon_2 T_{2D}}{q} \left( \frac{\epsilon_E}{kT} - \frac{\phi}{\lambda^2} \right) + N_{\text{imp}}. \]  

Substituting (3) into (5), the Fermi potential can be explicitly expressed as a function of the electrostatic potential

\[ V = \phi - \frac{kT}{q} \ln \left( \frac{\epsilon_2 T_{2D}}{q N_{DOS}} \left( \frac{\epsilon_E}{kT} - \frac{\phi}{\lambda^2} \right) + N_{\text{imp}} \right). \]

which is very useful in the following I–V model derivation.

Since current remains constant along the channel, it is convenient to convert (4) into an integral form as

\[ I_{ds} = \frac{q W \mu_0}{L} \int_{V_S}^{V_D} n_{2D} dV \]

\[ = \frac{q W \mu_0}{L} \int_{\phi_S}^{\phi_D} \left[ \frac{\epsilon_2 T_{2D}}{q} \left( \frac{\epsilon_E}{kT} - \frac{\phi}{\lambda^2} \right) + N_{\text{imp}} \right] dV \]

The explicit form of (6) makes possible the variable change from \( V \) to \( \phi \). \( \mu_0 \) here is an effective mobility that is independent of biasing condition. \( L \) is the channel length. With the known source voltage \( V_S \) and drain voltage \( V_D \), the lower limit \( \phi_S \) and upper limit \( \phi_D \) of the integral can be obtained by applying Newton–Raphson’s approximation to (6). The final expression for the drain current has a closed form under a continuous function covering all regions of the FET operation (linear, saturation, and subthreshold)

\[ I_{ds} = \frac{q W \mu_0}{L} \left( \frac{\epsilon_2 T_{2D}}{q} \left( \frac{\epsilon_E}{kT} - \frac{\phi_{S,D}}{\lambda^2} \right) + N_{\text{imp}} \right) \left( \phi_D - \phi_S \right) \]

which essentially avoids any nonphysical error when higher-order derivatives are applied to the derived current expression. Although differences exist between the 2D and 3D physics, such as the DOS, and in terms of the methodologies employed in treating the channel potential for 2D FETs and Si semiconductor-on-insulator (SOI)/double-gate (DG) FETs [20], it can be observed that the final expressions have similar form. However, Si SOI/DG FET model cannot be arbitrarily used for 2D FETs, from both the mathematical and device physics perspectives. Specifically, equations for obtaining the unknown terms, \( \phi_S,D \), in the final expressions are very different. On the other hand, DOS in Si SOI/DG FETs is 3D, while it is 2D in 2D FETs, which is physically not interchangeable. Therefore, a physics-based derivation starting from the fundamentals is desirable to provide a convincing result specifically for 2D FETs. To verify the model, transfer characteristics and output characteristics are calculated using the model/simulation throughout this paper, 2-nm SiO$_2$ is used as used in the calculation are \( \mu_0 = 50 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \), \( L = 10 \mu\text{m} \), \( N_{\text{imp}} = 3.5 \times 10^{11} \text{cm}^{-2} \), \( \epsilon_2 = 4.8\epsilon_0 \), where \( \epsilon_0 \) is the vacuum permittivity. As shown in Fig. 2, the analytical model is in good agreement with numerical simulation in all regimes for
both DG and SOI modes. The large S/D contact resistance in the top-gated devices is basically a constant and can be fed into the developed model in the form of a constant series resistance extracted from experiments. Note that this approach is applicable for back-gated devices only when the Schottky barriers at the S/D contacts are low and gate dependence of contact resistance is negligible [8], [9]. Due to the limited space and the similarity between the I–V curves for SOI and DG modes, subsequent analysis and results are shown for the SOI mode only, unless specified otherwise.

V. INTERFACE TRAP MODEL

Interface traps that degrade device performance are inevitable in FETs, even for those made by state-of-the-art CMOS technology. The emerging 2D FETs suffer from this issue even more, since the SS of fabricated 2D FETs so far is mostly found to be much larger than the expected value. Therefore, it is necessary to include this effect into the compact model.

For n-type devices, acceptor-type traps, which are negatively charged when occupied by electrons and are in the upper half of the bandgap in energy, contribute most to I–V characteristics. The charged trap density (equal to the density of electrons that occupy the trap states) can be written as

$$N_{\text{it},j}^{-2D} = \sum_j \frac{N_{\text{it},j}}{1 + e^{-\frac{V_g - E_{\text{it},j}}{kT}}}$$

where $N_{\text{it},j}$, $g_{\text{it},j}$, and $E_{\text{it},j}$ are the trap density, degeneracy, and energy level with respect to the conduction band minima, respectively. By tuning $N_{\text{it},j}$, $E_{\text{it},j}$, and the number of trap levels, $j$, the real trap distribution in energy can be mimicked. To include the contribution from the interface traps, $N_{\text{imp}}$ in (2), (5), and (7) should be revised to be $N_{\text{imp}} - N_{\text{it}}^{-2D}$. Then, an explicit expression of $V$ similar to that in (6) can be obtained. Subsequently, the change of variable procedure can be accomplished in the same manner as introduced in Section IV. The closed form of the last-step integral is achievable, but too complex and long winded. A numerical integration is recommended in this step.

As shown in Fig. 3(a), a good agreement is achieved between the results obtained from the compact model and simulation in the cases of free-of-trap, one trap level (at $E_{\text{it}} = -5kT$) and two trap level (at both $E_{\text{it}} = -5kT$ and $E_{\text{it}} = -10kT$). The trap density for each level is set as $1 \times 10^{12}$ cm$^{-2}$. It can be observed that the interface traps not only degrade SS but also shift the...
threshold voltage. A recent experimental work [10] is used to verify the validity of the developed model in Fig. 3(b) in which relevant parameters are listed. It can be found that the intrinsic $I–V$ model slightly deviates from the experimental values around the threshold point. By introducing a single trap level with appropriately tuned density and energy level [values shown in Fig. 3(b)], the experimental data can be well captured by the interface trap model.

VI. MOBILITY DEGRADATION

Carrier mobility is not only dependent on the material but also affected by the biasing (or electric field) condition of the device, in which the material is integrated. In long-channel devices, lateral electric field is generally weak, thus its effects on the carrier mobility, such as velocity saturation, are negligible. Interestingly, MoS$_2$ was reported to exhibit a very high critical electric field (∼1.15 × 10$^5$ V/cm) [21], which further enhances the immunity of long-channel MoS$_2$ FETs to velocity saturation. In contrast, the strong vertical electric field that shifts the charge centroid in the 2D channel toward the dangling bonds of the gate dielectric is expected to increase the scattering rate for carriers and thus degrade carrier mobility. Due to the lack of a rigorous mobility model for 2D FETs at this stage, we employ an empirical mobility model that has been widely used for Si MOSFETs [22]

$$\mu = \frac{\mu_0}{1 + \left(\left|\xi_{cL}^f\right| + \left|\xi_{bL}^f\right|\right)/\xi_{cL}^f} \quad (10)$$

where $\xi_{cL}^f$ is the critical vertical electric field, $\alpha$ is a fitting factor, and

$$\xi_{cL}^f = \frac{\varepsilon_{\mathrm{BOX}} V_{\mathrm{gl}} - \Delta \psi_I - \varphi(x)}{\varepsilon_{\mathrm{2D}}} T_{\mathrm{OX}}, \quad \xi_{bL}^f = \frac{\varepsilon_{\mathrm{BOX}} V_{\mathrm{gb}} - \Delta \psi_B - \varphi(x)}{\varepsilon_{\mathrm{2D}}} T_{\mathrm{BOX}}$$

are the effective vertical top/bottom dielectric electric fields acting on the carriers. To justify this model for 2D FETs, it is fitted with experimental data extracted from [1] and [23] and our own fabricated top-gated monolayer MoS$_2$ FETs with device topology schematically shown in Fig. 4(a). It can be observed that a good agreement is achieved when $\xi_{cL}^f$ and $\alpha$ are set to be the values listed in the figure, which to some extent reflects the similarity of mobility degradation mechanisms in Si MOSFETs and 2D TMD FETs (for typical Si MOSFETs, $\xi_{cL}^f$ is $\sim 9 \times 10^7$ V/m and $\alpha$ is $\sim 1.86$ [22]). Note that the values of $\xi_{cL}^f$ and $\alpha$ would typically vary a little bit under different processing conditions or with different gate dielectric materials.

To include this mobility model, only (7) needs to be revised as

$$I_{ds} = \frac{q W}{L} \int_{V_g} \mu \left[2 V_{\mathrm{2D}} T_{\mathrm{2D}} \left(2 - \frac{\varphi}{\Delta \psi} - \frac{\varphi}{\Delta \psi} - \frac{\varphi}{\Delta \psi} + N_{\mathrm{imp}} \right) + \frac{d V}{d \varphi} \right] d \varphi. \quad (11)$$

Following the procedure introduced in Section IV, the current can be calculated. Similar to the case of the interface traps, the last-step integral can be achieved using numerical integration due to its complex closed form. As shown in Fig. 4(b), the accuracy of including the mobility model into the $I–V$ model is well verified by simulations. It can be observed that mobility degradation results in the nonlinearity of the $I_{ds}$–$V_g$ curves (linear scale in red) and decrease of transconductance ($g_m$) after turn-ON. It is worth mentioning that any other vertical-field-dependent mobility model for 2D FETs that may be established by systematic study in the future can be integrated into our $I–V$ model in the same manner, as shown in this section.

VII. INEFFICIENT SOURCE/DRAIN DOPING

Similar to other low-dimensional materials, such as 1D nanotubes and nanowires, 2D semiconductors currently lack efficient doping method (a recently developed doping method can achieve high doping level, but it is not practical due to the instability of the gas-phase dopants [10]), which makes the access resistance of the 2D FETs significantly high. Although the contact resistance, one component of the access resistance of FETs, has been effectively reduced (to 0.8 kΩ·μm for few-layer MoS$_2$ FETs [8]) by effectively metalizing the TMD underneath with selected metals that can form overlapped d-orbitals with TMD, so that the Schottky and tunnel barriers vanish [11], [24], the resistances in the S/D extensions between gate and contact remain high. Purely using a series resistance to model the function of S/D extension is
A more reasonable approach is to divide the device into three regions along the channel: a depletion region at the drain side, and dependent on the bias dependent. More specifically, it is dependent on the Fermi potentials are only fixed at source (extension), and to drain (source extension), and  to drain extension. Each region is seen as a separate device with different structures. For the device operated in SOI mode shown in Fig. 1(d), the channel region remains an SOI device, while S/D extensions act as bottom-gated FETs. The Fermi potentials are only fixed at and continuous at and . The other useful condition is that current is continuous at and . These four equations can be written as

\[
\begin{align*}
V(o) &= V_{S/D}(\phi_S(o)) = V_{Ch}(\phi_S(o)) \\
V(x_L) &= V_{S/D}(\phi_D(x_L)) = V_{Ch}(\phi_D(x_L)) \\
I_{ds} &= I_{ds,S/D}(\phi_S(x_S), \phi_D(x_D)) = I_{ch,S/D}(\phi_S(x_S), \phi_D(x_D)) \\
&= I_{ds,S/D}((\phi(x_S), \phi_D(x_D)))
\end{align*}
\]

where and are modified functions of and , respectively, in which is replaced by and is replaced by . and are the same as in (6) and (8), respectively.

\[
\phi = \frac{\phi(0) \sinh[(L - x)/\lambda] + \phi(L) \sinh(x/\lambda)}{\sinh(L/\lambda)}
\]

where and are determined by the boundary conditions (BCs) at of : at drain side, at source (extension) and , and at drain extension. Subthreshold current can be obtained by substituting (4) to

\[
I_{ds} = \frac{\mu_0 W k T N_{DOS} (1 - e^{-\theta(V_D - V_S)})}{\int_0^L e^{-\theta(x)} dx}
\]

Substituting (15) into the definition of SS, we get

\[
SS = \left( \frac{d \log(I_{DS})}{dV_G} \right)^{-1} = \frac{2.3 k T}{q} \frac{\int_0^L e^{-\theta(x)} dx}{\int_0^L e^{-\theta(x)} d\phi(x) dx}
\]

where

\[
\frac{d\phi}{dV_g} = \begin{cases} 
\frac{2}{\lambda T} \left(1 - \frac{\sinh[(L - x)/\lambda] + \sinh(x/\lambda)}{\sinh(L/\lambda)}\right), & \text{SOI} \\
1 - \frac{\sinh[(L - x)/\lambda] + \sinh(x/\lambda)}{\sinh(L/\lambda)}, & \text{DG}
\end{cases}
\]

It can be observed from the above expressions that the controllability of gate (d\phi/dV_g) (relevant to the vertical electric...
field in the gate dielectric) is independent of the permittivity of the 2D semiconductor channel, which is due to the fact that the 2D channel is so thin that it contributes little to the potential or electric field distribution in the vertical direction. It can also be found that \( dp/dV_g \) is degraded when gate length \( L \) becomes small. SS is calculated using (16) for the DG-mode case in Fig. 6. SS increases rapidly when \( L \) decreases to sub-20 nm regime. It is observed that the compact model deviates from simulation results when \( L \) decreases to sub-30 nm. The inset shows the potential profile along the channel in the case of \( L = 20 \) nm, which also deviates from simulation at the S/D sides. Results in the SOI mode deviate even more, which is not shown here due to space limitation. This stems from an assumption during the establishment of the differential system in the beginning that the electric field in the oxides is along the vertical direction. In fact, electric field in the top and bottom oxides also has lateral component similar to that considered in the channel. The preassumption that electric field in the gate dielectric is vertical to the channel, is only valid when the channel is much thicker than the channel as in ultra-thin body (UTB) SOI/DG MOSFETs. For 2D FETs, the gate dielectric is much thicker than the channel. Under this condition, the electric field distribution cannot simply be considered vertical to the channel. 2D Poisson’s equation should be rigorously solved in the gate dielectric to obtain the channel potential. This effect therefore needs careful consideration for 2D FETs with \( L < 30 \) nm.

IX. CONCLUSION

In summary, a compact \( I-V \) model for 2D TMD semiconductor channel FETs that not only considers intrinsic device performance but also includes the effects of interface traps, mobility degradation, and inefficient S/D extension doping effect, is introduced and verified by 2-D numerical simulations as well as experimental results for state-of-the-art top-gated monolayer TMD FETs. The scalability of the model for ultra-short channel 2D FETs up to sub-30 nm channel lengths is discussed as well. The compact models developed in this paper are found to pass the Gummel symmetry test, as demonstrated in Appendix IV. Moreover, they are derived from the fundamentals considering the unique physical properties of the 2D TMDs, and thus are specific to them. This eradicates the necessity of any tentative effort in modifying the models for Si MOSFETs to that for 2D FETs, which may introduce unphysical issues. From an utility point of view, these models not only provide a useful platform for circuit explorations and benchmarking (with respect to Si) with such emerging 2D FETs but also offer the growing 2D TMD FET device community a user-friendly tool to gain straightforward insight into these devices and also to examine their device characterization results, thereby facilitating device design and performance optimization.

APPENDIX I

VERIFYING BOLTZMANN STATISTICS

To verify the validity of using Boltzmann statistics, we calculate the channel potential versus gate voltage for monolayer MoS\(_2\) (a typical material among TMDs) DG FETs considering Fermi–Dirac and Boltzmann distribution respectively, as shown in Fig. A1. It can be observed that only for the condition of aggressively scaled gate oxide (both TOX and BOX in Fig. 1(d) = 1 nm SiO\(_2\)), and only in the very strong inversion regime, does the channel potential go beyond the Fermi potential, i.e., degenerate condition. However, the essence of using ultrathin 2D TMDs as channel materials in FETs is to help improve the device electrostatics, which in turn avoids the aggressive scaling of gate dielectric and prevents gate leakage. In fact, the TMD FETs are even further away from degenerate condition compared with Si DG FETs, which can be shown by comparing Fig. A1 with Fig. 3 in [27]. This is due to the large DOS and hence large quantum capacitance (\( C_q \) in S1) that leads to the weak dependence of the channel potential, beyond the threshold voltage, on the gate voltage (most of it drops across the gate dielectric), and thus prevents the gate from moving \( E_F \) above \( E_c \).

\[
C_q = \frac{\partial n_{2D}}{\partial \phi} \approx \frac{q^2 N_{DOS}}{kT} e^{-\frac{E_F-E_c}{kT}}. \tag{S1}
\]

Therefore, using Boltzmann distribution in this paper is justified. It is worthwhile to mention that the large DOS can also help prevent source starvation [28] in 2D TMD FETs that degrades device performance in the ballistic transport regime in the ultrashort channel case.
APPENDIX II
NUMERICAL SIMULATION

In our numerical simulation, the 2-D Poisson’s equation

\[ \frac{\partial}{\partial x} \left( \epsilon(x, y) \frac{\partial \phi}{\partial x} \right) + \frac{\partial}{\partial y} \left( \epsilon(x, y) \frac{\partial \phi}{\partial y} \right) = \frac{q(n_{2D} + N_{2D, it} - N_{imp})}{\varepsilon_0} \]

and the 1-D transport equation along the channel

\[ \begin{cases} \frac{d}{dx} (qWn_{2D}(x)\mu(x)\frac{dV(x)}{dx}) = I_{ds} \\ \frac{d}{dx} I_{ds}(x) = 0 \end{cases} \]

are solved iteratively with finite difference method within the domain shown in Fig. A2. Electrostatic and Fermi potentials, instead of the usually adopted electostatic potential and carrier density, are chosen as variables in the self-consistent iteration to ensure a good numerical stability. Dirichlet (first-type) BC is used at top/bottom gates marked with blue lines, while Neumann (second-type) BC is used elsewhere marked with red lines [29]. Fermi potential is fixed at the source and drain. Carrier distributions in the conduction band and trap states are the same as in (3) and (9), respectively. Mobility model is integrated as a function of the local vertical electric field near the single-row grid points in the channel.

APPENDIX III
MODEL FOR P-TYPE DEVICE

In order for the developed model to be applicable to p-type devices, some parameters for electrons should be modified to that for holes. Detailed derivation procedure is similar to that in Sections III-V, and we only provide the key results as follows.

First, electron density \( n_{2D} \), should be changed to hole density \( p_{2D} \), and (3) should be modified as

\[ p_{2D} = \int_{-\infty}^{E_g} DOS_{2D}(E) [1 - f(E - E_F)] dE \approx P_{DOS} \left( \frac{E - E_F}{kT} \right) \]

where \( DOS_{2D} = g_s m^*_p / (2 \pi h^2) \), \( P_{DOS} = g_s m^*_p kT / (2 \pi h^2) \), and \( m^*_p \) is the hole effective mass. Here, we only consider the first hole valley at K point in the first Brillouin zone. Second, (6) should be modified as

\[ V = \phi + \frac{E_g}{q} + kT \ln \left( \frac{\left( \frac{e_20 T_{2D}}{q DOS_F} \left( \frac{\phi}{kT} - \varsigma \right) - N_{imp} \right)}{\left( N_{imp} \right)} \right) \]

and finally, (8) should be modified as

\[ I_{ds} = \frac{qW\mu_0}{L} \left( \frac{e_20 T_{2D}}{q} \left( \frac{kT}{q} \frac{\phi}{kT} - \varsigma \right) - N_{imp} \right) \left( \phi_s - \phi_D \right) \]

\[ + \frac{T_{2D} e_20 \phi_s^2 - \phi_D^2}{2q\lambda^2} \]

APPENDIX IV
GUMMEL SYMMETRY TEST

Gummel symmetry test [30] is usually used as a benchmark test for developed compact models, to quantify their S/D symmetry. It can be found that during the mathematical derivation in this paper, source and drain are not specifically marked test for developed compact models, to quantify their S/D symmetry. It can be found that during the mathematical derivation in this paper, source and drain are not specifically labeled, which indicates the inherent S/D symmetry of the developed models. As plotted in Fig. A3, \( I_{ds} \) and its second derivatives are odd functions of S/D stimulus voltage \( V_x \) and continuous in the vicinity of \( V = 0 \), which meets the requirements of Gummel symmetry test.

REFERENCES


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