Nano-Engineered Electronic Device Simulation Node (NEEDS)

Compact Model oTFT ver. 2.04.01
For Simulation of Organic and other Thin-Film Transistors

Manual

Ognian Marinov
McMaster University – ECE, 1280 Main Street West, Hamilton, Ontario, L8S 4K1 Canada
Tel: +1(905)525-9140 ext. 27266
Email: omarinov@yahoo.com

The oTFT compact models are aimed to support the bias enhancement of the charge carrier mobility and the significant contact effect in organic thin-film transistors (OTFTs). The oTFT models are “mirror” of the TFT structure.

The current version 2.04.01 of the oTFT compact model level 2 also supports other effects, such as channel conductance modulation (analogous to the channel length modulation in MOS transistors) and Ohmic and non-linear leakages. Quasi-static charge sub-model supports frequency and temporal response by AC and transient simulations.

The model is with default values of parameters for organic thin-film transistors, but otherwise, the oTFT models are also applicable to other thin-film transistors (TFTs). Just the model parameters are with other values.

This manual is with the purpose of advising for the use of the Verilog-A implementation of the oTFT ver. 2.04.01. The Verilog-A code is available at https://nanohub.org/groups/needs/compact_models

The manual guides through the implantation and usage of the code, and provides links to the background of the oTFT compact models. However, the background is discussed in publications, and it will be not emphasized in the manual. The emphasis is to provide for utilization of the code for device and circuit simulation by researchers that might not be primary involved in compact modeling and computer simulation.

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1. TFT mirrored in oTFT compact model

The oTFT compact models are aimed to support the bias enhancement of the charge carrier mobility and the significant contact effect in organic thin-film transistors (OTFTs). The oTFT compact model level 2 also supports other effects, such as channel conductance modulation (analogous to the channel length modulation in MOS transistors) and Ohmic and non-linear leakages. Quasi-static charge and overlap capacitance sub-models support AC and transient simulations.

The distinct difference between TFT models and models for crystalline semiconductor field-effect transistors is that the mobility \( \mu \) in TFT increases at higher bias as a power-law function

\[
\mu(V_G) \approx \frac{\mu_o(V_G)}{(V_G - V_T)^\gamma}, \text{ usually } V_T = 1V
\]

where the mobility enhancement factor \( \gamma > 0 \) (gamma in the oTFT compact models) is in the exponent of the power-law function, and \( \mu_o \) is a known value of the mobility at given overdrive voltage \( V_T \). The low-field mobility \( \mu_o \) is denoted with “uo” in the oTFT 2.04.01 compact model, and \( \mu_o \) and \( V_T \) are model parameters. \( V_G \) stands for gate bias voltage and the threshold voltage \( V_T \) of the OTFT is also a parameter in the oTFT compact model.

The oTFT models are “mirroring” the OTFT structure as depicted in Figure 1. Conceptually, the oTFT models are arranged so that the sub-model components can be changed, replaced, removed or upgraded [1], as the needs evolve.

![Figure 1. Correspondence between the structures of OTFT and oTFT models [4]](image)

The oTFT models are hierarchical. The top hierarchical level is module oTFT (G,D,S,G1,D1,S1), in which there are “rails” for interconnection of the sub-models and instantiations of the sub-models between the rails (Figure 2). The “rails” are:

- Terminal nodes G, S and D for gate, source and drain, respectively. The oTFT model is connected in circuits by these nodes G, S and D;
• Intrinsic nodes GI, SI and DI. The semiconducting film of the OTFT is between SI and DI, and GI represents the interface of the gate dielectric with the gate conductor. Contact resistances and other terminal effects (such as geometric capacitances) are placed between rails S-SI, D-DI and G-GI. The intrinsic OTFT (semiconducting film and gate dielectric) is placed between the intrinsic nodes SI, DI, and GI;

• Control nodes GTS, GTD are conveying values of effective overdrive voltages. \( V_{GTS} \approx (V_{GI} - V_T - V_{SI}) \) and \( V_{GTD} \approx (V_{GI} - V_T - V_{DI}) \) are effective overdrive voltages at the source and drain ends of the intrinsic channel. These \( V_{GTS} \), \( V_{GTD} \) are generated by a model for effective overdrive voltage, and \( V_{GTS} \), \( V_{GTD} \) control many sub-model components, including the TFT generic charge drift DC model and the quasi-static charge model. \( V_{GI} \), \( V_{SI} \) and \( V_{DI} \) are the potentials of the intrinsic nodes GI, SI, DI, and \( V_T \) is the threshold voltage of the OTFT. The use of the control “rail” GTS, GTD makes the oTFT model symmetric and independent of the reference potential of electrical ground. The control nodes are implements as real variables VGTS and VGTD in the Verilog-A code of oTFT 2.04.01 compact model.

The adoption of the above three “rails” provides advantages and convenience. For example, one clearly identifies sub-models for channel or for contacts, and can easily replace a sub-model (or even ignore it in simplifications during experimental characterizations [2], [5]), without destructing the behavior of the oTFT model. The “rails” also allow the sub-models to be simple, well related to physical interpretations and minimizes the number of model parameters and interferences between parameters [1]. In fact, the oTFT models are circuits with manageable components, instead of fixed “rigid” template of characteristic equations.

![Figure 2. Topology of the oTFT compact models with sub-models and interconnecting “rails”](image)

The hierarchy of the oTFT compact models is illustrated in Figure 3. Stimuli from the circuit are taken by the hierarchical top of the oTFT model, which also adds the model parameters of the OTFT and distributes the signals and parameters to the sub-models. The sub-models themselves distribute the stimuli and parameters downwards in the hierarchy. The responses from the sub-models propagate upwards to the rails of the hierarchical top, which establishes the operation of the oTFT compact model. The response from the terminal rail G, D, S is returned to the circuit.
Figure 3. Hierarchy of the oTFT compact model

Considering the modularity both in topology and hierarchy, the oTFT compact models are flexible for manipulations both for simplifications and enhancements [1], as desired in the practice of OTFT development. The hierarchical top manages the connection of the sub-models and distributes the model parameters (Table 1 in Sec. 2.1) by instantiation of sub-models. The characteristic equations of the sub-models are given in Sec. 2. The customization of the oTFT model is addressed in Sec. 5. Customization by “reconnection” of sub-models is inconvenient, due to a need changing the Verilog-A code. Therefore, a proper assignment of model parameters values is the method for suppression of sub-models in oTFT 2.04.01 compact model. Once a sub-model is suppressed, then one can explore a custom model by connecting circuits between the rails of the oTFT model. For example, one can suppress the leakage sub-model in the oTFT model, and connect a circuit that represents optical generation between the terminals or intrinsic nodes. To allow this method for activation and suppression of sub-models, a special care is taken that each sub-model is self-consistent and fully determined by parameters and controls from its immediate “parent” in the hierarchy. Thus, one can “cut” a branch in the hierarchical tree without destructing the behavior of the other branches in the oTFT model. Once the sub-models are organized from top to bottom of the hierarchy, then the simulation adequately represents the TFT. Examples with the current-voltage curves of the oTFT compact model with default values of the model parameters are given in Sec. 6.

Of course, the reconfiguration of the oTFT model has a limit. One should never “cut” the tree or suppress the core sub-model. The core sub-model is the generic TFT charge drift model [1], [4], shown on left in Figure 3. This sub-model is the identity and determines the overall behavior of the oTFT models. The other sub-models affect magnitudes, but do not change the overall behavior.
2. Parameters and characteristic equations of the oTFT compact model

The oTFT 2.04.01 compact model contains several sub-models, connected between the device terminals (G,S,D), intrinsic nodes (G_{I},S_{I},D_{I}) and control rail (V_{GTS},V_{GTD}). The sub-models included in the oTFT 2.04.01 compact model are:

- Generic TFT charge drift DC model with sub-models for overdrive voltages (core model)
- Contact model (for contact resistances between terminal and intrinsic nodes)
- Channel modulation model (for conductance between drain and source in saturation regime)
- Channel leakage model (for leakage current between drain and source)
- Quasi-static charge model (for charges and capacitive currents)
- Overlap capacitances (and other geometrical capacitances between TFT terminals)
- Monitor of quantities (forwards quantities to test terminals, isolated from oTFT model)

The latter monitor is included in the particular Verilog-A implementation of the oTFT 2.04.01 compact model. The monitor forwards a copy of selected internal quantities to a monitoring rail with electrical nodes (testGND,testSIGNAL). The monitor will not be addressed in this section, because the monitoring rail is “isolated” from the other rails, and it does not affect the operation of the oTFT model.

On below in this section, the sub-models in the oTFT 2.04.01 compact model are explained, so that researchers, designers or other users of the compact model become aware of the significance of model parameters, and properly manage the compact model. The model parameters are summarized in Table 1 with brief comments for immediate reference.

2.1. Generic TFT charge drift DC model with sub-models for overdrive voltages

The generic TFT charge drift DC model is the core in the oTFT models. The generic TFT charge drift model is connected between the intrinsic nodes (G_{I},S_{I},D_{I}) of the oTFT models, as shown in Figure 4. The sub-models for overdrive voltages generate the control rail (V_{GTS},V_{GTD}). The current flow in the generic TFT charge drift DC model is controlled by overdrive voltages (V_{GTS},V_{GTD}).

![Figure 4. Mapping of the generic TFT charge drift DC model in oTFT compact model](image-url)
The generic TFT charge drift DC model is given by [1]

$$I_{\text{DS,}} = \text{np} \times \left[ \frac{W}{L} \frac{C}{\mu_0} \frac{H_0}{(V_I)^{\gamma}} \right] \times \left\{ \frac{(V_{\text{GTS}})^{(2+\gamma)} - (V_{\text{GTD}})^{(2+\gamma)}}{2 + \gamma} \right\}$$

(2)

where the overdrive voltages $V_{\text{GTS}}$ and $V_{\text{GTD}}$ at the source and drain ends of the intrinsic channel are given by the effective overdrive voltage model [1]

$$V_{\text{GTS}} = V_{\text{SS}} \ln \left[ 1 + \exp \left( \frac{\text{np}(V_{\text{GI}} - V_T - V_{\text{SI}})}{V_{\text{SS}}} \right) \right] \approx \left\{ \text{np}(V_{\text{GI}} - V_T - V_{\text{SI}}) \text{ above threshold} \right\} > 0$$

$$V_{\text{GTD}} = V_{\text{SS}} \ln \left[ 1 + \exp \left( \frac{\text{np}(V_{\text{GI}} - V_T - V_{\text{DI}})}{V_{\text{SS}}} \right) \right] \approx \left\{ \text{np}(V_{\text{GI}} - V_T - V_{\text{DI}}) \text{ above threshold} \right\} > 0$$

(3)

These sub-models determine the overall “shape” and “scaling” of the TFT characteristics. The scaling is through the TFT device constant $(W/L)C_\mu_0/(V_\gamma)$ in the square brackets of eq. (2). The channel current $I_{\text{DS,}}$ is proportional to channel width $W$, unit-area gate oxide capacitance $C$, low-field mobility $\mu_0$, and inversely proportional to the channel length $L$. One usually takes value of 1 volt for the reference overdrive voltage $V_\gamma$ for $\mu_0$, so that $(V_\gamma)^{\gamma}$ is also of unity value. The TFT polarity selector is np=+1 for n-type TFT, causing $I_{\text{DS,}}$ to flow from drain to source, or oppositely, when np=-1 for p-type TFT. The “shape” of the DC characteristics is determined by the term in the curly brackets of eq. (2) in conjunction with the values of the overdrive voltages from eq. (3). Consider n-type TFT, for which np=+1.

At gate biasing $V_{\text{GI}}$ above the threshold voltage $V_T$, $V_{\text{GTS}} \approx (V_{\text{GI}}-V_T-V_{\text{SI}})$ and $V_{\text{GTD}} \approx (V_{\text{GI}}-V_T-V_{\text{DI}})$, because $(V_{\text{GI}}-V_T-V_{\text{SI}})/V_{\text{SS}}>>1$ and $(V_{\text{GI}}-V_T-V_{\text{DI}})/V_{\text{SS}}>>1$, since $\ln(1+\exp(x)) \approx x$ for $x>>1$ in eq. (3). Consequently, for the linear regime of operation of the TFT, $V_{\text{DS,}}=V_{\text{DI}}-V_{\text{SI}}<<V_{\text{GTD}}<V_{\text{GTS}}$, and the expression in the curly brackets of eq. (2) reduces to

$$\left\{ \frac{(V_{\text{GTS}})^{(2+\gamma)} - (V_{\text{GTD}})^{(2+\gamma)}}{2 + \gamma} \right\} \approx (V_{\text{GTS}} - V_T)^{(1+\gamma)} V_{\text{DS,}}$$

for linear regime

(4)

This equation shows the effect of the mobility enhancement factor gamma ($\gamma>0$). The TFT current is a power-law function of the gate bias, $I_{\text{DS,}} \propto (V_{\text{GS}} - V_{\text{T}})^{(1+\gamma)}$ in presence of bias enhancement of mobility, instead of being a linear function. Similarly, for the saturation regime $V_{\text{GTS}}>>V_{\text{GTD}} \approx 0$, the expression in the curly brackets of eq. (2) reduces to

$$\left\{ \frac{(V_{\text{GTS}})^{(2+\gamma)} - (V_{\text{GTD}} \approx 0)^{(2+\gamma)}}{2 + \gamma} \right\} \approx \frac{(V_{\text{GTS}} - V_T)^{(2+\gamma)}}{2 + \gamma},$$

for saturation regime

(5)

so that in presence of mobility enhancement ($\gamma>0$), the TFT current is again a power-law function of the gate bias, $I_{\text{DS,}} \propto (V_{\text{GS}} - V_{\text{T}})^{(2+\gamma)}$ that it is “steeper” than the quadratic function established for field-effect transistors with constant mobility ($\gamma=0$).

In the sub-threshold regime, the overdrive voltages are exponential functions of the gate bias, because np$(V_{\text{GI}}-V_T-V_{\text{DI}})/V_{\text{SS}} \ll \text{np}(V_{\text{GI}}-V_T-V_{\text{SI}})/V_{\text{SS}}<<-1$ when np$(V_{\text{DI}}-V_{\text{SI}})>>V_{\text{SS}}$. Since $\ln(1+\exp(x)) \approx \exp(x)$ for $x<<-1$, then from eq. (3) $V_{\text{GTD}}<<V_{\text{GTS}} \propto V_{\text{SS}} \exp[\text{np}(V_{\text{GI}}-V_T-V_{\text{SI}})/V_{\text{SS}}]$, and the expression in the curly brackets of eq. (2) reduces to

$$\left\{ \frac{(V_{\text{GTS}})^{(2+\gamma)} - (V_{\text{GTD}} \ll V_{\text{GTS}})^{(2+\gamma)}}{2 + \gamma} \right\} \propto \exp \left[ \frac{V_{\text{GI}}}{V_{\text{SS}}/(2 + \gamma)} \right],$$

for sub-threshold regime

(6)
<table>
<thead>
<tr>
<th>No.</th>
<th>Model Parameter</th>
<th>Notation</th>
<th>Unit or [value]</th>
<th>Default value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>oTFT model version</td>
<td>version_oTFT</td>
<td>numeric</td>
<td>2.0401</td>
<td>oTFT model version = 2.04.01. Unused in the code.</td>
</tr>
<tr>
<td>2</td>
<td>Type of TFT</td>
<td>np</td>
<td>[-1, +1]</td>
<td>+1</td>
<td>TFT polarity, np=(+1)= n-type TFT, np=(−1)=p-type TFT</td>
</tr>
<tr>
<td>3</td>
<td>Channel width</td>
<td>W</td>
<td>m</td>
<td>100 µm</td>
<td>Channel size perpendicular to the current flow</td>
</tr>
<tr>
<td>4</td>
<td>Channel length</td>
<td>L</td>
<td>m</td>
<td>10 µm</td>
<td>Channel size collinear with the current flow</td>
</tr>
<tr>
<td>5</td>
<td>Gate dielectric capacitance per area</td>
<td>C_l</td>
<td>F/m²</td>
<td>350 µF/m²</td>
<td>Default value is 35nF/cm² and corresponds to SiO₂ of thickness d=100nm and dielectric constant ε=3.9</td>
</tr>
<tr>
<td>6</td>
<td>Threshold voltage</td>
<td>V_T</td>
<td>V</td>
<td>0 V</td>
<td>The value is extrapolated from above-threshold regime of operation of the TFT</td>
</tr>
<tr>
<td>7</td>
<td>Low-field mobility</td>
<td>µ_o</td>
<td>m²/Vs</td>
<td>10⁻⁵</td>
<td>The value corresponds to overdrive (V_G−V_T)=V_γ. Default value is 0.1cm²/Vs for OTFTs</td>
</tr>
<tr>
<td>8</td>
<td>Mobility enhancement factor</td>
<td>γ (gamma)</td>
<td>numeric</td>
<td>0.6</td>
<td>The actual mobility is $\mu=\mu_o\times(V_G−V_T)/V_\gamma$. Temperature dependence $(2+\gamma)=2T_0/T$ with $T_0\approx400K$ for OTFTs, is not implemented in oTFT 2.04.01 compact model.</td>
</tr>
<tr>
<td>9</td>
<td>Voltage override for µ_o</td>
<td>V_T</td>
<td>V</td>
<td>1 V</td>
<td>The value corresponds to overdrive (V_G−V_T)=V_T, for which the value of µ_o is given.</td>
</tr>
<tr>
<td>10</td>
<td>Subthreshold slope voltage</td>
<td>V_SS</td>
<td>V</td>
<td>1 V</td>
<td>For asymptotic interpolation of the overdrives $V_{GTS}$. With $V_\gamma=[V_{DI},V_{SI}]$, $V_{GTS}=V_SS\times\ln{1+\exp[\text{np}×(V_G−V_T)/V_SS]}$.</td>
</tr>
<tr>
<td>11</td>
<td>Minimum (contact) resistance of terminal</td>
<td>R_C</td>
<td>Ω</td>
<td>100 kΩ</td>
<td>Should obey 1/W scaling, but R_C is implemented as absolute value</td>
</tr>
<tr>
<td>12</td>
<td>Maximum (contact) resistance of terminal</td>
<td>R_Cmax</td>
<td>Ω</td>
<td>300 kΩ</td>
<td>The maximum resistance of a terminal is $(R_C+R_Cmax)$ at low current &lt;I_Cmax. Typically R_Cmax~3R_C for OTFTs.</td>
</tr>
<tr>
<td>13</td>
<td>Max current for R_Cmax</td>
<td>I_Cmax</td>
<td>A</td>
<td>1 nA</td>
<td>The actual contact resistance is given by $R_C+R_Cmax[I_Cmax/(I_Cmax+</td>
</tr>
<tr>
<td>14</td>
<td>Reduction exponent for R_Cmax</td>
<td>nC</td>
<td>numeric</td>
<td>0.75</td>
<td>Meaningful values for nC are between 0.5 (SCLC) and 1 (constant voltage drop at contact)</td>
</tr>
<tr>
<td>15</td>
<td>Resistance of the gate conductor</td>
<td>R_Gmin</td>
<td>Ω</td>
<td>1 Ω</td>
<td>The gate resistance is insignificant for OTFT. R_Gmin is introduced for compatibility and tune-up of AC response.</td>
</tr>
<tr>
<td>16</td>
<td>Selector for Channel Modulation</td>
<td>selectQS</td>
<td>[0,1]</td>
<td>1</td>
<td>nSCLC=4 selects channel modulation due to fringing capacitance at semiconducting film’s “back” of the. Other possible models are not implemented in oTFT 2.04.01.</td>
</tr>
<tr>
<td>17</td>
<td>Relative permittivity at film’s “back” (for channel modulation)</td>
<td>eB (eB)</td>
<td>numeric</td>
<td>2</td>
<td>Effective value of the dielectric constant of the medium at the “back” of the semiconducting film (for channel modulation). Typically for oTFT, eB=2.</td>
</tr>
<tr>
<td>18</td>
<td>Relative permittivity at film’s “back” (for channel leakage)</td>
<td>eBleak</td>
<td>numeric</td>
<td>0.5</td>
<td>Effective value of the dielectric constant of the medium at the “back” of the semiconducting film (for channel leakage). Typically $e_{Bleak}=e_B/4$ for oTFT.</td>
</tr>
<tr>
<td>19</td>
<td>Threshold voltage for non-linear leakage</td>
<td>V_TL</td>
<td>V</td>
<td>0 V</td>
<td>V_TL should have value close to the value of the TFT threshold voltage V_T (V_T is for the “front” of the film, interfacing with the gate dielectric).</td>
</tr>
<tr>
<td>20</td>
<td>Sheet resistance of the bulk of the semiconducting film</td>
<td>R_BS</td>
<td>Ω/□</td>
<td>10¹²Ω/□ (10¹⁰Ω/□)</td>
<td>For linear (Ohmic) leakage due to conduction in the bulk of semiconducting film. “Leaky” OTFTs can have low value for R_BS~10MΩ/□. The TFT bulk resistance is R_BS×L/W.</td>
</tr>
<tr>
<td>21</td>
<td>Selector for quasi-static model</td>
<td>selectQS</td>
<td>[0,1]</td>
<td>1</td>
<td>selectQS=0 suppresses the quasi-static capacitances. The quasi-static charges are still calculated. selectQS=1 selects quasi-static model with fixed gate capacitance $C_{G0}=WLC_0$, by using literal formula for $C_{G0}$ in oTFT 2.04.01 model.</td>
</tr>
<tr>
<td>22</td>
<td>Drain/source length overlapping the gate</td>
<td>L_OV</td>
<td>m</td>
<td>30 µm</td>
<td>Geometrical overlap of gate conductor with drain/source contact pad. Used in literal formula $C_{OV}=C_{G0}×W×L_OV$ for overlap capacitance $C_{OV}$ between gate and drain/source. $C_{OV}$ is the dominant capacitance in OTFT.</td>
</tr>
<tr>
<td>23</td>
<td>Relative permittivity at film’s “back” (for geometric capacitance)</td>
<td>eBov</td>
<td>numeric</td>
<td>1</td>
<td>Dielectric constant at film’s “back” for geometric capacitance $C_{DSOV}$ between drain and source. Typically $e_{Bov}=e_B/2$ for oTFT. $C_{DSOV}$ is negligible in TFT, and implemented as literal formula for the upper limit.</td>
</tr>
<tr>
<td>24</td>
<td>Minimum non-zero voltage difference</td>
<td>V_min</td>
<td>V</td>
<td>10 µV</td>
<td>Prevents from division by zero. (2-4) × simulator absolute tolerance for voltage. Literal constant in oTFT 2.04.01.</td>
</tr>
</tbody>
</table>
Therefore, the TFT current exponentially decreases, when lowering the gate bias in the sub-threshold regime of operation of the TFT, and the sub-threshold slope voltage parameter $V_{SS}$ determines the steepness of the exponential decrease in the oTFT models. The sub-threshold slope $SS$ of the exponential reduction is usually reported in unit [V/dec]. The relation between $V_{SS}$ and $SS$ is [1]

$$V_{SS}[V] = \frac{\partial V_g}{\partial (\ln(I_D))} \approx 0.43(2 + \gamma)SS[V/\text{dec}] \approx SS = \frac{\partial V_g}{\partial (\log_{10}(I_D))}, \text{ for } \gamma \approx 0.33 \quad (7)$$

Typical values for sub-threshold slope voltage in OTFT are $V_{SS} \sim 1V$.

Regarding scaling rules in the model parameters, the models for crystalline field-effect transistors and inorganic TFT suggest $V_{SS} = 2kT/q \sim 52\text{mV}$, $C_t = \varepsilon_r \varepsilon_o / t_I$ and $\gamma = 2T_o / T - 2$, where $k$ is Boltzmann constant, $T$ is absolute temperature, $\varepsilon_o$ is permittivity of vacuum, $\varepsilon_r$ and $t_I$ are relative permittivity (dielectric constant $\varepsilon_r = 3.9$ for SiO$_2$) and thickness of gate oxide, and $T_o$ is characteristic temperature of the exponential distribution of density of states ($T_o \sim 400K$ for organic semiconductors). While these rules have physical significances, the oTFT models do not use the rules, because many factors cause pronounced deviations from the scaling rules, especially for organic TFTs. For example, $\mu_o$ varies with temperature, and $\gamma$ and $C_t$ vary between identical and simultaneously produced OTFTs. Also $V_{SS} \sim 1V$ is well beyond any meaningful interpretation of population of density of states by Fermi or Boltzmann statistics. Therefore, the model parameters are implemented without scaling rules and temperature dependences in the oTFT compact models, following the recommendation in [1] that the scaling rules should remain “external” for compact models of organic TFTs, since the rules are often obscured, owing to variations in materials, fabrication approaches, structures and poor reproducibility in organic TFTs. Thus, there is no temperature dependence implemented in the oTFT model, especially in the generic charge drift DC model, overdrive voltage model and in the following contact resistance model. One has to assign absolute values for the model parameters by instantiation of the oTFT model, reflecting geometrical and temperature effects in the values of the model parameters. For other sub-model, there are geometrical scaling rules adopted, since those models address impacts of lesser significance for organic TFTs.

Overall, the core of the generic TFT charge drift DC model with its sub-model for overdrive voltages is of critical importance in the oTFT compact model, because these models hold the behavioral consistency of the compact model, reflecting the two most significant physical phenomena in organic TFTs: charge drift and bias enhancement of mobility.

2.2. Contact model for contact resistances between terminal and intrinsic nodes

The contact model is important for the consistent modeling of the DC and other characteristics of the organic TFTs (OTFTs). The importance originates from accumulated experience that the contacts significantly reduce the currents in OTFTs – approximately half of the conduction ability of the organic semiconductors is “lost” in the contacts of the OTFT.

The contact sub-models connect the TFT device terminals (G,S,D) to the corresponding intrinsic nodes ($G_I,S_I,D_I$), as shown in Figure 5. The contact effects are significant between channel ends $S_I,D_I$ and terminals S,D. The gate resistance is of marginal significance for OTFTs. Appropriate characterization techniques for extraction the contact resistance characteristics and parameters are available in [2] for the saturation regime of operation of the OTFT and in [5] for the linear regime.
The contact sub-models in oTFT 2.04.01 compact model are two-terminal resistance models. Each model consists of two portions for linear and non-linear contact resistance. The characteristic equations of the sub-models for the contacts are [1]

\[ V_G - V_{Gi} = (R_{Gmin} + 0) \times I_{G,GI} \text{, for gate} \]

\[ V_S - V_{Si} = \left[ R_C + R_{Cmax} \times \left( \frac{I_{Cmax}}{I_{Cmax} + I_{S,SI}} \right)^{n_{IC}} \right] \times I_{S,SI} \text{, for source} \]

\[ V_D - V_{Di} = \left[ R_C + R_{Cmax} \times \left( \frac{I_{Cmax}}{I_{Cmax} + I_{D,DI}} \right)^{n_{IC}} \right] \times I_{D,DI} \text{, for drain} \]

where \( R_C \) is the minimum contact resistance and represents linear contact between terminal and channel, \( R_{Cmax} \) represents the elevation of the contact resistance at low current through the contact, \( I_{Cmax} \) is the maximum current, below which the contact tends to have resistance \((R_C + R_{Cmax})\), and the exponent \( n_{IC} \) describes the steepens of the transition from \((R_C + R_{Cmax})\) toward \( R_C \), when increasing the current through the contact above \( I_{Cmax} \). The current through the source contact is \( I_{S,SI} \), flowing from terminal S to intrinsic node SI. The current through the drain contact is \( I_{D,DI} \), flowing from terminal D to intrinsic node DI. The current through the gate contact is \( I_{G,GI} \), flowing from terminal G to intrinsic node GI. Gate leakages are usually low in OTFTs. Therefore, \( I_{G,GI} \approx 0 \), the gate contact is insignificant for DC, and the gate contact is modeled only as linear contact of resistance \( R_{Gmin} \), eventually to reflect a pole at high frequency. For the source and drain contacts in OTFTs, typical ratio is \( R_{Cmax}/R_C \sim 3 \) and \( I_{Cmax} \) is in the nanoampere range. For OTFTs with linear contacts, \( R_{Cmax} = 0 \), resulting in model with constant resistance \( R_C \). For non-linear contacts, the reduction exponent ranges from \( n_{IC} = 0.5 \) for space charge limited conduction (SCLC) to \( n_{IC} = 1 \) for built-in (constant) voltage drop across the contact. For OTFTs with non-linear contacts, \( n_{IC} \approx 0.75 \), indicating combined contribution from SCLC and built-in voltage.

While the literature suggests scaling rules for contacts in TFTs, the contact model and parameters are implemented in absolute values and without scaling in the oTFT compact model.
The reason is that many conducting and semiconducting materials are used for OTFTs, and the scaling rules for contacts are rarely reproducible even when the OTFTs are fabricated simultaneously on the same substrate.

Being two-terminal model, the contact model is implicit function of the gate bias with unique current-voltage (I−V) characteristic independent of the gate bias. On the other hand, the literature that uses TLM characterization techniques for contacts, often suggests gate bias dependence by ignoring the different currents by measuring TFTs with different channel lengths at same gate bias. Inspection of published data for non-linear contacts and modeling of experimental I−V curves form many publications [6] imply that the contacts in organic TFTs tend to have unique (gate bias-independent), but drain current-dependent characteristics. Therefore, the two-terminal model is implemented in the oTFT compact model. Nevertheless, one may decide using custom models for contacts, which requires to suppress the contact models in the oTFT compact model. The suppression can be accomplished by two ways. One way is to set low values for \( R_C \), e.g., \( R_C=1\Omega \), and zero value for \( R_{C\max}=0 \); and add the custom contact model connected in series with the terminal nodes D and S in the electrical circuit where the oTFT compact model is used. Second way is to set very high values for \( R_C=100T\Omega \), and connect the custom model between terminal and intrinsic nodes S−SI and D−DI. For DC simulations, both ways are equivalent. However, for transient and AC simulations, there might be differences acquired between the two ways. The reason is that the quasi-static charge model in the oTFT compact model is connected to the terminal nodes G, S and D, and adding impedance in series with the terminals (the 1\textsuperscript{st} way), there will be effects in the frequency response, e.g., poles will be introduced. These effects can be minimized, if using the second way of connecting the custom contact models between the terminal and intrinsic nodes S−SI and D−DI. Using the second way, the DC characteristics of the oTFT model will be modified by the custom contact model as desired, while the AC response will be weakly affected by the introduced custom model, as long as the overdrive voltages \( V_{GTS} \) and \( V_{GTD} \) are kept at the same given values. For the 2\textsuperscript{nd} way in particular, the static differential parameters (such as transconductance \( g_m \) and drain conductance \( g_d \)) will be affected by the custom contact model, but the quasi-static capacitances will be not affected (again, as long as the \( V_{GTS} \) and \( V_{GTD} \) are kept at the same given values).

2.3. Channel modulation model

The channel modulation in TFT addresses the elevation of the channel current with drain bias and the finite drain conductance \( g_d=\partial I_D/\partial V_D>0 \) between drain and source in the saturation regime of operation of the TFT, where the generic TFT charge drift model predicts constant saturation current \( I_{DS,sat} \) (independent of \( V_D \)) and zero drain conductance \( g_d=\partial I_D/\partial V_D=0 \). The channel modulation model is connected between the intrinsic nodes S,DI as shown in Figure 6. The channel modulation model is controlled by the potentials \( V_{GI}, V_{SI}, V_{DI} \) of the intrinsic nodes and the overdrive voltages \( V_{GTS}, V_{GTD} \).

The channel modulation can be treated by several ways, and a model parameter \( n_{SCLC} \) is present in the oTFT compact models for selection of the treatment [1]. Channel length modulation models are assigned to \( n_{SCLC}=[0,1] \). Space-charge limited conduction (SCLC) models are assigned to \( n_{SCLC}=[2,3] \). All these models use expressions with channel modulation parameter \( \lambda \), so that \( I_{DS}/I_{DS,sat}=1+\lambda(V_{DS}-V_{DS,sat}) \). These models are useful for DC modeling, but have problems with discontinuity of derivatives in the transition between linear and saturation regimes of operation of the TFT. Therefore, oTFT 2.04.01 compact model uses channel modulation sub-
model that is based on effects of fringing capacitance \( C_L \) at the “back” of the semiconducting film [3]. The drain bias induces extra charge \( \Delta Q_L \propto C_L \times V_D \) in the channel through the fringing capacitance \( C_L \) in a similar manner and in addition to the charge \( Q \propto C_I \times (V_G - V_T) \) induced by the gate bias through the gate capacitance \( C_I \) at the “front” of the semiconducting film. In the saturation regime, \( Q_{sat} \propto C_I \times (V_G - V_T) \) is independent of the drain bias, but the extra charge \( \Delta Q_L \) continues increasing with \( V_D \). Thus, the channel modulation due to fringing capacitance at the film’s “back” results in extra channel modulation current \( \Delta I_{DS} \propto \Delta Q_L \propto C_L \times V_D \). The channel modulation model due to fringing capacitance \( C_L \) at the “back” of the semiconducting film is assigned to \( n_{SCLC} = 4 \).

\[
\Delta I_{DS} = n_p \times K_{AID} \frac{V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma}}{2 + \gamma} \\
+ K_{AID} \left( \frac{V_{DI} + V_{SI}}{2} - (V_{GI} - V_T) \right) V_{GTS}^{1+\gamma} - V_{GTD}^{1+\gamma} \\
+ K_{AID} \frac{f_{AID}(V_{GTS}, V_{GTD}, \gamma)}{2(1 + \gamma)(3 + 2\gamma)} (V_{DI} - V_{SI})
\]

where the fringing capacitance constant \( K_{AID} \propto C_L \) and the function \( f_{AID}(V_{GTS}, V_{GTD}, \gamma) \) are.

Figure 6. Mapping of the sub-model for channel conductance modulation in saturation regime in the oTFT compact model. The control from \( V_G \) is not shown for clarity of the figure.

Derived in [3] by conformal mapping of planar capacitance between drain contact pad and channel, the expression for the unit-area capacitance \( C_L \) at the “back” of the semiconducting film is

\[
C_L = \frac{\varepsilon_B \varepsilon_0}{\pi L}
\]

where \( \varepsilon_B \) is the relative permittivity (dielectric constant) of the medium at the “back” of the semiconducting film. The notation in the Verilog-A code is \( \varepsilon_B \), and \( \varepsilon_B \sim 2 \) is a model parameter. Following the derivation procedures in [3], the expression for the channel modulation “extra” current by bias-enhanced mobility is derived in [6]
\[
K_{\text{AID}} = \frac{W}{L} 6C_l \mu_o \left[ \frac{V_{\gamma}^{3+2\gamma}}{V_{\gamma}^{1+\gamma}} - (3 + 2\gamma) V_{\gamma}^{2+\gamma} V_{\text{GTD}}^{1+\gamma} \right. + (3 + 2\gamma) V_{\gamma}^{2+\gamma} V_{\text{GTD}}^{1+\gamma} - V_{\gamma}^{2+\gamma} \left. \right]^{1+\gamma} \varepsilon_{\text{B}} + \left[ (1 + \text{num}) V_{\text{min}} \right]^{2+\gamma},
\]

respectively. The small voltage \([(1 + \text{num}) V_{\text{min}}] \approx 10^{-50}\mu\text{V} > 0\) is added to avoid division on zero in numerical simulators. Note that \(f_{\text{AID}}\) is in unit \([V^{1+\gamma}]\) and the fringing capacitance \(6C_l\) serves in the fringing capacitance constant \(K_{\text{AID}}\), as \(C_l\) serves in the TFT device constant in the square brackets in eq. (2).

Thus, the channel modulation current \(\Delta I_{DS} \approx K_{\text{AID}} \approx C_l \approx \varepsilon_\text{B} / L\) is reciprocal of the channel length \(L\) and proportional to the relative permittivity \(\varepsilon_\text{B}\) (dielectric constant) of the medium at the “back” of the TFT film. The order of magnitude for \(\varepsilon_\text{B}\) is \(\varepsilon_\text{B} \approx 2^{-3}\), considering finite thickness of the semiconducting film and encapsulation of the TFT. Thus, one adjusts the elevation of the drain current due to channel modulation at high drain bias, by adjusting the value of the model parameter \(\varepsilon_\text{B} \approx \varepsilon_\text{B}^{\text{sat}}\). If one sets \(\varepsilon_\text{B}=0\), then \(\Delta I_{DS}=0\) and the channel modulation is suppressed in the oTFT compact model.

While accurate and with smooth derivatives, eq. (10) is quite bulky. Therefore, three variables (numerator, denominator and \(f_{\Delta I_{ID}}\)) are used to perform the calculation in steps, and the three lines in eq. (10) correspond to the three accumulation statements in the analog processing section in the Verilog-A code. Nevertheless, although bulky in the region of the linear regime of operation of the TFT, eq. (10) simplifies in the saturation regime, since \(V_{\text{GTD}} \approx 0\) is negligible in the saturation regime. The reduced eq. (10) in the saturation regime is

\[
\Delta I_{DS,\text{sat}} = n p \times K_{\text{AID}} V_{\gamma}^{2+\gamma} \left( \frac{1}{2+\gamma} - \frac{1}{1+\gamma} \right) + K_{\text{AID}} \left( \frac{2+\gamma}{(1+\gamma)(3+2\gamma)} \right) V_{\gamma}^{1+\gamma} V_{\gamma}^{2+\gamma} V_{DS}
\]

\[
\downarrow
\]

\[
\frac{\partial (\Delta I_{DS,\text{sat}})}{\partial V_{DS}} = \frac{\partial (I_{DS,\text{sat}})}{\partial V_{DS}} = g_{d,\text{sat}} = \frac{(2+\gamma) V_{\gamma}^{1+\gamma} V_{\text{GTD}}^{1+\gamma}}{(1+\gamma)(3+2\gamma)} \pi L \frac{\varepsilon_\text{B} \varepsilon_0}{V_{\gamma}^{2+\gamma}} \mu_o
\]

\[
\downarrow \text{by dividing on TFT saturation current } I_{DS,\text{sat}} = K_{\text{TFT}} V_{\gamma}^{2+\gamma} / (2+\gamma)
\]

\[
\frac{\partial \ln (I_{DS,\text{sat}})}{\partial V_{DS}} = \frac{g_{d,\text{sat}}}{I_{DS,\text{sat}}} = \frac{6(2+\gamma)^2}{\pi (1+\gamma)(3+2\gamma)} \times \frac{\varepsilon_\text{B} \varepsilon_0}{C_1 V_{\gamma}^{1+\gamma} L} \approx \frac{2\varepsilon_\text{B} \varepsilon_0}{C_1 V_{\text{GTD}}^{1+\gamma} L} \text{ for } \gamma \approx 0.6
\]

\[
\downarrow
\]

\[
\frac{\partial \ln (I_{DS,\text{sat}})}{\partial V_{DS}} = \frac{g_{d,\text{sat}}}{I_{DS,\text{sat}}} \approx \frac{2\varepsilon_\text{B} \varepsilon_0}{C_1 V_{\gamma}^{1+\gamma} L} \approx \frac{2\varepsilon_\text{B} d_i}{e_i V_{\text{GTD}} L} \text{ for } e_i \approx 4
\]

where \(g_{d} = \partial I_{DS} / \partial V_{DS}\) is the drain conductance of the OTFT, \(e_i \approx 4\) is the relative permittivity (dielectric constant) of the gate dielectric and \(d_i\) is the thickness of the gate dielectric.

In the last line of eq. (12), the quantity \(\partial \ln (I_{DS,\text{sat}}) / \partial V_{DS}\) is the channel modulation parameter, denoted in other models with \(\lambda = \Delta L / L\), where \(\Delta L (V_{DS,\text{sat}} = (V_{GS} - V_T))\) is the modulation of the channel length at high drain bias in the saturation regime of operation of the TFT, \(V_{DS,\text{sat}} = (V_{GS} - V_T)\). No channel length modulation in used in the oTFT model, because fringing capacitance is used. Nevertheless, and to provide relation to the model parameters of other models and characterization techniques, the following relations for channel modulation hold.
\[
\frac{2\varepsilon_B d_t}{\varepsilon_s V_{GTS} L} \approx \frac{\varepsilon_B d_t}{2(V_{GS} - V_T) L} = \frac{g_{d,\text{sat}}}{I_{DS,\text{sat}}} \text{, with } \varepsilon_s \approx 4 \text{ and } V_{DS} > (V_{GS} - V_T) \\
\frac{\partial \ln(I_{DS,\text{sat}})}{\partial V_{DS}} = \frac{\Delta L}{L} = \lambda = \frac{1}{V_{\text{Early}}}
\]

where \(V_{\text{Early}} = 1/\lambda\) was denoted as Early voltage sometimes ago. Eq. (13) indicates that the channel modulation \(\Delta I_{DS,\text{sat}}/\Delta V_{DS}/I_{DS,\text{sat}} = g_{d,\text{sat}}/I_{DS,\text{sat}}\) (slope of the \(I_D-V_D\) curve or drain conductance \(g_d\) in ratio to the saturation current) in the oTFT model is inversely proportional to the channel length and gate biasing. If the reciprocal dependence of the channel modulation on the gate bias is not present in the experimental data for oTFT, then one should set the model parameter \(\varepsilon_B = 0\) to suppress the channel modulation in the oTFT model, and add custom model between the drain and source terminals of the TFT in the electrical circuit where the oTFT model is used. Alternatively, one can manipulate the leakage sub-model in the oTFT model, which also causes elevation of the drain current as function of the drain bias.

2.4. Channel leakage model

The channel leakage model addresses the leakage current between drain and source, which can be significant at low gate biasing of the TFT. The channel leakage is defined in the oTFT compact model as drain to source current \(I_{\text{leak}}\) independent of gate bias. The channel leakage depends only on the drain-source bias. Therefore, leakage model is connected only to the OTFT terminal nodes D and S, as shown in Figure 7 to calculate the leakage current \(I_{\text{leak}}\) between these nodes. There is no problem to connect the channel leakage model between the internal nodes \(D_i\) and \(S_i\), but this connection is commented in the Verilog-A code of the oTFT 2.04.01 compact model, since one can have only one leakage model at a time, and because the leakage is small to cause significant voltage drop on the terminal resistances that are between nodes D-\(D_i\) and S-\(S_i\).

Figure 7. Mapping of the sub-model for leakage in the oTFT compact model

Two types of leakage are considered in the channel leakage model. One type is linear (Ohmic) leakage with linear dependence between drain-source bias voltage \(V_{DS}\) and leakage current
The Ohmic leakage is implemented with W/L scaling rule in the analog processing section of the Verilog-A code as

\[
I_{\text{leak,Ohmic}} = \frac{V_{DS}}{R_{BS}} \times \frac{W}{L}
\]  

where \( R_{BS} \) is the sheet resistance of the bulk of semiconducting film at no gate biasing. For OTFTs, the semiconducting film bulk sheet resistance is typically \( R_{BS} \sim 10^{13} \Omega/\square \sim 10T \Omega/\square \). The actual resistance of the bulk of the semiconducting film increases with the channel length \( L \) and decreases with the channel width \( W \), resulting in the term \( W/L \) in eq. (14). For example, having an OTFT with aspect ratio \( W/L=10 \), the bulk resistance is \( R_{BS}/10=1T \Omega \), and biasing the drain at \( V_{DS}=10V \), then the Ohmic leakage is \( I_{\text{leak,Ohmic}}=10V/1T \Omega=10pA \). Some OTFTs are “very leaky”, and \( R_{BS} \) may be much lower for these leaky OTFTs, e.g., in the range of \( R_{BS} \sim 10^7 \Omega/\square = 10M \Omega/\square \).

The second type of leakage is non-linear, e.g., with quadratic dependence of \( I_\text{leak} \propto (V_{DS})^2 \), if considering space-charge limited conduction in the semiconductor film bulk. Similarly to the channel modulation, the non-linear leakage in the OTFT model is based on effects of fringing capacitance at the “back” of the semiconducting film. (The “front” of the semiconducting film is the interface with the gate dielectric.) It has been shown in [3] that the drain bias induces charge in the semiconductor film through the fringing capacitance \( 6C_L \) in a way as the gate bias induces charge through the gate dielectric capacitance \( C_I \). Thus, there is an extra leakage TFT diode between D and S, with gate connected to drain, and another leakage TFT diode between S and D with gate connected to source, the latter for the case when drain and source are swapped. (The TFT is symmetric structure; not discriminating which of the channel ends is drain and which is source.) Therefore, the non-linear leakage is calculated by two instantiations of the generic TFT charge drift DC model with gate capacitance \( 6C_{LL} \), instead of \( C_I \), and eventually with threshold voltage \( V_{TL} \) instead of \( V_T \), since the threshold for the non-linear leakage at the “back” of the semiconducting film might be different from the threshold voltage \( V_T \) in the “front” of the semiconducting film, although theoretically \( V_T \) and \( V_{TL} \) should be the same and both close to zero for OTFTs. Eq. (15) for \( C_{LL} \) is identical to eq. (9) for \( C_I \) in the channel modulation model,

\[
C_{LL} = \frac{\varepsilon_{\text{Bleak}} \varepsilon_0}{\pi L}
\]

just another parameter \( \varepsilon_{\text{Bleak}} \sim 0.5 \) is used for the is the relative permittivity (dielectric constant) of the medium at the “back” of the semiconducting film, because, typically for OTFTs, \( \varepsilon_{\text{Bleak}} \sim \varepsilon_B/4 \). The notation for \( \varepsilon_{\text{Bleak}} \) is \( \varepsilon_{\text{Bleak}} \) in the Verilog-A code of the OTFT 2.04.01 compact model.

Thus, adding the Ohmic leakage from eq. (14) to the two leakage diodes, the channel leakage current flowing from drain to source terminals in the OTFT compact model is calculated as

\[
I_{\text{leak}}(D,S) = \left( \frac{V_D - V_S}{R_{BS}} \right) \frac{W}{L}, \text{ for Ohmic leakage}
\]

\[
+ np \times \frac{W}{L} 6C_{LL} \mu_0 \left( \frac{1}{V_T} \right)^\gamma \frac{V_{2+\gamma}^{D,S} - V_{2+\gamma}^{D,T} \left( \frac{V_D}{V_T} \right)^\gamma}{2+\gamma}, \text{ for the forward leakage diode}
\]

\[
+ np \times \frac{W}{L} 6C_{LL} \mu_0 \left( \frac{1}{V_T} \right)^\gamma \frac{V_{2+\gamma}^{S,T} - V_{2+\gamma}^{S,D} \left( \frac{V_S}{V_T} \right)^\gamma}{2+\gamma}, \text{ for the reverse leakage diode}
\]
where, for a normal (forward) polarity of biasing \( np \times (V_D - V_{TL} - V_s) > V_{SS} \) and \( np \times (V_D - V_s) > 0 \),
for the forward diode \( V_{DTS} \approx np \times (V_D - V_{TL} - V_s) > V_{SS} \)
\[ V_{DTS} = EODR (-np \times V_{TL}) < V_{SS} \], and
for the reverse diode \( V_{STS} \approx EODR (-np \times V_{TL}) < V_{SS} \)
\[ V_{STD} = EODR (np \times (V_s - V_{TL} - V_D)) \approx 0. \]
As follows from eq. (16), one can increase the Ohmic leakage by reducing \( R_{BS} \) and increase the non-linear leakage by reducing \( np \times V_{TL} \) and increasing \( \varepsilon_{Bleak} \). Such manipulation can be useful to outsource the channel modulation into the leakage sub-model of the oTFT compact model, although it is not recommended. In contrary, one can suppress the Ohmic and/or non-linear leakage in the oTFT model by increasing \( R_{BS} \) to very large number, e.g., \( R_{BS} > 10^{30} \Omega/\square \) and/or setting \( \varepsilon_{Bleak} = 0 \). Once the leakage is suppressed in the oTFT model, then a custom model for leakage can be added between the drain and source terminals of the TFT in the electrical circuit where the oTFT compact model is used.

2.5. Quasi-static charge model

The quasi-static charge model calculates the amounts of charge in the semiconducting film and gate, as seen from the TFT terminal nodes and as function of the bias potentials \( V_G, V_S, V_D \) of the TFT. Thus, as shown in Figure 8, the quasi-static charges \( Q_G, Q_S, Q_D \) correspond to the TFT terminals G,S,D, respectively, and the DC parameters and characteristics of the oTFT fully determine the quasi-static charges [4]. Accordingly, the time derivatives of \( \partial Q_G / \partial t, \partial Q_S / \partial t, \partial Q_D / \partial t \) correspond to capacitive currents \( i_G, i_S, i_D \) in the TFT terminals G,S,D, and voltage derivatives \( \partial Q_G / \partial V(G,S,D), \partial Q_S / \partial V(G,S,D), \partial Q_D / \partial V(G,S,D) \) correspond to quasi-static capacitances of or between the terminals. The matrix of quasi-static capacitances [4] is not necessary for performing of AC and transient analyses in computer simulators. Therefore, expressions for quasi-static capacitances are not implemented in the Verilog-A code, although the values of the capacitances can be calculated during AC simulation and are numerically available in parts for routing to test terminals in the monitoring section of the code.

Figure 8. Mapping of the quasi-static charge sub-model in the oTFT compact model
The expressions of the quasi-static charges have been derived in [4]. Obeying the charge conservation principle, the gate charge \( Q_G \) is inverted sum \(-(Q_S + Q_D)\) of the source and drain charges \( Q_S, Q_D \). Therefore, the expression for the gate quasi-static charge \( Q_G \) is

\[
Q_G = -Q_S - Q_D = np \times (+C_{G0}) \times \left( \frac{2 + \gamma}{3 + \gamma} \right) \frac{V_{GTS}^{3+2\gamma} - V_{GTD}^{3+2\gamma}}{V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma}}
\]

where \( C_{G0} = W \times L \times C_I \) is the gate dielectric capacitance over the entire area of the TFT channel. The quasi-static charge \( Q_S \) of the source is given by

\[
Q_S = np \times (-C_{G0}) \times \left( \frac{2 + \gamma}{3 + \gamma} \right) \frac{V_{GTS}^{5+2\gamma} - V_{GTD}^{5+2\gamma}}{V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma}}
\]

and the quasi-static charge \( Q_D \) of the drain is given by

\[
Q_D = np \times (-C_{G0}) \times \left( \frac{2 + \gamma}{3 + \gamma} \right) \frac{V_{GTS}^{5+2\gamma} - V_{GTD}^{5+2\gamma}}{V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma}}
\]

However, the direct use of the expressions in eqs. (18) and (19) meets with two problems by numerical calculations. One problem is that \( V_{GTS} \) and \( V_{GTD} \) can be within wide range of 5–6 decades, e.g., from less than a millivolt to hundreds of volts, and the exponentiation with \( (2+\gamma) \), \( (3+\gamma) \) and \( (5+2\gamma) \) expands the numerical ranges up to the numerical truncation, which is in the order of 16 decimal digits for calculations with double precision in the computer simulators. Consequently, the differences in the numerators and denominators become vulnerable to the numerical quantization, and the derivatives, e.g., for currents and capacitances, become inaccurate, when calculated by finite differences in the simulators. Therefore, it is necessary to rearrange the equations in normalized format. Appropriate normalization can be achieved defining normalized overdrive voltages, given by [6]

\[
\xi_S = \frac{V_{GTS}}{V_{GTS} + V_{GTD}} \Leftrightarrow V_{GTS} = \xi_S (V_{GTS} + V_{GTD}) \begin{cases} \xi_S + \xi_D \equiv 1 \\ 0 \leq \xi_S \leq 1 \\ 0 \leq \xi_D \leq 1 \end{cases}
\]

\[
\xi_D = \frac{V_{GTD}}{V_{GTS} + V_{GTD}} \Leftrightarrow V_{GTD} = \xi_D (V_{GTS} + V_{GTD}) \begin{cases} \xi_S V_{GTD} = \xi_D V_{GTS} \end{cases}
\]

The normalized overdrive voltages \( \xi_S \) and \( \xi_D \) are denoted with ksiS and ksiD in the Verilog-A code.

Substituting \( V_{GTS} \) and \( V_{GTD} \) by means of \( \xi_S \) and \( \xi_D \), and after cancelling terms \( (V_{GTS} + V_{GTD}) \) in numerators and denominators, then the normalized generic quasi-static charge model of the TFT becomes as

\[
Q_G = -Q_D - Q_S = np \times (+C_{G0}) \times (V_{GTS} + V_{GTD}) \times \left( \frac{\xi_S^{3+\gamma} - \xi_D^{3+\gamma}}{(3+\gamma)\left[\frac{\xi_S^{3+\gamma} - \xi_D^{3+\gamma}}{(2+\gamma)\left[\xi_S^{3+\gamma} - \xi_D^{3+\gamma}}\right]\right]}\right)
\]

\[
Q_D = np \times (-C_{G0}) \times (V_{GTS} + V_{GTD}) \frac{\text{num}_D}{\text{den}}
\]

\[
Q_S = np \times (-C_{G0}) \times (V_{GTS} + V_{GTD}) \frac{\text{num}_S}{\text{den}}
\]

where the functions in the numerators and denominators are
\[
\text{den} = \left( \frac{\xi_{2+\gamma}^{2+\gamma}}{2+\gamma} - \frac{\xi_{2+\gamma}^{2+\gamma}}{2+\gamma} \right)^{2} \frac{1}{[2+\gamma]^{2}}
\]

\[
\text{num}_{S} = \frac{1}{2+\gamma} \left( \frac{\xi_{3+\gamma}^{5+2\gamma}}{3+\gamma} \right) \left( \frac{\xi_{2+\gamma}^{2+\gamma}}{2+\gamma} \right) + \frac{1}{3+\gamma} \left( \frac{\xi_{2+\gamma}^{5+2\gamma}}{5+2\gamma} \right) < \frac{1}{[2+\gamma]^{2}}
\]

\[
\text{num}_{D} = \frac{1}{3+\gamma} \left( \frac{\xi_{3+\gamma}^{5+2\gamma}}{5+2\gamma} \right) - \frac{1}{2+\gamma} \left( \frac{\xi_{2+\gamma}^{2+\gamma}}{2+\gamma} \right) + \frac{1}{2+\gamma} \left( \frac{\xi_{2+\gamma}^{5+2\gamma}}{5+2\gamma} \right) < \frac{1}{[2+\gamma]^{2}}
\]

These functions in eq. (22) are denoted accordingly with \(\text{den}, \text{num}_S, \text{num}_D\) in the Verilog-A code. The functions \(\text{den}, \text{num}_S, \text{num}_D\) are smaller than unity, but not very small. These functions are in the unity order of 0.1 to 0.2, if \(V_D \neq V_S\), when either \(V_{GTS} \gg V_{GTD}\) or \(V_{GTS} \ll V_{GTD}\), irrespectively whether the actual voltages are small (mV) or large (kV). Thus, the expressions in eq. (22) are normalized for numerically accurate calculation of differences without truncation; and the charges are mainly proportional to the larger of the overdrive voltages \(V_{GTS}\) or \(V_{GTD}\), via the multiplier \((V_{GTS}+V_{GTD})\) in the previous eq. (21), which does not compromise the accuracy of the numerical calculation, since the multiplications are not vulnerable to numerical truncations. Observe also that the expressions in the round brackets in eq. (22) are reduced power-law functions.

\[
\frac{\xi_{i}^{n}}{n^{n}} \leq \frac{1}{n^{2}} \leq 1, \quad n \geq 2 \Rightarrow \text{limited derivatives: } \frac{\partial (\xi_{i}^{n})}{\partial \xi_{i}} = \xi_{i}^{n-1} \leq 1
\]

with \(i=D\) or \(i=S\) and \(n=(2+\gamma), (3+\gamma), \text{ or } (5+2\gamma)\); thus, \(n \geq 2\) in the normalized generic quasi-static charge model of the TFT, and the derivatives are also first “normalized” within unity for correct numerical subtraction without experiencing numerical quantization; and then the result is scaled with \((V_{GTS}+V_{GTD})\), using the chain rule, which performs multiplication, thus, it is not vulnerable to numerical quantization by floating point calculations. Thus, the time derivatives of \(\partial Q_{G}/\partial t, \partial Q_{S}/\partial t, \partial Q_{D}/\partial t\) quasi-static charges used for calculation of the capacitive currents \(i_{G, S, D}\) in the TFT terminals G,S,D are also not vulnerable to numerical quantization by floating point calculations.

The second problem in the TFT quasi-static charge model by numerical calculations is the division by zero in eqs. eqs. (18) and (19) and (21), when \(V_D=V_S\) and \(V_{GTS}=V_{GTD}\). The circuit simulators, such as SPICE, usually output zero by division on zero. The detailed analyses \([4],[6]\), both analytically by the L’Hospital rule and numerically by extrapolation of slopes, indicated that the expressions for the charges and their derivatives for capacitance have finite limits at \(V_D=V_S\). The normalization by eq. (22) allowed determining that the numerical problems by double precision calculations occur when the values of den, nums and numd correspond to about a ppm (part per million), or equivalently, 1–10 \(\mu V\), when \(V_{GTS}\) and \(V_{GTD}\) are in the range of tenths to tens of volts. Thus, one needs to “patch” the expressions, adding proportional parts in the numerators and denominators, which are negligible when \(|V_{GTS}-V_{GTD}|>1mV\), but take over when \(|V_{GTS}-V_{GTD}|<0.1mV\). It was found in \([6]\) that the following arrangement is accurate for the charge magnitude and its first derivatives for capacitances at \(V_D=V_S\) and \(|V_{GTS}-V_{GTD}|>1mV\), with errors not exceeding 0.1% at \(|V_{GTS}-V_{GTD}|<1mV\) and not compromising the monotonic behavior of charge and capacitance characteristics, but with some undulations in the first derivative, owing to the inaccurate second derivative that tends to zero in the same range \(|V_{GTS}-V_{GTD}|<1mV\).
Thus, the arrangement of the normalized generic quasi-static charge model of the TFT for computer simulators in the Verilog-A code became as follows. Firstly, the normalized overdrive voltages $\xi_S$ and $\xi_D$ are made non-zero, calculating by

$$
\xi_S = \frac{\sqrt{V_{GTS}^2 + V_{\text{min}}^2}}{\sqrt{V_{GTS}^2 + V_{\text{min}}^2 + \sqrt{V_{GTD}^2 + V_{\text{min}}^2}}} > 0 \text{ and } \xi_D = \frac{\sqrt{V_{GTD}^2 + V_{\text{min}}^2}}{\sqrt{V_{GTS}^2 + V_{\text{min}}^2 + \sqrt{V_{GTD}^2 + V_{\text{min}}^2}}} > 0,
$$

with $V_{\text{min}} = 10 \mu V$

since it is numerically possible that a biasing deep in the subthreshold regime may cause $V_{GTS}=0$ and $V_{GTD}=0$, due to the exponential functions in eq. (3) for overdrive voltages. Zero $V_{GTS}$ and $V_{GTD}$ would cause division by zero, if using eq. (20) for calculation of $\xi_S$ and $\xi_D$. No problem with zeros in (24), because $V_{\text{min}}>0$.

Secondly, the denominator and numerator functions are calculated as defined in eq. (22), by

$$
den = \left[ \frac{\xi_S^{2+\gamma}}{2+\gamma} - \left( \frac{\xi_D^{2+\gamma}}{2+\gamma} \right)^2 \right],
$$

$$
um_s = \frac{1}{2+\gamma} \left( \frac{\xi_{S}^{5+2\gamma}}{5+2\gamma} - \frac{\xi_{S}^{2+\gamma}}{2+\gamma} \right) + \frac{1}{3+\gamma} \left( \frac{\xi_{D}^{5+2\gamma}}{5+2\gamma} \right),
$$

$$
um_d = \frac{1}{3+\gamma} \left( \frac{\xi_{S}^{5+2\gamma}}{5+2\gamma} - \frac{\xi_{S}^{2+\gamma}}{2+\gamma} \right) + \frac{1}{2+\gamma} \left( \frac{\xi_{D}^{5+2\gamma}}{5+2\gamma} \right)
$$

Thirdly, the quasi-static charges for the TFT terminals S,D,G are calculated adding proportional parts when $\text{den}<V_{\text{min}}$, by

$$
Q_G = -Q_D - Q_S, \text{ where with } V_{\text{min}} = 10 \mu V \text{ and } C_{G0} = W \times L \times C_t,
$$

$$
Q_S = np \times (-C_{G0}) (V_{GTS} + V_{GTD}) \sqrt{\left( \frac{\text{num}_s}{2} + \left( \frac{1+\xi_S}{6} V_{\text{min}} \right)^2 \right) \left( \text{den}^2 + V_{\text{min}}^2 \right)^2}
$$

$$
Q_D = np \times (-C_{G0}) (V_{GTS} + V_{GTD}) \sqrt{\left( \frac{\text{num}_d}{2} + \left( \frac{1+\xi_D}{6} V_{\text{min}} \right)^2 \right) \left( \text{den}^2 + V_{\text{min}}^2 \right)^2}
$$

Finally, the capacitive currents $i_G,i_S,i_D$ in the TFT terminals G,S,D are the time derivatives $\partial Q_G/\partial t$, $\partial Q_S/\partial t$, $\partial Q_D/\partial t$, calculated by

$$
i_G(G,\text{virtualNode}) = \frac{\partial Q_G}{\partial t} \times \min(1,\text{selectQS})
$$

$$
i_S(S,\text{virtualNode}) = \frac{\partial Q_S}{\partial t} \times \min(1,\text{selectQS})
$$

$$
i_D(D,\text{virtualNode}) = \frac{\partial Q_D}{\partial t} \times \min(1,\text{selectQS}),
$$

grounding the virtualNode by $V(\text{virtualNode})=0$,

since $(i_G + i_S + i_D) = 0 \pm$ numerical rounding error,

and a multiplier $\min(1,\text{selectQS})$ is added in the calculation, so that the capacitive currents $i_G,i_S,i_D$ are calculated, if the model parameter selectQS$\geq 1$. 
The model parameter selectQS (select quasi-static) is an integer number for selection of the quasi-static model. Instantiation of the oTFT 2.04.01 compact model with selector selectQS=1 enables the quasi-static model described above. One may desire to suppress the quasi-static model by various reasons, for example, to evaluate the contribution of the quasi-static capacitance in the frequency or transient response in proportion with overlap capacitances, or to implement custom model for capacitances in the TFT. The point is that the quasi-static model is fully determined by the parameters for DC response of the TFT, which requires to add an extra model parameter to control the occurrence of the quasi-static model. For the case of suppression of the quasi-static model, one instantiates the oTFT 2.04.01 compact model with selectQS=0, which will make zero the capacitive currents \( i_G, i_S, i_D \) in the TFT terminals G, S, D. Thus, the quasi-static model will be suppressed in the response of the oTFT 2.04.01 compact model, while the quasi-static charges will be still available for other purposes, such as monitoring, if desired. Furthermore, the use of the function \( \min(1, \text{selectQS}) \) also allows to have other variant for the quasi-static model in the future. For example, the quasi-static model in the oTFT 2.04.01 compact model does not consider the “extra” charge due to channel modulation and leakage in the TFT. These have not been considered due to two reasons. One reason is that the extra charge is small fraction of channel charge induced by the gate bias. Second reason is that the geometrical overlap capacitances in the TFT structure between contact pads and gate usually dominate over the TFT channel quasi-static capacitances [4], which makes unnecessary to include the even smaller capacitances that might be present due to the extra charge by channel modulation and leakage. Finally, the response from the quasi-static model is directly forwarded to the TFT terminals, as recommended in [4] to preserve the quasi-static assumption, but one might be curious to include also the contact resistance in the frequency response of the TFT. The latter will need reconnection of the current sources, eq. (27), to the intrinsic nodes \( G_I, D_I, S_I \), which can be accomplished assigning another value for selectQS, e.g., selectQS =2, and implementing an “if” statement in the Verilog-A code, so that the capacitive currents \( i_G, i_S, i_D \) are redirected to the intrinsic nodes \( G_I, D_I, S_I \). Mentioned above, this is not recommended, because the connection of \( i_G, i_S, i_D \) to the intrinsic node will cause the contact resistances to initiate a transient process in the evolution of the quasi-static charges, which obscures the quasi-static assumption for the quasi-static charge models [4].

2.6. Overlap capacitances and other geometrical capacitances between TFT terminals

The TFT structures usually have significant geometrical overlaps of conductive layers. For example, the contact pads for source and drain can be larger than the channel length of the TFT. This typical situation for organic TFTs (OTFTs) is shown in Figure 9, in which the capacitances \( C_{OV} \) due to geometrical overlap dominate over quasi-static and other capacitances of the TFT channel [4].

The length \( L_{OV} \) of the geometrical overlap of the gate conductor with drain/source pad is a model parameter in the oTFT 2.04.01 compact model. Accordingly, the source-gate and drain-gate overlap capacitances \( C_{OV} \) are assumed equal and scalable with the gate dielectric capacitance and channel width, so that

\[
C_{OV} = C_1 \times W \times L_{OV}
\]  

(28)

The overlap capacitance model calculates the capacitive current between gate and source/drain terminals of the TFT by multiplying \( C_{OV} \) with the time derivatives of the terminal voltages, as
\[ i_{GS} = C_{ov} \frac{\partial (V_G - V_S)}{\partial t}, \text{ for gate-source overlap capacitance} \]
\[ i_{GD} = C_{ov} \frac{\partial (V_G - V_D)}{\partial t}, \text{ for gate-drain overlap capacitance} \]

(29)

Mentioned above, the overlap capacitances dominate over the quasi-static capacitances. Therefore, when evaluating quasi-static capacitances, one suppresses overlap capacitances by instantiation of the oTFT 2.04.01 compact model with zero value for the overlap length parameter \( L_{OV} = 0 \).

Another geometrical capacitance in the TFT structure is the drain-source fringing capacitance, denoted by \( C_{DSOV} \) in the Verilog-A code of the oTFT 2.04.01 compact model. This capacitance is insignificant, having upper limit \[4\] of
\[ C_{DSOV} \leq W \times 2 \frac{\varepsilon_{Bov} \varepsilon}{\pi}, \varepsilon_{Bov} \sim 1-\varepsilon_B/2 \]

(30)

where \( \varepsilon_{Bov} \) is again the relative permittivity (dielectric constant) of the medium at the “back” of the semiconducting film. (The “front” of the semiconductor film is the interface with the gate dielectric.) The notation in the Verilog-A code is \( \varepsilon_{Bov} \) for \( \varepsilon_{Bov} \), and \( \varepsilon_{Bov} \sim 1-\varepsilon_B/2 \) is a model parameter. Similar to the overlap capacitances, the capacitive current due to the fringing capacitance \( C_{DSOV} \) is calculated by multiplying \( C_{DSOV} \) with the time derivatives of the D,S terminal voltages by the following expression
\[ i_{DS} = C_{DSOV} \frac{\partial (V_D - V_S)}{\partial t}, \text{ for drain-source geometrical capacitance} \]

(31)

While possibly \( C_{DSOV} \) and \( i_{DS} \) are negligible for TFTs, one can suppress the geometrical capacitance \( C_{DSOV} \) in simulations by instantiation of the oTFT 2.04.01 compact model with zero value for the model parameter \( \varepsilon_{Bov} \equiv \varepsilon_{Bov} = 0 \). For the reason of independent suppression of channel modulation, leakage and geometrical capacitance, the oTFT 2.04.01 compact model uses different parameters (\( \varepsilon_B \equiv \varepsilon_B \), \( \varepsilon_{Bleak} \equiv \varepsilon_{Bleak} \) and \( \varepsilon_{Bov} \equiv \varepsilon_{Bov} \), respectively) for dielectric constant of the medium in the semiconducting film “back”. Ideally, these three parameters for dielectric constant
should have identical values. Practically, however, one may need to use different values for permittivity, in order to fit experimental characteristics of organic TFTs.

2.7. Monitor of quantities (forwards quantities to test terminals, isolated from oTFT model)

The Verilog-A code of the oTFT 2.04.01 compact model also contains a template for monitoring of internal quantities in the model. Mentioned in the beginning of Sec. 2, the monitor forwards a copy of selected internal quantities to a monitoring rail with electrical nodes (testGND,testSIGNAL). The monitor will not be addressed in this section, because the monitoring rail is “isolated” from the other rails, and it does not affect the operation of the oTFT model.

However, one should manipulate the code in order to use the monitor, and also, to connect external resistor the test terminals. The default definition of module oTFT in the Verilog-A code is with all nodes available for connection in circuits, but the lines at the end of the analog processing section are commented in the default text of the Varilog-A code. Thus, zeros are forwarded to terminals (testGND,testSIGNAL), and one should uncomment a line in the analog processing section accordingly, so that the desired quantity for monitoring is forwarded the test terminals of the oTFT module.
3. Implementation details of the characteristic equations in oTFT 2.04.01 compact model

This section relates the characteristic equations of the oTFT 2.04.01 compact model to Verilog-A code of the compact model. Refer to Table 1 in Sec. 2.1 for definitions and default values of the model parameters.

/* ============ Generic TFT charge drift DC model ============ */

By eqs. (2) and (3) in Sec. 2.1, the characteristic equations of the generic TFT charge drift DC model and the sub-models for overdrive voltages are

\[
I_{D,S} = n_p \times \frac{W}{L} C_t \frac{\mu_c}{(V_T)^\gamma} \times \left\{ \frac{(V_{GTS})^{(2+\gamma)} - (V_{GTD})^{(2+\gamma)}}{2 + \gamma} \right\}
\]

\[
V_{GTS} = V_{SS} \ln \left[ 1 + \exp \left( \frac{n_p (V_{GI} - V_T - V_{SI})}{V_{SS}} \right) \right]
\]

\[
V_{GTD} = V_{SS} \ln \left[ 1 + \exp \left( \frac{n_p (V_{GI} - V_T - V_{DI})}{V_{SS}} \right) \right]
\]

It is possible that a calculation with the exponential function \( \exp(x) \) can cause overflow in case when \( x > 40 \). Therefore, \( V_{SS} \) is implemented as function also of the positive magnitude \( n_p (V_{G-I} - V_T - V_i) \), \( i = D, S \). Thus, the implementation of the characteristic equation for the source overdrive voltage \( V_{GTS} \) is

\[
V_{SSS} = \sqrt{V_{SS}^2 + \left[ \frac{n_p (V_{GI} - V_T - V_{SI}) - V_{SSS}}{64} \right]^2}
\]

\[
V_{GTS} = V_{SSS} \ln \left[ 1 + \exp \left( \frac{n_p (V_{GI} - V_T - V_{SI})}{V_{SSS}} \right) \right] \approx V_{SSS} + V_{GTS}/32
\]

without overflow of \( \exp(x) \) at large \( x \), because \( x \leq 32 \). The resulting Verilog-A code for \( V_{GTS} \) is

\[
V_{GTS} = \sqrt{\text{pow}(V_{SSS},2) + \text{pow}(\text{abs}(V_{GTS}-V_{SSS}),2)}; \quad \text{// To ensure } V_{GTS}/V_{SS} < 32
\]

\[
V_{GTS} = \text{VSSS}\ln(1 + \exp(\text{abs}(V_{GTS}-V_{SSS}))/64); \quad \text{// Source overdrive voltage}
\]

Similarly, \( V_{SSD} \) function is calculated for \( V_{GTD} \) without overflow of the exponential function, as

\[
V_{SSD} = \sqrt{\text{pow}(V_{SSS},2) + \text{pow}(\text{abs}(V_{GTD}-V_{SSS}),2)}; \quad \text{// To ensure } V_{GTD}/V_{SS} < 32
\]

\[
V_{GTD} = \text{VSSD}\ln(1 + \exp(\text{abs}(V_{GTD}-V_{SSD}))/64); \quad \text{// Drain overdrive voltage}
\]

Since no overflow will be present in \( V_{GTS} \) and \( V_{GTD} \), then the current of the generic TFT charge drift DC model (placed between the intrinsic nodes \( D_i, S_i \)) is calculated as defined, by

\[
I_{(D,I,S)} = \frac{n_p W}{L} u_o / \gamma \times \left( \frac{V_{GTS}}{V_{GTD}} \right)^{\gamma/2}
\]

By eq.(8) in Sec.2.2, linear and non-linear components are given for the contacts, respectively by

\[
V_{C,\text{lin}} = R_C \times I_C
\]

\[
V_{C,\text{non-lin}} = R_{C\text{max}} \times I_C \times \left( \frac{I_{C\text{max}}}{I_{C\text{max}} + I_C} \right)^{n_C}
\]
Accordingly, the contact voltage drops are placed between terminal and intrinsic nodes, and calculated in 6 steps by the following Verilog-A code. The odd-number lines are for linear contacts and the even lines are for non-linear contacts.

```verbatim
V(G,G) <- RGmin*I(G,G); // negligible gate contact resistance
V(G,G) <- 0*I(G,G)*pow(IICmax/(IICmax+abs(I(G,G))),nIC); // zero non-linear gate contact resistance
V(S,S) <- RC * I(S,S); // source's linear contact resistance
V(S,S) <- RCmax*I(S,S) * pow(IICmax/(IICmax + abs(I(S,S))),nIC); // source's non-linear contact
V(D,D) <- RC * I(D,D); // constant (minimum) drain's linear contact resistance
V(D,D) <- RCmax*I(D,D) * pow(IICmax/(IICmax + abs(I(D,D))),nIC); // drain's non-linear contact
```

```verbatim
/* =========== Channel modulation =========== */
By eq. (9) in Sec. 2.3, the unit-area fringing capacitance \( C_L \) at the “back” of the semiconducting film is

\[
C_L = \frac{\varepsilon B \varepsilon_0}{\pi L}
\]

The formula for \( C_L \) is implemented as a literal macro in the declaration section of the Verilog-A code by

\`
#define CL  eB * `P_EPS0 / `M_PI / L
```

where \( \varepsilon_0 \) and \( \pi \) are constants in "constants.vams".

By eqs. (10) and (11) in Sec. 2.3, the channel modulation “extra” current due to the fringing capacitance \( C_L \) at the “back” of the semiconducting film and by bias-enhanced mobility has three components

\[
\Delta I_{DS} = \frac{W}{L} \frac{u_0}{V_{gamma}} \frac{\mu_0}{V_g} \left( \frac{V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma}}{2 + \gamma} \right) + \left( \frac{V_{DI} + V_{SI}}{2} - (V_G - V_T) \right) \frac{V_{GTS}^{1+\gamma} - V_{GTD}^{1+\gamma}}{1 + \gamma} + \frac{f_{\Delta ID}(V_{GTS}, V_{GTD}, \gamma)}{2(1 + \gamma)(3 + 2\gamma)} (V_{DI} - V_{SI})
\]

where the fringing capacitance constant \( K_{\Delta ID} \propto C_L \) and the function \( f_{\Delta ID}(V_{GTS}, V_{GTD}, \gamma) \) are

\[
K_{\Delta ID} = \frac{W}{6C_L} \frac{u_0}{V_g} \left( \frac{V_{3+2\gamma}^{GTS} - (3 + 2\gamma) \frac{V_{GTS}^{2+\gamma}}{V_{GTD}^{1+\gamma}} + (3 + 2\gamma) \frac{V_{1+\gamma}^{GTS}}{V_{GTD}^{2+\gamma}} - V_{3+2\gamma}^{GTD}}{\left| V_{2+\gamma}^{GTS} - V_{2+\gamma}^{GTD} \right| + \left[ (1 + \text{num}) V_{\text{min}} \right]^{2+\gamma}} \right)
\]

The corresponding lines in the code for channel modulation are

```verbatim
I(DI,SI) <+ np*W/L*uo/pow(Vgamma, gamma)*6*CL*(pow(VGTS, gamma+2)-pow(VGTD, gamma+2))/(gamma+2); // first component of channel modulation current
I(DI,SI) <+ W/L*uo/pow(Vgamma, gamma)*6*CL*(V(DI)/2+V(SI)/2-V(GI)-VT)*(pow(VGTS, gamma+1)-pow(VGTD, gamma+1)))/(gamma+1); // second component of channel modulation current
numerator=abs(pow(VGTS,3+2*gamma)-(3+2*gamma)*pow(VGTS,2+gamma)*pow(VGTD,1+gamma) + (3+2*gamma)*pow(VGTS,1+gamma)*pow(VGTD,2+gamma)-pow(VGTD,3+2*gamma));
典
ominator - abs(pow(VGTS,2+gamma)*pow(VGTD,2+gamma)) + pow((1+3)*Vmin,2+gamma); // small voltage (1+3)*Vmin~40uV added to avoid division on zero
fDeltaID = numerator/denominator;
I(DI,SI) <+ W/L*uo/pow(Vgamma, gamma)*6*CL*(V(DI)-V(SI))*fDeltaID/2/(gamma+1)/(3+2*gamma); // third component of channel modulation current
```

The value of \( V_{\text{min}} \) is defined as literal constant in the declaration section of the Verilog-A code by

\`
#define Vmin 10.0e-6
```
//* ============ Channel leakage ============ */

By eq. (14) in Sec. 2.4, the Ohmic (linear) leakage is

\[ I_{\text{leak,Ohmic}} = \frac{V_{DS}}{R_{BS}} \times \frac{W}{L} \]

The equation is implemented in the Verilog-A code by the line

\[ I(D,S) <+ V(D,S) \times \frac{W}{L} / R_{BS}; // \text{Ohmic leakage in the bulk of the semiconducting film} \]

The non-linear leakage, caused by the fringing capacitance \( C_{LL} \) at the “back” of the semiconducting film, results in two anti-parallel connected TFT diodes. Similarly to \( C_L \) for channel modulation, the unit-area fringing capacitance \( C_{LL} \) at the “back” of the semiconducting film for leakage is

\[ C_{LL} = \frac{e_{\text{Bleak}} e_0}{\pi L} \]

and the formula for \( C_{LL} \) is implemented as a literal macro in the declaration section of the Verilog-A code by

\[ \text{'define } C_{LL} \text{ } e_{\text{Bleak}} * 'P_EPS0 / 'M_PI / L \]

where \( 'P_EPS0 = \varepsilon \) and \( 'M_PI = \pi \) are constants in "constants.vams".

By eq. (16) in Sec.2.4, the expressions for the two anti-parallel connected TFT diodes for the non-linear leakage are

\[ I_{\text{leak,non-linear}}(D,S) = np \times \frac{W}{L} 6 C_{LL} \frac{\mu_o}{(V_\gamma)^2} \times \frac{V_{DTS}^{2+\gamma} - V_{DTD}^{2+\gamma}}{2+\gamma}, \text{ for the forward leakage diode} \]

\[ + np \times \frac{W}{L} 6 C_{LL} \frac{\mu_o}{(V_\gamma)^2} \times \frac{V_{STS}^{2+\gamma} - V_{STD}^{2+\gamma}}{2+\gamma}, \text{ for the reverse leakage diode} \]

where, for a normal (forward) polarity of biasing \( np \times (V_D - V_{TL} - V_S) > V_{SS} \) and \( np \times (V_D - V_S) > 0 \),

for the forward diode \( V_{DTS} \approx np \times (V_D - V_{TL} - V_S) - V_{SS} \)

\[ V_{DTD} = \text{EODR} (np \times V_{TL}) < V_{SS}, \text{ and} \]

for the reverse diode \( V_{STS} \approx \text{EODR} (np \times V_{TL}) < V_{SS} \)

\[ V_{STD} = \text{EODR} (np \times (V_S - V_{TL} - V_D)) \approx 0. \]

The corresponding lines in the Verilog-A code for channel leakage are

\[ // \text{Forward leakage diode} \]
\[ \text{VSSSLF=sqrt(pow(VSS,2)+pow((np*(V(D)-VTL-V(S))+abs(V(D)-VTL-V(S)))/64,2)); // Ensure VGT_/VSS_ <32,} \]
\[ \text{so that not overflowing exp(VGT_/VSS_) at high bias and small VSS} \]
\[ \text{VGTSLF=VSSSLF*ln(1+exp(np*(V(D)-VTL-V(S))/VSSSLF)); // Source overdrive for forward leakage diode} \]
\[ \text{VSSDLF=sqrt(pow(VSS,2)+pow((np*(V(D)-VTL-V(D))+abs(V(D)-VTL-V(D)))/64,2)); // Ensure VGT_/VSS_ <32,} \]
\[ \text{so that not overflowing exp(VGT_/VSS_) at high bias and small VSS} \]
\[ \text{VGTDLF=VSSDLF*ln(1+exp(np*(V(D)-VTL-V(D))/VSSDLF)); // Drain overdrive for forward leakage diode} \]
\[ I(D,S) <+ np*W/L*\mu_o/pow(Vgamma,\gamma)*6*e_{\text{CLL}}*(pow(VGTSLF,\gamma+2)-pow(VGTDLF,\gamma+2))/(\gamma+2); // TFT generic for forward leakage diode} \]
Reverse leakage diode

\[
V_{SSSLR} = \sqrt{\left(V_{SS}^2 + \left(\frac{np(V(S) - V_{TL} - V(S))}{64}\right)^2\right)} \quad \text{// Ensure } V_{GT}/V_{SS} < 32, \\
\text{so that not overflowing } exp(V_{GT}/V_{SS}) \text{ at high bias and small } V_{SS}
\]

Source overdrive for reverse leakage diode

\[
V_{GTSLR} = V_{SSSLR} \cdot \ln(1 + \exp(\frac{np(V(S) - V_{TL} - V(S))}{V_{SSSLR}}))
\]

Drain overdrive for reverse leakage diode

\[
I(D,S) < np^*W/L*uo/pow(V_{gamma},\gamma)*6^*`CLL*(pow(V_{GTSLR},\gamma+2)-pow(V_{GTDLR},\gamma+2))/(\gamma+2);
\]

Quasi-static charge model

By eqs. (17), (18) and (19) in Sec. 2.5, the expressions for the quasi-static charges \(Q_G, Q_S, Q_D\) corresponding to the TFT terminals G, S, D, respectively, are

\[
Q_G = -Q_D - Q_S = \text{np} \times \left( -C_{G0} \right) \times \left( \frac{2 + \gamma}{3 + \gamma} \right) \frac{V_{GTS}^{3+\gamma} - V_{GTD}^{3+\gamma}}{V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma}}
\]

\[
Q_S = \text{np} \times \left( -C_{G0} \right) \times \left( \frac{2 + \gamma}{3 + \gamma} \right) \frac{V_{GTS}^{5+2\gamma} - V_{GTD}^{5+2\gamma}}{(V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma})^2}
\]

\[
Q_D = \text{np} \times \left( -C_{G0} \right) \times \left( \frac{2 + \gamma}{3 + \gamma} \right) \frac{V_{GTS}^{5+2\gamma} - V_{GTD}^{5+2\gamma}}{(V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma})^2}
\]

where \(C_{G0}=W \times L \times C_I\) is the gate dielectric capacitance over the entire area of the TFT channel, and \(C_{G0}\) is defined by a literal macro in the declaration section of Verilog-A code as

\`
\text{'define } CG0 W*L*C_I
\`

However, the direct use of these expressions meets with problems of truncation and division on zero by numerical calculations. Therefore, the equations are normalized and enhanced with inclusion of \(V_{min}=10 \mu V\) in the modified expressions so that the numerical problems are resolved, and the numerical calculation of the quasi-static charges and their derivatives are smooth and continuous. The modifications of the equations resulted in normalized generic quasi-static charge model of TFT for computer simulators with expressions, as follows.

Firstly, by eq. (24) in Sec 2.5, the normalized overdrive voltages \(\xi_S\) and \(\xi_D\) are made non-zero, calculating by

\[
\xi_S = \frac{\sqrt{V_{GTS}^2 + V_{min}^2}}{\sqrt{V_{GTS}^2 + V_{min}^2} + \sqrt{V_{GTD}^2 + V_{min}^2}} > 0 \quad \text{and} \quad \xi_D = \frac{\sqrt{V_{GTD}^2 + V_{min}^2}}{\sqrt{V_{GTS}^2 + V_{min}^2} + \sqrt{V_{GTD}^2 + V_{min}^2}} > 0,
\]

with \(V_{min}=10 \mu V\)

even when the exponential functions in eq. (3) for the overdrive voltages \(V_{GTS}\) and \(V_{GTD}\) might become zero for biasing of the TFT deep in the subthreshold regime. The corresponding lines in the Verilog-A code for normalized overdrive voltages \(\xi_S\) and \(\xi_D\) are

\`
ksiS=sqrt(pow(VGTS,2)+pow(\'Vmin,2))/(sqrt(pow(VGTS,2)+pow(\'Vmin,2)) + sqrt(pow(VGTD,2)+pow(\'Vmin,2))); // normalized overdrive voltages for source
ksiD=sqrt(pow(VGTD,2)+pow(\'Vmin,2))/(sqrt(pow(VGTS,2)+pow(\'Vmin,2)) + sqrt(pow(VGTD,2)+pow(\'Vmin,2))); // normalized overdrive voltages for drain
\`

*/

**Quasi-static charge model**
Mentioned above for channel modulation, the value of $V_{\text{min}}$ is defined as literal constant in the declaration section of the Verilog-A code by
```
`define Vmin 10.0e-6
```

Secondly, by eq. (25) in Sec 2.5, denominator and numerator functions are calculated as

$$\text{den} = \left[ \left( \frac{\xi^{2+\gamma}}{2 + \gamma} \right) - \left( \frac{\xi_D^{2+\gamma}}{2 + \gamma} \right) \right]^2$$

$$\text{num}_s = \frac{1}{2 + \gamma} \left( \frac{\xi^{5+2\gamma}}{5 + 2\gamma} \right) - \left( \frac{\xi_D^{5+2\gamma}}{5 + 2\gamma} \right) + \frac{1}{2 + \gamma} \left( \frac{\xi^{3+\gamma}}{3 + \gamma} \right)$$

$$\text{num}_d = \frac{1}{3 + \gamma} \left( \frac{\xi^{5+2\gamma}}{5 + 2\gamma} \right) - \left( \frac{\xi_D^{5+2\gamma}}{5 + 2\gamma} \right) + \frac{1}{2 + \gamma} \left( \frac{\xi^{3+\gamma}}{3 + \gamma} \right)$$

The corresponding lines in the Verilog-A code for the functions den, numS and numD are
```
den = pow((pow(ksiS,2+gamma))/(2+gamma)-pow(ksiD,2+gamma)/(2+gamma),2); // denominator of the normalized functions of QS and QD
numS = (pow(ksiS,5+2*gamma)/(5+2*gamma))/(2+gamma) - (pow(ksiS,3+gamma)/(3+gamma))*pow(ksiD,2+gamma)/(2+gamma) + (pow(ksiD,5+2*gamma)/(5+2*gamma))/(3+gamma); // numerator of the normalized function of QS
numD = (pow(ksiS,5+2*gamma)/(5+2*gamma))/(3+gamma) - (pow(ksiS,2+gamma)/(2+gamma))*pow(ksiD,3+gamma)/(3+gamma) + (pow(ksiD,5+2*gamma)/(5+2*gamma))/(2+gamma); // numerator of the normalized function of QD
```

Thirdly, by eq. (26) in Sec 2.5, the quasi-static charges for the TFT terminals S,D,G are calculated adding proportional parts when $\text{den}<V_{\text{min}}$, by

$$Q_G = -Q_D - Q_S, \text{ where with } V_{\text{min}} = 10 \mu V \text{ and } C_{G0} = W \times L \times C_1,$$

$$Q_S = np \times (-C_{G0}) \left( V_{GTS} + V_{GTD} \right) \sqrt{\frac{(\text{num}_S)^2 + \left( \frac{1+\xi_S}{6} V_{\text{min}} \right)^2}{(\text{den})^2 + \left( V_{\text{min}} \right)^2}}$$

$$Q_D = np \times (-C_{G0}) \left( V_{GTS} + V_{GTD} \right) \sqrt{\frac{(\text{num}_D)^2 + \left( \frac{1+\xi_D}{6} V_{\text{min}} \right)^2}{(\text{den})^2 + \left( V_{\text{min}} \right)^2}}$$

The corresponding lines in the Verilog-A code for the quasi-static charges are
```
Q_S = np*(-`CG0)*(VGTS+VGTG)*sqrt((pow(numS,2)+pow(1+ksiS,6)/6)/pow(den,2)+pow(Vmin,2)); // quasi-static charge of source terminal
Q_D = np*(-`CG0)*(VGTG+VGTG)*sqrt((pow(numD,2)+pow(1+ksiD,6)/6)/pow(den,2)+pow(Vmin,2)); // quasi-static charge of drain terminal
Q_G = -(Q_S+Q_D); // The quasi-static charge of gate terminal is inverted sum of the quasi-static charges of source and drain terminals (charge conservation)
```

Finally, by eq. (27) in Sec 2.5, the capacitive currents $i_G,i_S,i_D$ in the TFT terminals G,S,D are the time derivatives $\partial Q_G/\partial t$, $\partial Q_S/\partial t$, $\partial Q_D/\partial t$, calculated by
\[
\begin{align*}
    i_g (G, \text{virtualNode}) &= \frac{\partial Q_{g}}{\partial t} \times \min(1, \text{selectQS}) \\
    i_s (S, \text{virtualNode}) &= \frac{\partial Q_{s}}{\partial t} \times \min(1, \text{selectQS}) \\
    i_d (D, \text{virtualNode}) &= \frac{\partial Q_{n}}{\partial t} \times \min(1, \text{selectQS}),
\end{align*}
\]

grounding the virtualNode by \(V(\text{virtualNode})=0\), since \((i_g + i_s + i_d) = 0\) ± numerical rounding error,

and a multiplier \(\min(1, \text{selectQS})\) is added in the calculation, so that the capacitive currents \(i_g, i_s, i_d\) are calculated, if the model parameter \(\text{selectQS} \geq 1\). Thus, instantiation of the oTFT 2.04.01 compact model with \(\text{selectQS} = 0\) will make zero the capacitive currents \(i_g, i_s, i_d\) in the TFT terminals \(G, S, D\), suppressing the response from the quasi-static model in the oTFT 2.04.01 compact model, while the quasi-static charges will be still available for other purposes. The current sources for \(i_g, i_s, i_d\) are connected to virtualNode, and virtualNode is also grounded to “sink” numerical rounding errors.

The corresponding lines in the Verilog-A code for the capacitive currents \(i_g, i_s, i_d\) in are

\[
\begin{align*}
    I(G,\text{virtualNode}) &= +\frac{\partial Q_g}{\partial t} \times \min(1, \text{selectQS}); // capacitive current in gate terminal from QG variation \\
    I(S,\text{virtualNode}) &= +\frac{\partial Q_s}{\partial t} \times \min(1, \text{selectQS}); // capacitive current in source terminal from QS variation \\
    I(D,\text{virtualNode}) &= +\frac{\partial Q_n}{\partial t} \times \min(1, \text{selectQS}); // capacitive current in drain terminal from QD variation \\
    V(\text{virtualNode}) &= +0; // grounding the virtual node
\end{align*}
\]

/* ============ Overlap capacitances ============ */

By eq. (28) in Sec. 2.6, the source-gate and drain-gate overlap capacitances \(C_{ov}\) are

\[C_{ov} = C_i \times W \times L_{ov}\]

where \(L_{ov}\) is the length of the geometrical overlap of the gate conductor with drain/source pads. The formula for \(C_{ov}\) is defined by a literal macro in the declaration section of Verilog-A code as

`define COV CI*W*L_OV

By eq. (29) in Sec. 2.6, \(C_{ov}\) is multiplied with the time derivatives of the terminal voltages to calculate the capacitive current between gate and source/drain terminals of the TFT by the following expressions

\[
\begin{align*}
    i_{gs} &= C_{ov} \frac{\partial (V_G - V_S)}{\partial t}, \text{ for gate-source overlap capacitance} \\
    i_{gd} &= C_{ov} \frac{\partial (V_G - V_D)}{\partial t}, \text{ for gate-drain overlap capacitance}
\end{align*}
\]

The corresponding lines in the Verilog-A code for the capacitive currents \(i_{gs}, i_{gd}\) due to the geometrical overlap capacitances are

\[
\begin{align*}
    I(G,S) &= + \text{COV} \times \text{ddt}(V(G)-V(S)); // Gate-source overlap capacitance \\
    I(G,D) &= + \text{COV} \times \text{ddt}(V(G)-V(D)); // Gate-grain overlap capacitance
\end{align*}
\]

By eq. (30) in Sec. 2.6, the upper limit for geometric and also fringing capacitance between the drain-source terminals is

\[C_{DSOV} \leq W \times 2 \frac{\varepsilon_{fr} \varepsilon_0}{\pi}\]
The formula for $C_{DSOV}$ is defined by a literal macro in the declaration section of Verilog-A code as

\[
\text{`define CDSOV } W \ast 2 \ast eBov \ast \text{'P_EPS0} / \text{'M_PI}
\]

where \text{'P_EPS0} = \varepsilon_o \text{ and } \text{'M_PI} = \pi \text{ are constants in "constants.vams".}

Similar to $\varepsilon_B$ for $C_L$ and $\varepsilon_{\text{Bleak}}$ for $C_{LL}$ before, $eBov = \varepsilon_{Bov} \sim 1$ is the dielectric constant of the medium at the “back” of the semiconducting film for the geometrical fringing capacitance between the drain-source terminals. Since $C_{DSOV}$ is geometrical capacitance, then similar to the overlap capacitances $C_{OV}$, then the capacitive current $i_{DS}$ due to the fringing capacitance $C_{DSOV}$ is calculated by multiplying $C_{DSOV}$ with the time derivatives of the D,S terminal voltages. Thus, by eq. (31) in Sec. 2.6, the expression for the capacitive current $i_{DS}$ due to the drain-source fringing capacitance $C_{DSOV}$ is

\[
i_{DS} = C_{DSOV} \frac{\partial(V_D - V_S)}{\partial t}, \text{ for drain-source geometrical capacitance}
\]

The corresponding line in the Verilog-A code for the capacitive current $i_{DS}$ due to the geometrical capacitance $C_{DSOV}$ is

\[
I(D,S) <+ \text{`CDSOV} \ast \text{ddt}(V(D)-V(S)); // Drain-source overlap capacitance (usually negligible)
\]

Overall, the overlap capacitance $C_{OV}$ dominates in TFTs, whereas the fringing capacitance $C_{DSOV}$ is usually negligible.

```verbatim
/* ============ Monitor of quantities ============ */
There is not a particular characteristic equation in the oTFT 2.04.01 compact model associated with the monitor located at the end of the analog processing section in the Verilog-A code. The code of the monitor is a tool for forwarding copy of internal quantities from the oTFT model to test terminals testGND, testSIGNAL. The code of the monitor assumes that current is sourced out from terminal testSIGNAL and an external resistor between testSIGNAL and testGND receives the current. For example, connecting testGND to the circuit ground, the line

\[
I(testGND, testSIGNAL) <+ \text{np}*(V(SI)-V(S)); // monitor the magnitude of contact voltage drop, converted to current, 1A=1V
\]

will output the contact voltage drop across the source contact as current exiting from testSIGNAL.

There are several examples for monitoring of different quantities in the code of the monitor. All these are commented in the code, except for the default monitoring of nothing

\[
I(testGND, testSIGNAL) <+ 0; // The default is monitoring nothing.
\]

The monitor is helpful for detailed investigation of the oTFT model, but the monitor is not part of the model. Therefore, the monitor is not under consent, and it is isolated from the oTFT model, so that the operation of the oTFT model is not affected by whether the monitor is used or not used.
```
4. Installation and instantiation of oTFT 2.04.01 compact model

The installation and instantiation of the oTFT 2.04.01 compact model depends on the simulation environment. In the majority of these simulation environments, one prepares a model library, and places and links the file with the Verilog-A code appropriately in the library.

As described in the Verilog-A file, the oTFT 2.04.01 compact model can be used with three, six, five, or with all 8 terminals, depending which lines are commented in the beginning of the code. The default terminal configuration is with all 8 terminals, for which the code is

```
`include "constants.vams"
`include "disciplines.vams"
module oTFT(G,S,D,GI,SI,DI,testGND,testSIGNAL); // oTFT model with all nodes available
    parameter real version_oTFT = 2.0401; // oTFT model version = 2.04.01
...
endmodule // module oTFT;
```

At minimum, the oTFT model has to be with three terminals, for which the code is

```
`include "constants.vams"
`include "disciplines.vams"
module oTFT(G,S,D); // The simplest 3-terminal oTFT model, only with nodes G,S,D
    parameter real version_oTFT = 2.0401; // oTFT model version = 2.04.01
...
endmodule // module oTFT;
```

Depending on the terminal configuration and the design environment, the instantiation of the oTFT model can be as sub-circuit or model. Assuming sub-circuit representation for SPICE simulators, the instantiation of the 3-terminal oTFT model for p-type TFT with source terminal grounded could be

```
.hdl 'oTFT_3T.va'
.lib 'oTFT_2_04_01.lib' oTFT_3T
x1 Gbias 0 Dbias oTFT_3T np=-1 W=0.001 L=0.00001
```
5. Customization and reconfiguration of oTFT 2.04.01 compact model

The customization and reconfiguration of the oTFT model can include:
- Change of model parameter value
- Suppression of sub-model
- Change of terminals
- Customization of monitored quantity

5.1. Change of model parameter value

The oTFT 2.04.01 compact model has default values of its model parameters, as described in Table 1. In Sec. 2.1. One will need to change values of model parameters. Perform the change by instantiation of the model. For example, a Verilog-AMS instantiation

\[ \text{oTFT}_2 \_04 \_01 \# (.\text{np}(-1), .\text{W}(0.001)) \text{pTFT1 (Gbias, Sbias, Dbias)} \]

will create a copy of the oTFT 2.04.01 model, it will assign name pTFT1 to the copy, it will change the polarity to p-type TFT with channel width of 1mm, and it will connect the G,S,D terminals to circuit nodes Gbias, Sbias, Dbias.

5.2. Suppression of sub-model

The oTFT 2.04.01 compact model includes several sub-models, as described in Sec. 2. One may desire suppressing a sub-model. The suppression is properly accomplished by setting model parameters to values by instantiation of the oTFT model, as given in Table 2.

Table 2. Proper assignment of model parameters for suppression of sub-models in oTFT 2.04.01 compact model

<table>
<thead>
<tr>
<th>Set parameter</th>
<th>To suppress</th>
</tr>
</thead>
<tbody>
<tr>
<td>gamma = 0</td>
<td>suppresses bias enhancement of mobility</td>
</tr>
<tr>
<td>eB=0</td>
<td>suppresses channel modulation</td>
</tr>
<tr>
<td>eBleak=0 and RBS=10.0e30 (or larger)</td>
<td>suppresses the leakage sub-model</td>
</tr>
<tr>
<td>RC=1 and RCmax=0</td>
<td>suppresses the contact resistance sub-model</td>
</tr>
<tr>
<td>selectQS=0</td>
<td>suppresses quasi-static capacitances</td>
</tr>
<tr>
<td>LOV=0</td>
<td>suppresses overlap capacitances between gate drain/source</td>
</tr>
<tr>
<td>eBox=0</td>
<td>suppresses geometric capacitance between drain and source</td>
</tr>
</tbody>
</table>
5.3. Change of terminals

The oTFT 2.04.01 can be reconfigured with different terminals for connection in circuits. To modify a configuration, change the declaration of the module in the Verilog-A file. The most useful terminal configurations are:

```verbatim
module oTFT(G,S,D); // The simplest 3-terminal oTFT model, only with nodes G,S,D for gate, source and drain terminals, respectively (use for circuit simulations)

module oTFT(G,S,D,GI,SI,DI); // oTFT model with terminal and intrinsic nodes available (no test terminals for inspection of internal quantities of the model)

module oTFT(G,S,D,testGND,testSIGNAL); // oTFT model with terminal and test nodes available (change the end of the code to select and route quantity to the test terminals)

module oTFT(G,S,D,GI,SI,DI,testGND,testSIGNAL); // oTFT model with all nodes available (for research and troubleshooting). This is the default configuration when downloading the Verilog-A code of the oTFT 2.04.01 compact model from https://nanohub.org/groups/needs/compact_models
```

5.4. Customization of monitored quantity

The monitor at the end of the analog section of the Verilog-A code can be used to route internal quantities from the oTFT 2.04.01 compact model to test terminals (testGND, testSIGNAL).

If you wish monitoring internal quantities in the oTFT model, then use test nodes testGND and testSIGNAL. Examples are given below.

The test terminals are available, if instantiating the oTFT model with the test nodes, e.g.

```verbatim
module oTFT(G,S,D,GI,SI,DI,testGND,testSIGNAL); // oTFT model with all nodes available
module oTFT(G,S,D,testGND,testSIGNAL); // oTFT model with terminal and test nodes
```

The test terminals can be used pushing current from testGND to testSIGNAL. Connect testGND to circuit ground. Connect 1 Ohm resistor between testSIGNAL and ground, and monitor the current through the resistor.

Missing to connect testGND and testSIGNAL to a circuit, it will possibly force the simulator to place $g_{\text{min}}$ to these nodes, or ground the nodes. Do not care, because the test nodes are isolated from the model, and the oTFT model will properly operate.

Next, uncomment the line in the monitor that forwards the desired quantity to the test terminals. The default state of monitor is monitoring nothing, because the Verilog-A code when downloaded has only one line uncommented in the monitor

```verbatim
I(testGND, testSIGNAL) <+ 0; // The default is monitoring nothing.
```
Uncommenting the next line, the monitor will forward the contact voltage drop on the source terminal as current in the test terminal. This line is

// monitor contact voltage drop
I(testGND, testSIGNAL) <+ np*(V(SI)-V(S)); // monitor the magnitude of contact voltage drop

Comment the above line and uncomment the next line. The magnitude of the gate terminal quasi-static charge normalized of gate capacitance $C_{G0}$ and overdrive voltage will be monitored. This line is

I(testGND, testSIGNAL) <+ np*($(QG/(`CG0*VGTS))$); // $(2+\gamma)/(3+\gamma) = 0.72222$ for $\gamma=0.6$

The expression on right is what value the normalized gate charge should have in the saturation regime of operation of the TFT.

The next three lines are for the other two quasi-static charges in the TFT.

In similar manner, the next section of the monitor can be used to calculate the quasi-static capacitances during AC simulation.

The last line in the monitor can be used to observe the numerical error in the simulation, since the current flow into the virtualNode should be zero. This line is

I(testGND, testSIGNAL) <+ I(virtualNode); // monitor numerical error for (capacitive) currents

Monitoring of other quantities can be arranged by the manner above. However, make sure that only one line is uncommented in the monitor, because the operation of the statements

I(testGND, testSIGNAL) <+ value1;
// I(testGND, testSIGNAL) <+ value2;
I(testGND, testSIGNAL) <+ value3;

accumulates the values from all uncommented lines. In the particular example, the accumulated value will be $I(testGND, testSIGNAL) = value1 + value3$. 

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6. Examples for simulation of device characteristics

In this section, characteristics of thin-film transistor (TFT) simulated with the oTFT 2.04.01 compact model are given. The values of the model parameters correspond to typical values for simulation of organic thin-film transistor (OTFT). The default values and purposes of all model parameters are given in Table 1 in Sec. 2.1.

The simulations of the TFT characteristics were carried out using the circuit shown in Figure 10. The parameters on the top of the figure are the default values of the parameters, as implemented in the Verilog-A code of the oTFT 2.04.01 compact model. DC bias ($V_{Gdc}, V_{Ddc}$), AC signals (1V) and pulse signals (0-$V_{Gdc}$ or 0-$V_{Ddc}$) were applied for simulation of current-voltage characteristics (I−V curves), transconductance ($g_m=\partial I_D/\partial V_G$) and output impedance ($z_d=\partial V_D/\partial I_D$), and transient current ($i_d(t)$) of the simulated TFT. The monitor was used to obtain internal characteristics of the TFT, such as contact voltage drop, and to check the charge and current conservations in the model. The results are given in the following subsections, varying polarity of the TFT (np=±1), and contact resistance the oTFT compact model.

In Figure 10, series connections of voltage sources provide DC bias, AC stimuli and pulses. The DC bias is from sources $V_{Gac\_dc}$ and $V_{Dac\_dc}$, in which parameters $V_{Gdc}$ and $V_{Ddc}$ are swept during DC simulations. The DC voltages of the pulse sources $V_{Gpulse}$ and $V_{Dpulse}$ are zero. During AC analyses, either $V_{Gac}=1V$ in source $V_{Gac\_dc}$, or $V_{Dac}=1V$ in source $V_{Dac\_dc}$, to obtain transconductance ($g_m=\partial I_D/\partial V_G$) or output impedance ($z_d=\partial V_D/\partial I_D$), respectively. Similarly, having only one of $V_{Gac}$ or $V_{Dac}$ equal to unity in transient analyses, either $V_{Gpulse}$ is cycled between 0 and $-V_{Gdc}$, or $V_{Dpulse}$ is cycled between 0 and $-V_{Ddc}$, comprising on/off cycling at input (gate) or output (drain) of the TFT, since the DC biases from sources $V_{Gac\_dc}$ and $V_{Dac\_dc}$ remain at $V_{Gdc}$ and $V_{Ddc}$, and the voltages at TFT terminals are sums of voltages of sources. The cycling is with period $1/fHz$ and rise/fall times $0.1/fHz$, where $fHz$ is the frequency of the cycling.
The conditions for the simulations of one TFT with the circuit of Figure 10 are summarized in Table 3. The conditions (sweeps) are biasing voltages \( V_G, V_D \) and frequency \( f_{\text{Hz}} \). For DC characteristics, the results can be arranged in two-four plots. However, the AC characteristics \((g_m, z_d)\) are many, depending on frequency. Therefore, the \((g_m, z_d)\) characteristics will be shown only for selected values of the secondary sweeps. The number of plots for transient characteristics is very large, since the time cannot be reduced from the plots, and the time axis should remain in linear scale, in order to preserve the waveforms. Even when reducing the biasing conditions to four points for \( V_G \) and \( V_D \), the plots are still many, 48, and only selected plots will be shown.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>sweep conditions</th>
<th>Parameter</th>
<th>Plot Y(vs. X) @Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC/AC vs. drain bias ( V_D )</td>
<td>Output ( I_D(V_D) )</td>
<td>Primary sweep ( V_D ) ([-1 : +21, +0.5] ) ( V \times np )</td>
<td>( I_D(V_D) ) @( V_G )</td>
</tr>
<tr>
<td>Contact ( I_D(V_C) )</td>
<td>Secondary sweep ( V_D ) ([-2 : +16, +6] ) ( V \times np )</td>
<td>( I_D(V_C) ) @( V_G )</td>
<td></td>
</tr>
<tr>
<td>Other sweep ( f_{\text{Hz}} )</td>
<td>{1 Hz, 10 kHz, 100 kHz}</td>
<td>( V_C ) @( V_G )</td>
<td></td>
</tr>
<tr>
<td>Transfer ( g_{m\text{e}}(V_D) )</td>
<td>Constants ( V_D = 0V ) ( V_G = 1V )</td>
<td>( I_D(V_G) ) @( V_D, f_{\text{Hz}} )</td>
<td></td>
</tr>
<tr>
<td>Output ( z_{d\text{e}}(V_D) )</td>
<td>Constants ( V_G = 0V ) ( V_D = 1V )</td>
<td>( V_D/I_D(V_D) ) @( V_G, f_{\text{Hz}} )</td>
<td></td>
</tr>
<tr>
<td>DC/AC vs. gate bias ( V_G )</td>
<td>Transfer ( I_D(V_G) )</td>
<td>Primary sweep ( V_D ) ([-4V : +14V, +0.5V] \times np )</td>
<td>( I_D(V_G) ) @( V_D )</td>
</tr>
<tr>
<td>Contact ( I_D(V_C) )</td>
<td>Secondary sweep ( V_D ) {1, 2, 5, 10, 20} ( V \times np )</td>
<td>( I_D(V_C) ) @( V_G )</td>
<td></td>
</tr>
<tr>
<td>Other sweep ( f_{\text{Hz}} )</td>
<td>{1 Hz, 10 kHz, 100 kHz}</td>
<td>( V_C = V_G ) @( V_D, f_{\text{Hz}} )</td>
<td></td>
</tr>
<tr>
<td>Transfer ( g_{m\text{e}}(V_G) )</td>
<td>Constants ( V_D = 0V ) ( V_G = 1V )</td>
<td>( I_D(V_D) ) @( V_G, f_{\text{Hz}} )</td>
<td></td>
</tr>
<tr>
<td>Output ( z_{d\text{e}}(V_G) )</td>
<td>Constants ( V_G = 0V ) ( V_D = 1V )</td>
<td>( V_D/I_D(V_D) ) @( V_G, f_{\text{Hz}} )</td>
<td></td>
</tr>
<tr>
<td>Transient vs. time</td>
<td>Primary sweep ( V_G )</td>
<td>Time, ( t ) {0 : 2/f_{\text{Hz}}, \text{rise/fall time} = 0.1/f_{\text{Hz}}, \frac{1}{2} \text{sinusoid} }</td>
<td></td>
</tr>
<tr>
<td>Secondary sweep ( f_{\text{Hz}} )</td>
<td>{1 Hz, 10 kHz, 100 kHz}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other sweep ( V_D ) {-2, 4, 10, 20} ( V \times np )</td>
<td>for ( V_D = 10V \times np )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other sweep ( V_D ) {1, 2, 5, 20} ( V \times np )</td>
<td>for ( V_G = 10V \times np )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transient transfer ( I_D(V_G) )</td>
<td>Constants ( V_D = 0V ) ( V_G = 1V ), step ( v_G[0:V_G] )</td>
<td>( I_D(t) ), ( V_G(t) ) @( f_{\text{Hz}}, V_G, V_D )</td>
<td></td>
</tr>
<tr>
<td>Transient output ( I_D(V_D) )</td>
<td>Constants ( V_D = 0V ) ( V_D = 1V ), step ( v_D[0:V_D] )</td>
<td>( I_D(t) ), ( V_D(t) ) @( f_{\text{Hz}}, V_G, V_D )</td>
<td></td>
</tr>
</tbody>
</table>

Owing to the large number of plots, the extensive set of results from simulation will be shown only for the TFT with the default parameters. The simulation schedule was performed also for other settings of the model parameters. The I–V curves will be shown for all settings of model parameters. The AC and transient characteristics at different frequencies will be shown only for p-type TFT with \( np = -1 \) and all other parameters the same as the default parameters. The AC and transient characteristics at other changes of model parameters will be shown only for selected frequencies and biasing. All data can be found in numerical form in the files, as given in Table 4.

<table>
<thead>
<tr>
<th>Device</th>
<th>Parameters changed from default values</th>
<th>File name</th>
</tr>
</thead>
<tbody>
<tr>
<td>nTFT default</td>
<td>Default parameters in Verilog-A code</td>
<td>(000)oTFT_2.04.01 nTFT default.xls</td>
</tr>
<tr>
<td>pTFT default</td>
<td>Default parameters, except for ( np = -1 )</td>
<td>(001)oTFT_2.04.01 pTFT default.xls</td>
</tr>
<tr>
<td>pnTFT default</td>
<td>Compare pTFT to pTFT, default parameters</td>
<td>(002)oTFT_2.04.01 pTFT vs nTFT.xls</td>
</tr>
<tr>
<td>nTFT non-lin.R</td>
<td>nTFT with non-linear contacts, large RC_{max}=3M\Omega, I_{Cmax}=1\mu A and ( n_{IC}=1 )</td>
<td>(003)oTFT_2.04.01 nTFT non-linear_contact.xls</td>
</tr>
</tbody>
</table>
6.1. oTFT 2.04.01 with default values of model parameters

When downloaded from https://nanohub.org/groups/needs/compact_models, the Verilog-A code of the oTFT 2.04.01 compact model is for thin-film transistor (TFT) with n-type (electron) conduction (np=+1), and the default values correspond to an organic thin-film transistor (OTFT) with zero threshold voltage and mobility \( \mu_0=0.1 \text{ cm}^2/\text{Vs} \) (\( u_0=0.1e-4 \text{ m}^2/\text{Vs} \)). The default values and purposes of all model parameters are given in Table 1 in Sec. 2.1 and summarized also in Figure 10.

With these default values of the parameters, simulated characteristics of TFT are shown in Figure 11 (I–V curves), Figure 12 (small-signal differential characteristics for transconductance \( g_m \) and output impedance \( z_d \)), Figure 13 (frequency dependence of \( g_m \) and \( z_d \)), and in Figure 16 and Figure 17 (transient drain current \( i_D(t) \) due to pulsing bias of drain and gate).

In the left-hand plots of Figure 11, the plots in linear scales present well-shaped I–V curves. However, in the logarithmic plots in the right-hand plots, one observes the effect of the leakage. In particular, the bottom curve in the top plot (\( V_G=-2V \)) does not saturate at high drain bias, and on the left-hand side in the bottom plot (\( V_G<-2V<0V=V_T \)), the off-current significantly depends on...
the drain bias, shrinking the region with steep sub-threshold slope. The reason for the pronounced leakage effects are because the OTFT is with relatively short channel of length \( L = 10 \mu m \).

The contact effects are not directly visible in Figure 11. The I–V curves (gray color) of the contacts are virtually linear in the plots in linear scales, because \( I_{C_{\text{max}}} = 1 \text{nA} \) is small and \( R_{C_{\text{max}}} = 300 \Omega \) is not very large. Thus, the source and drain contacts are almost linear for \( I_D > 100 \text{ nA} \), each contact with resistance \( R_C = 100 \Omega \). The dotted curves in Figure 11 are obtained by subtracting the contact voltage drops from the continuous curves. The slope of the contact I–V curve in the output \( I_D-V_D \) plot corresponds to the sum of source and drain contact resistances, \( 2R_C = 200 \Omega \), causing the curves to “stretch” toward higher drain voltages, compared to the dotted I–V curves of the intrinsic OTFT. The stretch is 2–3V at high currents. The slope of the contact I–V curve in the transfer \( I_D-V_G \) plot corresponds only to the source contact resistance, \( R_C = 100 \Omega \), causing small “stretch” in the transfer curves of 1–2V, compared again to the dotted I–V curves of the intrinsic OTFT. While the stretches are not dramatic, the contact effects are affecting the I–V curves of the OTFT. The effects from contact resistance are more evident in the differential (small-signal) characteristics of the OTFT, shown in Figure 12.

![Differential characteristics](image)

**Figure 12.** Differential (small-signal) characteristics of transconductance \( g_m = \partial I_D / \partial V_G \) and output impedance \( (z_d = \partial V_D / \partial I_D) \), simulated with default values of the model parameters in the oTFT 2.04.01 compact model. Numerical data are in sheets “Transfer gm-VD”, “Transfer gm-VG”, “Output zd-VD” and “Output zd-VG” of file “(000)oTFT_2.04.01_nTFT_default.xls”.

In the left-hand plots of Figure 12, the transconductance \( g_m = \partial I_D / \partial V_G \) increases both with increasing the drain (\( V_D \)) and gate (\( V_G \)) bias. However, the higher is the bias, the higher is the impact from
contact resistances. The continuous-line curves in the left-hand plots represent $g_m$ at the OTFT terminals, while the dotted curves represent the intrinsic TFT. Observe that $g_m$ at the OTFT terminals is 20% lower than $g_m$ of the intrinsic TFT once both $V_G$ and $V_D$ are above 10V.

In the right-hand plots of Figure 12, the output impedance $z_d=\partial V_D/\partial I_D$ varies with the regime of operation of the OTFT. The impedance $z_d$ is low when the OTFT operates in linear regime at low drain bias and high gate bias, and $z_d$ increases in the saturation regime at high drain bias and low gate bias. Two specific features can be observed in the plots of $z_d$. One feature is that there is a peak, when $V_D=0$. The peak is due to the increase of the contact resistance from $R_C=100k\Omega$ at $V_D\neq0$ to $(R_C+R_{C_{\text{max}}})=400k\Omega$ when $V_D=0$, since the current becomes smaller than $I_{C_{\text{max}}}$ for the latter case – please see eq. (8). The second feature is that $z_d$ is peaking function of the bias. Observe that the maxima in the upper $z_d-V_D$ plot reduce when $V_G$ is higher. Similarly, observe the plateaus at low $V_G$ in the bottom $z_d-V_G$ plot reduce for higher $V_D$. These non-monotonic behaviors are due the channel modulation and leakage, which are more pronounced at high drain bias.

Note that the differential (small-signal) characteristics shown in Figure 12 are from AC simulation at very low frequency of 1 Hz. Increasing the frequency in the kHz range, significant contributions from capacitive currents occur, and the $g_m$ and $z_d$ characteristics depend on the elevation for the frequency, as shown in Figure 13.

![Figure 13](image-url)  
Figure 13. Frequency effects on transconductance $g_m$ and output impedance $z_d$, simulated with default values of the model parameters in the oTFT 2.04.01 compact model. Frequency elevation increases capacitive currents, increasing the minimum magnitude of $g_m$ and decreasing the maximum magnitude of $z_d$. Numerical data are in sheets “Transfer gm-VG” and “Output zd-VG” of file “(000)oTFT_2.04.01_nTFT_default.xls”.
The combined bias-frequency dependences are complicated and will not be discussed in this manual. However, the overall impact of frequency elevation is that capacitive currents increase with frequency, so that $g_m$ gets limited from the bottom, while $z_d$ gets limited from the top, and the frequency effects are more pronounced at low bias. This overall behavior is illustrated in Figure 13. In addition, when the capacitive currents dominate and limit $g_m$ and $z_d$, then the phases of $g_m$ and $r_d$ tend to $-90$ deg.

The transient simulations in the oTFT 2.04.01 compact model with the default values of the model parameters are now discussed. Mentioned in the introduction to Table 3 earlier in the beginning of Sec. 6, only selected data from transient simulations will be shown, since the waveform plots are too many to be all shown. In the selected waveform plots on below, the transient current $i_d(t)$ flowing into the drain terminal of TFT is shown and compared to the cycled step stimulus of either drain bias $v_D(t)$ or gate bias $v_G(t)$. The step of a stimulus is from 0 to $V_{Ddc}$ for $v_D(t)$ or from 0 to $V_{Gdc}$ for $v_G(t)$, representing on/off switching the TFT by output or input bias, respectively. Also, since there is no current limiting resistance in the simulation circuit (Figure 10), then the transitions of the voltage stimulus $v_D(t)$ or $v_G(t)$ between $=0$ and $\neq 0$ is with finite rate $|\partial v(t)/\partial t|<\infty$. Considering periodic cycling of the pulsing stimuli with repetition rate $f_{Hz}$ (frequency), then the period of the cycling is $1/f_{Hz}$, the transitions times (rise and fall times) are $0.1/f_{Hz}$, and the on/off plateaus of the pulsing stimulus are $0.4/f_{Hz}$, comprising 50% duty cycle of the cycling. Sinusoidal transition is used for the voltage stimuli, as the sinusoidal transition is built in component “vsource” from the analog library of the simulation environment for Spectre® simulator in Cadence®. Thus, as illustrated for $v_D(t)$ and $v_G(t)$ in Figure 14, the waveform of a voltage stimulus is described by

$$
\begin{align*}
&v_D(t) \\
\text{or } v_G(t) &\equiv v(t" = t - t') \equiv \begin{cases}
V_{Ddc} & \text{with } t' = \text{integer} \left( t \times f_{Hz} \right)/f_{Hz} : \\
V_{Gdc} & 1, \text{on-plateau for } 0.1/f_{Hz} \leq t" \leq 0.5/f_{Hz} \\
0, \text{off-plateau for } 0.6/f_{Hz} \leq t" \leq 1/f_{Hz} \\
\sin^2 (5 \pi f_{Hz} t") & \text{step for otherwise } t"
\end{cases}
\end{align*}
$$

(32)

The current $i_{ds}(t)$ through resistance-conductance elements (such as drain resistance $r_d$ or transconductance $g_m$) follows the shape of the voltage stimulus $v(t)$, so that

$$
i_{ds}(t) \propto v(t)
$$

(33)

where $I_{on}=I_D(V_{Gdc},V_{Ddc})$ is the static on-current at bias $(V_G,V_D)=(V_{Gdc},V_{Ddc})$, and $I_{on}$ is the same as $I_D$ in the I–V curves of the TFT at the particular bias point. The off-current $I_{off}$ is also a static current, and $I_{off}=I_D(V_{Gdc},V_D=0)=0$ in transient output waveforms or $I_{off}=I_D(V_G=0,V_{Ddc})$ in transient transfer waveforms. Usually $I_{on} >> I_{off}$, unless the gate on-bias brings the TFT toward sub-threshold regime of operation ($V_{Gdc}<0$ for n-type TFT). In the latter case of transfer transient waveforms in sub-threshold, $I_{on}$ and $I_{off}$ exchange each other, as illustrated in Figure 17 later.

Capacitive currents are time derivatives of voltages, and for a voltage stimulus $v(t)$ with sinusoidal transition, the current $i_c(t)$ through a capacitance $C$ is

$$
i_c(t) \equiv i_c(t" = t - t') \equiv \begin{cases}
+V_{Ddc} C & \text{with } t' = \text{integer} \left( t \times f_{Hz} \right)/f_{Hz} : \\
0 & \text{during plateaus}
\end{cases}
$$

(34)
The signs (+) and (−) in eq. (34) depend on whether the stimulus v(t) and the observation of ic are at the same side of the capacitor. Refer to Figure 14. When the stimulus vD(t) makes a step of the drain voltage, then the current ic of the capacitor C sums with the current ids of the channel, so that the terminal current is iD=(ids+iC), and the sinusoidal peak due to ic is with the polarity of the transition and plateau in the transient output waveform. Conversely, when the stimulus vG(t) makes a step of the gate voltage on the other side of the capacitor, then the current ic of the capacitor C subtracts from the current ids of the channel, and the sinusoidal peak due to ic becomes with polarity opposite to the polarity of the plateau in the transient transfer waveform. Note that the peak magnitudes are large at high frequency (fHz = 100 kHz), while at low frequency, the capacitive currents are negligible, and at fHz = 1 Hz, the terminal current iD=ids follows the waveform of the stimuli without any peak (although some distortion of the waveform shape is present due to the non-linear I–V dependences). Note also that the plateaus Ion and Ioff correspond to the DC current ID at the particular bias point (VGdc,VDdc), as mentioned above.

Figure 14. Summation of resistive and capacitive currents in (upper panel) transient output waveform iD(vD), and (lower panel) subtraction of the capacitive current from the transconductance current in transient transfer waveform iD(vG). Simulation result at high repetition rate fHz=100 kHz and high voltages VG=20V and VD=20V are shown, so that the plateaus and peaks are clearly visible. Numerical data are in sheets “Transient output” and “Transient transfer” of file “(000)oTFT_2.04.01_nTFT_default.xls”.

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The results from transient simulations of the oTFT 2.04.01 compact model with default values of model parameters are documented in sheets “Transient output” and “Transient transfer” in file “(000)oTFT_2.04.01_nTFT_default.xls”. In sheet “Transient output”, the drain bias is cycled between zero and $V_{Ddc}$, while the gate bias $V_{Gdc}$ was constant in time, comprising on/off at the output of the TFT. This cycling of the drain bias evaluates the TFT as a dynamic load. The roles of the gate and train biases are then exchanged, and in sheet “Transient transfer”, the gate bias is cycled between zero and $V_{Gdc}$, comprising on/off at the input of the TFT, while the drain bias $V_{Ddc}$ was constant in time. This cycling of gate bias evaluates the TFT as inverting amplifier, e.g., in inverters for digital circuits.

The results in sheets “Transient output” and “Transient transfer” are organized in a “matrix” format with three “dimensions”. The “matrix” organization is summarized in Figure 15. The frequency $f_{Hz}$ changes “horizontally” in the columns of each row of the “matrix”. The amplitude of the cycling stimulus changes “vertically” in the rows of each column. Several waveforms in each plot are for different values of the constant (un-cycled) bias voltage. Overall, the data in the upper-left corner of the “matrix” are for fast stimulus with large amplitude, while moving to the right and down, the cycling stimulus is slower and smaller in amplitude, respectively.

<table>
<thead>
<tr>
<th>Cycling voltage stimulus: $v_D(t)$ or $v_G(t)$</th>
<th>Fast cycling of stimulus ($f_{Hz}=100$ kHz)</th>
<th>Slower cycling of stimulus ($f_{Hz}=100$ kHz)</th>
<th>Slow cycling ($f_{Hz}=1$ Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Large amplitude of cycling stimulus</td>
<td>Large transient spikes ($Large signals$)</td>
<td>Small spikes ($High bias → Large signals$)</td>
<td>No spikes, but slow ($Large signals$)</td>
</tr>
<tr>
<td>Reducing amplitude of cycling stimulus …</td>
<td>…</td>
<td>($Constant bias effects$)</td>
<td>…</td>
</tr>
<tr>
<td>Small amplitude of cycling stimulus</td>
<td>Reduced spikes, but $Small signals$</td>
<td>Small spikes ($Low bias → Small signals$)</td>
<td>No spikes, but slow and $Small signals maybe$</td>
</tr>
</tbody>
</table>

Figure 15. Organization of data from transient simulation of oTFT 2.04.01 compact model in sheets “Transient output” and “Transient transfer” in file “(000)oTFT_2.04.01_nTFT_default.xls”.

Summaries of data from transient simulation of oTFT 2.04.01 compact model with default values of model parameters (Table 1 in Sec. 2.1) are shown in Figure 16 and Figure 17. In Figure 16, the drain bias $v_D(t)$ is cycled, and the transient output waveforms $i_D(v_D)$ represent a TFT operating as dynamic load. In Figure 17, the gate bias $v_G(t)$ is cycled and the transient transfer waveforms $i_D(v_G)$ represent a TFT operating as inverting amplifier. Overall, the behavior of the TFT under switching bias is that the transient “spikes” due to capacitive currents are large for high frequency ($f_{Hz} = 100$ kHz) and higher amplitudes (20V) of the cycling bias, which is in accordance with eq. (34). Reductions of switching bias amplitude reduce “spikes” amplitudes, as expected. Also as expected, reductions of transition rates of switching bias reduce magnitudes of the “spikes”. Observe that the “spikes” are small, almost buried in the larger static response of the TFT at $f_{Hz}=10$ kHz (middle columns in Figure 16 and Figure 17), and there is no spike visible at the low cycling rate of $f_{Hz} = 1$ Hz (right-hand columns in Figure 16 and Figure 17).
There are also differences between the output and transfer transient responses. One difference is the aforementioned opposite polarity of the “spikes” in output and transfer transient waveforms of the drain current $i_D(t)$. The “spikes” are with polarity of transition and plateau in transient output waveforms of $i_D(v_D)$ in Figure 16, whereas, the “spikes” are with opposite polarity in transient transfer waveforms of $i_D(v_G)$ in Figure 17. Another difference is that the plateaus are changing at different rates as function of the amplitude of the cycled bias. In Figure 16, the proportion between magnitudes of “spikes” and plateaus is virtually the same for any amplitude of the cycling drain bias $v_D(t)$. In Figure 17, in contrary, the proportion between “spikes” and plateaus varies with the amplitude of the cycling gate bias $v_G(t)$. In particular, owing to the super-linear dependence $I_D \propto (V_G - V_T)^{(1+\gamma)}$ in the linear regime of operation of the TFT, steep bias dependence $I_D \propto (V_G - V_T)^{(2+\gamma)}$ in the saturation regime and even steeper $I_D \propto [\exp(V_G - V_T)]^{(2+\gamma)}$ in the sub-threshold regime, the plateaus rapidly decrease when lowering the amplitude of the cycling gate bias; whereas, the quasi-static capacitances have much weaker sub-linear dependence on the gate bias [4], and the dominating overlap capacitances are constant, preserving almost linear dependence between “spikes” and amplitude of the cycling gate bias.
Figure 17. Summary of results from transient transfer simulations of oTFT 2.04.01 compact model with default parameters under on/off cycling of the gate bias $v_G(t)$. The transient transfer waveforms $i_D(v_G)$ represent the TFT as inverting amplifier, e.g., for digital circuits. Numerical data are in sheet “Transient transfer” of file “(000)oTFT_2.04.01_nTFT_default.xls”.

There are also other differences in the waveforms between cycling drain or gate bias. For example, comparing to the 50% duty cycles of the cycling voltage stimuli, the duty cycle of the current is increased in Figure 16 by cycling drain bias $v_D(t)$, whereas it is decreased in Figure 17 by cycling the gate bias $v_G(t)$. The reason for these changes of duty cycles is the different types of non-linearity in $I_D-V_D$ and $I_D-V_G$ dependences. In particular, the $I_D-V_D$ curves are sub-linear functions of $V_D$ with saturation, which suppresses high levels of current, while $I_D-V_G$ curves are super-linear functions of $V_G$, which emphasizes high levels of currents. Consequently, the different non-linearity in the $I_D-V_D$ and $I_D-V_G$ characteristics of the TFT distort differently the shape of the voltage stimuli $v(t)$. These distortions are not visible in the scales of Figure 16 and Figure 17. However, if the plateaus are with short durations, which is the case of using the TFT at high frequency, then the distortion due to non-linearity might be significant for the operation of circuits. In such cases, please, inspect closer the numerical data in sheets “Transient output” and “Transient transfer” of file “(000)oTFT_2.04.01_nTFT_default.xls”, in order to get insights.
6.2. oTFT 2.04.01 with default values of model parameters for p-type TFT (np=-1)

When downloaded from https://nanohub.org/groups/needs/compact_models, the Verilog-A code of the oTFT 2.04.01 compact model is for thin-film transistor (TFT) with n-type (electron) conduction (np=+1), and the default values correspond to an organic thin-film transistor (OTFT) with zero threshold voltage and mobility $\mu_o=0.1$ cm$^2$/V$s$ (uo=0.1e-4 m$^2$/V$s$). The default values and purposes of all model parameters are given in Table 1 in Sec. 2.1 and summarized also in Figure 10.

However, the majority of organic thin-film transistors (OTFTs) are with p-type (hole) conduction. Therefore, instantiate oTFT 2.04.01 compact model with model parameter np=-1 to convert the model for p-type TFT. The implementation of the oTFT model is accounting for polarity independently from other model parameters. The parameter “np” switches polarity and preserves magnitudes. Thus, using the default oTFT 2.04.01 compact model with only np=-1 changed, then the simulation of the p-type TFT should be identical to n-type TFT (np=+1) with inverted polarity of voltages and currents. Therefore, in this section, the simulations of p-type TFT with default parameters is compared to simulations of n-type TFT with default parameters.

The simulation schedule of p-type TFT (pTFT) with default parameters follows the schedule given in Table 3. The results from simulations of the default pTFT are documented in file “(001)oTFT_2.04.01_pTFT_default.xls”. The consistency between simulations of pTFT and nTFT with default parameters is verified in file “(002)oTFT_2.04.01_pTFT_vs_nTFT.xls”.

Figure 18. I–V curves of pTFT (np=-1, black color) with all other model parameters identical to oTFT 2.04.01 compact model with default parameters (gray color). Numerical data pTFT are in sheets “Output ID-VD” and “Transfer ID-VG” of file “(001)oTFT_2.04.01_pTFT_default.xls”.

The gray-color curves are for nTFT from Figure 11.
Figure 18 illustrates the central symmetry in the I–V characteristics of pTFT and nTFT. The symmetry implies that \( I_D(pTFT) = -I_D(nTFT) \) for \( (V_G, V_D)_{pTFT} = -(V_G, V_D)_{nTFT} \). Thus, summing the currents of corresponding points of the I–V curves, one expects \( I_D(pTFT) + I_D(nTFT) = 0 \). This equality is inspected in sheets “Output ID-VD” and “Transfer ID-VG” of file “(002)oTFT_2.04.01_pTFT_vs_nTFT.xls”, where all pairs of points have \( I_D(pTFT) + I_D(nTFT) = 0 \), except for only one point pair, which has negligible difference of \( 8 \times 10^{-28} \text{A} \).

The differential (small signal, AC) characteristics of pTFT and nTFT are also symmetric in respect to bias, and identical in values for \( (V_G, V_D)_{pTFT} = -(V_G, V_D)_{nTFT} \). This is illustrated for transconductance \( g_m \) in Figure 19. Note that the differential parameters are not inverted between nTFT and pTFT, as explained in [4]. Therefore, one expects \( g_m(pTFT) = g_m(nTFT) \) for \( (V_G, V_D)_{pTFT} = -(V_G, V_D)_{nTFT} \), and subtraction \( g_m(nTFT) - g_m(pTFT) = 0 \) was inspected in sheets “Transfer gm-VD”, “Output zd-VD”, “Transfer gm-VG” and “Output zd-VG” in file “(002)oTFT_2.04.01_pTFT_vs_nTFT.xls”. In these sheets, all point pairs have \( g_m(nTFT) - g_m(pTFT) = 0 \) and \( z_0(nTFT) - z_0(pTFT) = 0 \), including for phases, without any exception at any bias or frequency. Thus, oTFT 2.04.01 compact model is perfectly sustainable not only for currents and voltages in all regimes of operation of TFT, but also for derivatives.

![Figure 19](image_url)

Figure 19. Transconductance \( g_m \) of pTFT (np=−1, black color) is identical to \( g_m \) of nTFT (np=+1, gray color), but mirrored at opposite polarity of bias. Numerical data for pTFT are in sheets “Transfer gm-VG” of file “(001)oTFT_2.04.01_pTFT_default.xls”. The gray-color curves are for nTFT from Figure 12.

Since both the DC and AC characteristics are symmetric for nTFT and pTFT, then a symmetry in the transient response is also expected. This is illustrated in Figure 20. The symmetry is by inversion of polarity of voltages and currents. While the polarities are inverted, observe that the behaviors are the same. The peaks due to capacitive currents are with polarity opposite to the polarity of the transition between plateaus, since transient transfer waveforms are shown. Please, see the explanations in the previous Sec. 6.1. Note that the plateaus and peaks are of same magnitudes, although inverted between pTFT and nTFT. The “matrices” with the numerical data for pTFT are in sheets “Transient output” and “Transient transfer” in file “(001)oTFT_2.04.01_pTFT_default.xls”.

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Figure 20. Symmetry in the transient responses of pTFT (np=−1, black color) and nTFT (np=+1, gray color). Numerical data for pTFT are in sheet “Transient transfer” of file “(001)oTFT_2.04.01_pTFT_default.xls”. The gray-color curves are for nTFT from Figure 17 (upper-left corner of the “matrix”).

While looking perfectly symmetric in Figure 20, there are small differences between pTFT and nTFT in transient simulations, owing to the reduced accuracy in the iteration procedure of the transient simulation. Therefore, the differences are thoroughly inspected in sheets “Transient output” and “Transient transfer” in file “(002)oTFT_2.04.01_pTFT_vs_nTFT.xls”.

The analyses of the differences of voltages and currents in transient simulations of nTFT and pTFT indicate the following. The (min/standard deviation/max) differences for voltages are $\Delta v_D=(−0.78/0.05/+0.48)$mV in transient output waveforms for drain voltage $v_D$ and $\Delta v_G=(−01.37/0.11/+0.54)$mV in transient transfer waveforms for gate voltage $v_G$. The amplitudes for $v_D$ and $v_G$ are between 1V and 20V. Thus, the differences between transient simulations of nTFT and pTFT for voltage are smaller than 0.1%. The (min/standard deviation/max) differences for current are $\Delta i_D(v_D)=(-26/0.9/+3)$nA in transient output waveforms with cycling the drain voltage $v_D$ and $\Delta i_D(v_G)=(-69/4.5/+41)$nA in transient transfer waveforms with cycling the gate voltage $v_G$. The currents varied several decades, from ~10pA to ~50μA and the on-plateaus currents are between $i_D(v_D)=2.2−24$μA in transient output waveforms and between $i_D(v_G)=(0.08−24)$μA in transient transfer waveforms. Thus, while the differences between nTFT and pTFT are not “dramatic”, the differences between transient simulations of nTFT and pTFT for current can reach the range of the current, especially $\Delta i_D(v_G)−i_D(v_G)$ in transient transfer waveforms, when comparing transient current to the plateau current of the TFT operating in the sub-threshold regime. However, such uniformed comparison might be wrong, since the accuracy of transient simulation depends also on transition rates.
More insights for the inaccuracy in transient simulations is obtained when comparing the waveforms with the inaccuracy of the waveforms, as shown in Figure 21. The gray-color lines in the plots represent magnitudes of voltages and currents, and the black-color lines represent differences between nTFT and pTFT transient simulations. Observe that “large” differences are peaking at waveform transitions. The differences are small during plateaus. Thus, the differences perhaps are errors in the simulation rather than originating from the model. To support this conclusion, the settings for absolute and relative tolerances of the transient simulation are also indicated. In most cases, the differences $\Delta v_D$, $\Delta v_G$ and $\Delta i_D$ between data from simulation of nTFT and pTFT are smaller than the settings for absolute tolerances “abstol.v” for voltage and “abstol.i” for current. In occasions when the differences are larger, the differences are still not exceeding the limit for relative tolerance “reltol”=0.01%. There are also other “inconsistencies” in the plots. For example, the differences are not the same for consecutive transitions of the same waveform, e.g., there is no difference $\Delta v_D$, for the first pulse $v_D$ in the upper-left plot, while $\sim$1mV differences occur in the transitions in the second pulse of $v_D$, while these pulses are set identical and simulated in one run of the transient simulation. Such “memory” effects are unlikely to originate from the model, since all equations are algebraic, and there is no if-the-else statement in the Verilog-A code that might potentially create memory state.

Figure 21. Comparisons between transient simulations of pTFT and nTFT: magnitudes of cycling voltage stimuli $v_D(t)$ and $v_G(t)$ (gray color in the left-hand plots); differences between voltage magnitudes (black color in the left-hand plots); magnitudes of transient currents $i_D(t)$ (gray color in the right-hand plots) and differences between magnitudes of currents (black color in the right-hand plots), as extracted from transient output waveforms (upper plots) and transient transfer waveforms (lower plots). Numerical data are in sheets “Transient output” and “Transient transfer” of file “(002)oTFT_2.04.01_pTFT_vs_nTFT.xls”.
Thus, small differences between transient simulations with the oTFT 2.04.01 compact model are possible. However, such differences are not originating from the model, but from the settings of the transient simulation, because the differences are within the settings for tolerances of the transient simulation. The transient simulations are vulnerable to artifacts from settings, because conservative settings for high precision causes slow throughput from the simulator, owing to small time steps, increase of iterations and numerical truncations. Nevertheless, if the accuracy of the transient simulation is a concern, then repeat the transient simulation with slightly different settings for absolute and relative tolerances, and inspect for good reproduction of the results at different settings. The reproduction of results at different settings ensures that the transient simulation is not obscured by inappropriate settings.

Finally in this sub-section for pTFT, the oTFT 2.04.01 compact model has features for troubleshooting of problems with reproduction of transient simulations. In particular, the quasi-static sub-model in the oTFT compact model can be suppressed by setting model parameters selectQS=0, Lov=0 and eBov=0. These settings convert oTFT 2.04.01 compact model into truly static model, not affecting I−V curves and static differential characteristics. Then, addition of external capacitances of values C∗W∗(L+Lov)/2 between gate-drain and gate-source circuit nodes allow to test whether the transient simulation still encounters problems. (An example for such troubleshooting is not provided in this manual, because such a case was not encountered during the testing of the model.)

6.3. oTFT 2.04.01 for TFT with non-linear contacts

When downloaded from https://nanohub.org/groups/needs/compact_models, the Verilog-A code of the oTFT 2.04.01 compact model is for thin-film transistor (TFT) with n-type (electron) conduction (np=+1), and the default values of the model parameters correspond to an organic thin-film transistor (OTFT) with zero threshold voltage and mobility \( \mu_o = 0.1 \text{ cm}^2/\text{Vs} \) (\( \mu_o = 0.1 \times 10^{-4} \text{ m}^2/\text{Vs} \)). The default values and purposes of all model parameters are given in Table 1 in Sec. 2.1 and summarized also in Figure 10. The values for the model parameters for contacts correspond to an OTFT with linear contacts, since the parameter “Maximum (contact) resistance of terminal” \( R_{C_{\text{max}}} = 300 \text{k}\Omega \) is not much larger than the parameter “Minimum (contact) resistance of terminal” \( R_C = 100 \text{ k}\Omega \) and the parameter “Max current for \( R_{C_{\text{max}}} \)” \( I_{C_{\text{max}}} = 1 \text{nA} \) is low, so that the non-linearity of the contact (due to \( R_{C_{\text{max}}} \)) is at very low currents, compared to the channel currents \( I_D > 200 \text{nA} \) at normal bias of this OTFT (\( V_G > 4 \text{V}, V_D > 1 \text{V} \)).

However, some OTFTs do have non-linear contacts with high resistance. The non-linear contact manifests itself by several ways. Most often, the OTFT is said to have non-linear contact, when a sigmoid exists at the origin of the output \( I_D - V_D \) curves.

To introduce non-linear contact in oTFT 2.04.01 compact model, instantiate the model with larger values of the model parameters \( I_{C_{\text{max}}} > 300 \text{nA} \) and \( R_{C_{\text{max}}} > 1 \text{ M}\Omega > 10 \times R_C \), by keeping all other parameters with default values. Also, if the sigmoid in the \( I_D - V_D \) curves is very pronounced in shape, then increase the model parameter “Reduction exponent for \( R_{C_{\text{max}}} \)” \( n_{IC} \approx 1 \), but refrain increasing \( n_{IC} \) above, since \( n_{IC} > 1 \) means that the contact voltage drop reduces at high currents, which is unphysical and also may cause negative differential resistance and instability in simulations. (Just as precaution against improper use of the model, the range for \( n_{IC} \) is limited from 0.125 to 4, although the meaningful values for \( n_{IC} \) are between 0.5 and 1.0 – see the comment for \( n_{IC} \) in Table 1.)
Results from simulations of TFT with non-linear contacts are documented in file “(003)oTFT_2.04.01_nTFT_non-linear_contact.xls”. In the simulations, oTFT 2.04.01 compact model with default values of the model parameters (Table 1 in Sec. 2.1) is used, except for the parameters for non-linear contacts. According to above discussion, the values of these model parameters are increased to $R_{Cmax}=3M\Omega$, $I_{Cmax}=1\mu A$ and $n_{IC}=1$, which introduce strong non-linearity in the contact of the TFT. The TFT is with n-type (electron) conduction, since the default value of polarity parameter is $n_{p}=+1$. The simulation schedule again follows Table 3 and the format of the file “(003)oTFT_2.04.01_nTFT_non-linear_contact.xls” is identical with the format of the file for the default nTFT. The simulations of the default nTFT are thoroughly explained in Sec. 6.1. Thus, direct comparison can be made between the TFT with non-linear contacts and the default TFT with linear contacts. For example, one can compare the I–V curves of the TFT with non-linear contacts in Figure 22 below with the I–V curves of the default TFT with linear contacts in Figure 11 earlier in Sec. 6.1.

Figure 22. Current-voltage characteristics (I-V curves) of TFT with non-linear contacts. Except for $R_{Cmax}=3M\Omega$, $I_{Cmax}=1\mu A$ and $n_{IC}=1$, all other model parameters are with the default values (Table 1 in Sec. 2.1) of oTFT 2.04.01 compact model. Numerical data are in sheets “Output ID-VD” and “Transfer ID-VG” of file “(003)oTFT_2.04.01_nTFT_non-linear_contact.xls”. The double-line transfer and contact characteristics are for TFT with linear contacts from Figure 11.

Mentioned above, a non-linear contact causes a sigmoid at the origin of the output $I_d-V_D$ curves, as illustrated in the upper plots in Figure 22. The contact I–V curve (gray color) of non-linear
contacts has a diode-like shape. The diode is connected in series with the TFT channel. At low currents, almost the entire drain-source voltage drops on the contacts. At higher currents, the diode voltage drop does not increase much further, and higher portion of the drain voltage drops on the TFT intrinsic channel. For the particular values of the parameters, the non-linear contact is pronounced, and its nonlinearity affects even the logarithmic plot of the output $I_D-V_D$ curve, causing again sigmoidal deformation, instead of having the expected linear dependence between current and voltage in the linear regime of operation of the TFT. The non-linear contact also affects the transfer $I_D-V_G$ curves. However, since both shapes of the $I_D-V_G$ curve of the TFT and the non-linear contact are super-linear, no sigmoid can be observed in the $I_D-V_G$ curves. The sigmoid can be observed only in output $I_D-V_D$ curves, since the output curves of the intrinsic TFT are sub-linear and saturate at high drain voltage $V_D>(V_G-V_T)$.

The second effect of the non-linear resistance is the reduction of the currents of the TFT. Compare the $I$–$V$ curves in Figure 22 of the TFT with non-linear contacts with the $I$–$V$ curves in Figure 11 of the (default) TFT with linear contacts. Comparing the curves at high bias, the reduction is in the range of 30%-50%, from 14$\mu$A in the output curves for the TFT with linear contacts to 9$\mu$A in the output curves of the TFT with non-linear contacts, and from 11$\mu$A in the transfer curves for the TFT with linear contacts to 6.5$\mu$A in the transfer curves of the TFT with non-linear contacts. The reason for the reduction of the currents is mainly due to the voltage drop on the contact. This voltage is subtracted from the gate bias voltage, or equivalently added to the threshold voltage $V_T$. The source overdrive voltage $V_{GTS}=(V_G-V_T-V_{CS}-V_S)$ is reduced with the contact voltage drop $V_{CS}$ on the source contact. Consequently, the TFT current is reduced in the TFT with non-linear contact. The reduction of the overdrive voltage is approximately with the “built-in voltage” of the non-linear contact, which is $V_{CS}=R_{Cmax}$I$_{Cmax}=3\Omega \times 1\mu$A=3V in the particular example for TFT with non-linear contact. Twice larger reduction occurs for the drain bias voltage in the linear regime of operation of the TFT. Comparing the transfer characteristics of the TFTs with linear and non-linear contacts, there is a “shift” between the characteristics, as indicated with arrows in the transfer plot $I_D-V_G$ in linear scales. Note that characterization procedures may attribute this “shift” to an increase of threshold voltage.

The small-signal parameters are also affected by non-linear contact resistance. Inspect sheets” “Transfer gm-$VD$”, “Output zd-$VD$”, “Transfer gm-$VG$” and “Output zd-$VG$” in file “(003)oTFT_2.04.01_nTFT_non-linear_contact.xls”. Among these characteristics, the non-linear contact resistance affects strongly the output impedance $z_d=\partial V_D/\partial I_D$, as shown in Figure 23. The effects are at high gate bias ($V_G\geq 10V$) and low drain bias ($|V_D|<3V$) for the “linear” regime of operation of the TFT with non-linear contacts. At these conditions (black-color curves in Figure 23), $z_d \sim 2R_{Cmax}$ is large for $|V_D|<2V$, then $z_d$ decreases by increasing the drain voltage to $V_D \sim 7V$, and finally $z_d$ increases to high value at high drain bias $V_D>V_{GTS}$ in the saturation regime of operation of the TFT.

The gray-color curves in in Figure 23 are for the (default) TFT with linear contacts. These curves have been shown in Figure 12 in the previous Sec. 6.1. Comparing the black-color curves for the TFT with non-linear contacts to the gray-color curves for the TFT with linear contacts, the following observations can be made. First, the small and narrow peak of $z_d$ at $V_D=0$ due the small $R_{Cmax}=300k\Omega$ and $I_{Cmax}=1nA$ in the TFT with linear contacts becomes large and broad in the TFT with non-linear contacts, since $R_{Cmax}=3\Omega$ and $I_{Cmax}=1\mu$A are large in the TFT with non-linear contacts. Second, the differences between TFTs with linear and non-linear contacts vanish when reducing the gate bias toward and below the threshold voltage ($V_T=0$ in the example), observing that gray-color and black-color curves coincide for $V_D>3V$ at low gate bias.
$V_G=+4\text{V}$, and the curves overlap in the subthreshold regime for $V_G=-2\text{V}$. Third, the non-linear contact “shifts” the region of high-$z_d$ for saturation regime of operation of the TFT toward higher drain bias.

The above three observations in the output impedance $z_d-V_D$ curves are actually identity for presence of non-linear contact in the TFT. Peaking of $z_d$ at zero $V_D$ is possible, if the TFT contains a diode-like contacts in series with the channel, which implies carrier injection through Schottky or tunneling junction between terminal conductor (metal) and (organic) semiconductor. The vanishing of the $z_d$ peak at zero $V_D$ by lowering the gate bias indicates that the non-linear phenomenon is extrinsic and superimposed to the TFT, because the impedance of the intrinsic TFT changes with gate bias in the subthreshold regime, but the peak does not. The “shift” of the high-$z_d$ region for saturation regime toward higher $V_D$ indicates that the threshold voltage is not origin for the shift, since the direction of the shift should be in the opposite direction, if the $V_T$ is increased, as a characterization method based on $I-V$ curves may extract. Thus, discrepancy for saturation voltage $V_{DSat}=(V_G-V_T)$ in $z_d-V_D$ curves compared to $V_{DSat}=(V_G-V_T)$ in $I_D-V_D$ curves implies an elevation of the source potential due to contact voltage drop, rather than a larger threshold voltage.

![Graph](image.png)

Figure 23. Differential (small-signal) characteristics of output impedance ($z_d=\frac{\partial V_D}{\partial I_D}$) of TFT with non-linear contacts (black color) as function of drain bias voltage $V_D$, simulated with oTFT 2.04.01 compact model. Numerical data are in sheet “Output zd-VD” of file (003)oTFT_2.04.01_nTFT_non-linear_contact.xls”. Gray-color curves are for (default) TFT with linear contacts (from Figure 12).

Regarding contact effects in transient simulations. The effects are mainly in the plateaus, and much less in capacitive currents. The minor effect of contact resistance on capacitive currents in oTFT 2.04.01 is due to two reasons [4]. One reason is that the geometric overlap capacitances dominate over the channel capacitances in real OTFT, and second reason is that a quasi-static
model for charge is implemented in oTFT 2.04.01 compact model. The quasi-static assumption implies that the charge reflects instantly the static state of the TFT channel. Accordingly, the capacitive current sources are connected to the terminals (G,S,D) of the oTFT compact model, but not to the intrinsic nodes (G, S, D), because the latter connection would cause temporal feedback from capacitive (transient) currents and static currents through the contact resistances, which compromises the quasi-static assumption.

The effect of non-linear contact in transient simulation with oTFT 2.04.01 compact model is illustrated in Figure 24. The figure also summarizes the data analysis flow in file “(004)oTFT_2.04.01_nTFT_non-lin_vs_lin_contact.xls”.

As discussed in Sec. 6.1, the response in transient simulations consists of static and capacitive currents. In the oTFT 2.04.01 compact model, the static currents are due to the DC models, including the contact model. Therefore, performing transient simulation at low cycling rate of \( f_{Hz} = 1\, \text{Hz} \), one obtains the static response with plateaus that strongly depend on drain bias and contact linearity – observe in the second row of plots in Figure 24 that the levels of the
plateaus in the waveforms “static id(t) are very different between the TFTs with linear and non-linear contacts.

Increasing the cycling rate to \( f_{c} = 100 \text{ kHz} \), peaks of capacitive currents superimpose over the static waveform, as seen in the third row of plots in Figure 24. However, the peaks seem the same for different bias conditions and contact resistances, although the plateaus from the static response are different. Therefore, the static response waveforms (row 2) are subtracted from the transient response waveforms (row 3), and the capacitive currents are shown in the fourth row in Figure 24. Apparently, the capacitive current waveforms overlap and look identical for TFTs with linear and non-linear contact resistance. Subtracting the average of the waveforms at different biasing from each waveform at each biasing condition, one obtains the differences in the capacitive currents as function of the bias in the last row, on left for the TFT with linear contacts and on the right for the TFT with non-linear contact. The differences are small, not exceeding 5-6% of the capacitive currents. Thus, the bias dependence of the capacitive currents is weak, confirming that the geometric overlap capacitances in TFT dominate over the bias-dependent quasi-static capacitances of the TFT channel. Detailed reasoning why the overlap capacitances dominate in OTFTs is available in [4].

More interesting is when subtracting the capacitive currents from TFTs with linear and non-linear contacts. The subtraction is for each biasing condition, and occurrence of difference would imply a contact effect in the capacitive currents. However, the differences are negligible, less than 3%, as shown in the middle plot at the bottom of Figure 24, which means that the capacitance and quasi-static model in oTFT 2.04.01 are not interfering with each other. This independence is vital for the proper operation of the model in computer simulators, providing also convenience for the users of the model, since troubleshooting of unforeseen problems is unlikely necessary, when reconfiguring the model or fitting it to experimental data.

The independence of the capacitance and contact models originates from the quasi-static assumption. The charges in quasi-static models should instantly follow the biasing of the device, and notting should obscure the quasi-static charges to instantly follow the variation of bias. However, temporal variation of charge is capacitive current, and current sources for these currents are connected directly to the terminals of the TFT, bypassing the contact resistances, since otherwise there will be a feedback and the model will be not quasi-static. In fact, the small differences in the middle plot at the bottom of Figure 24 verifies that the quasi-static model is properly implemented in the Verilog-A code of the oTFT 2.04.01 compact model. One may argue that the quasi-static model for channel should be connected to the intrinsic nodes (and modify the code in this way). However, such modification is not recommended by the following three reasons [4]: connection of resistance or other impedance in series with quasi-static charge ruins the quasi-static assumption, because an extra pole is introduced; the dependences in the sub-models for contact, channel and charge are highly non-linear, and a connection of quasi-static current source to intrinsic node causes immediately a loop, potentially causing states and other problems for stability of numerical methods; there is no single rule that can direct users what will be the effect of interference between contact resistance and charge in the channel, thus, the user will lose control over the model. Finally, the channel capacitances are minor contributors to the dominant overlap capacitances in organic TFT, and it is a questionable worth to complicate the model without clear reason and without proof that the model will survive numerical methods. At the present arrangement of the Verilog-A code, the model is unconditionally stable for \( n_{C} \leq 1 \), which is the last comment on what is appropriate assignment of parameters for oTFT 2.04.01 compact model to keep it sustainable in computer simulators.
7. Examples for circuit simulations

This section provides a typical sequence for using oTFT 2.04.01 compact model in circuit simulation. The sequence is modeling of device characteristics, simulation of building block for a circuit, and simulation of the circuit. The circuit is 5-stage ring oscillator, which uses inverters with organic thin-film transistors (OTFTs). The analysis of the ring oscillator circuit with OTFTs can be found in [4] and experimental data are from [7], where a complete set of information for device, inverter and ring oscillator characteristics is given. Overall, the circuit is a ring oscillator made of low-voltage pentacene OTFTs. The OTFTs are unipolar of p-type conductance. Therefore, the inverter circuit consists of inverting transistor with high aspect ratio W/L=10 for high gain and a loading transistor in diode connection. The aspect ratio of the loading transistor is low W/L=1, in order to provide sufficient impedance when connected to the drain of the inverting transistor.

7.1. OTFT modeling with oTFT 2.04.01 for circuit simulation

When downloaded from https://nanohub.org/groups/needs/compact_models, the Verilog-A code of the oTFT 2.04.01 compact model is for thin-film transistor (TFT) with n-type (electron) conduction (np=+1), and the default values of the model parameters correspond to an organic thin-film transistor (OTFT) with zero threshold voltage and mobility μo=0.1 cm²/Vs (uo=0.1e-4 m²/Vs). The default values and purposes of all model parameters are given in Table 1 in Sec. 2.1 and summarized also in Figure 10.

To adapt the oTFT 2.04.01 compact model for circuit simulation, it is first necessary to model the devices used in the circuit. In this particular example, the OTFTs are p-type, so model parameter np=-1. Other parameters are adopted from the design information [7], as follows. The gate dielectric capacitance per unit area is C=7mF/m²=0.7μF/cm², two transistors with sizes (W=100μm, L=10μm) and (W=50μm, L=50μm) are used as inverting and load transistors in the inverter circuit, the charge carrier mobility is in the range of 0.4 cm²/Vs. The threshold voltages are in the range of −1V. The sub-threshold slope is in the range of 100mV/dec. The contact resistance (of two contacts) is 850 Ωcm. The geometric overlap of gate to drain/source is LOV=10μm. From this information, and after fitting the current-voltage characteristics (I−V curves) from [7], the actual values of the model parameters of the inverting and loading transistors are determined and listed in Table 5. The last row in the table includes interconnect resistance R_icon, which is not part of oTFT 2.04.01 compact model, but interconnect resistances are present in the layout of organic electronic circuits, and R_icon, was used to match the ring oscillator frequency and amplitude.

The match between the oTFT 2.04.01 compact models to the measured I−V curves (reported in [7]) is given in Figure 25. The match is good, considering the variability in OTFT characteristics. For example, one observes that the model output I−V curve in Figure 25 is slightly higher than the measured data, but the model I−V curve is slightly lower in the measured transfer I−V curve. The reason is that the currents in the two measurements actually differ for the same biasing condition (VG,VD). This is a typical situation for OTFTs, which have not very good reproducibility [8], [9]. Other detail is that the leakage in the I−V curves is low. Therefore, εBleck=εBleck=0 is taken, while the modulation of the drain current in saturation is high and εB=εB=200 is considered, although this value is inconsistent with back-film capacitance. Perhaps, space-charge limited conduction causes the drain conductance modulation, which results in high values of εB=εB, as noted in [3]. The numerical data from experiments and simulation of the I−V curves is recorded in file “(005)oTFT_2.04.01_pTFT_lowV_pentacene.xls”.  

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Table 5. Model parameters of the oTFT 2.04.01 compact model for two OTFTs used as inverting and loading transistors in inverters and ring oscillators in [7]

<table>
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<th>No</th>
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<th>Notation</th>
<th>Unit or [value]</th>
<th>Default value</th>
<th>Inverting transistor</th>
<th>Load transistor</th>
<th>Comments</th>
</tr>
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<td>oTFT model version</td>
<td>version_oTFT</td>
<td>numeric</td>
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<td>2.0401</td>
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<td>Channel width</td>
<td>W</td>
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<td>50 µm</td>
<td>Adopted from [7].</td>
</tr>
<tr>
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<td>Channel length</td>
<td>L</td>
<td>m</td>
<td>10 µm</td>
<td>10 µm</td>
<td>50 µm</td>
<td>Adopted from [7].</td>
</tr>
<tr>
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<td>Gate dielectric capacitance per area</td>
<td>C_I</td>
<td>F/m²</td>
<td>350 µF/m²</td>
<td>7mF/m²</td>
<td>7mF/m²</td>
<td>Adopted from [7].</td>
</tr>
<tr>
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<td>V</td>
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<td>-0.9 V</td>
<td>After fitting of I–V curves, close to -1V from [7].</td>
</tr>
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<td>m²/Vs</td>
<td>(10^{-5}) m²/Vs</td>
<td>(45\times10^{-6}) m²/Vs</td>
<td>(45\times10^{-6}) m²/Vs</td>
<td>After fitting of I–V curves, close to 0.4cm²/Vs from [7].</td>
</tr>
<tr>
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<td>Mobility enhancement factor</td>
<td>(\gamma)</td>
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<td>Voltage overdrive for (\mu_o)</td>
<td>V_(Vgamma)</td>
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<td>1 V</td>
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<td>V</td>
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<td>1 V</td>
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<td>Using V_SS=subthreshold slope=0.1V from [7].</td>
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<td>R_C</td>
<td>Ω</td>
<td>100 kΩ</td>
<td>50 kΩ</td>
<td>100 kΩ</td>
<td>Using 1/W scaling, with 2R_C×W=1kΩ≈850Ω from [7].</td>
</tr>
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<td>Maximum (contact) resistance of terminal</td>
<td>R_(Cmax)</td>
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<td>300 kΩ</td>
<td>150 kΩ</td>
<td>300 kΩ</td>
<td>Using R_(Cmax)=3R_C, the contacts are linear in these OTFTs.</td>
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<td>I_(Cmax)</td>
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<td>1 nA</td>
<td>1 nA</td>
<td>1 nA</td>
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<td>14</td>
<td>Reduction exponent for R_(Cmax)</td>
<td>(n_{R_C})</td>
<td>numeric</td>
<td>0.75</td>
<td>0.75</td>
<td>0.75</td>
<td>Using default in oTFT 2.04.01.</td>
</tr>
<tr>
<td>15</td>
<td>Resistance of the gate conductor</td>
<td>R_(Gmin)</td>
<td>Ω</td>
<td>1 Ω</td>
<td>1 Ω</td>
<td>1 Ω</td>
<td>Using default in oTFT 2.04.01.</td>
</tr>
<tr>
<td>16</td>
<td>Selector for Channel Modulation</td>
<td>n_(SCLC)</td>
<td>[...,4,...]</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>Using default in oTFT 2.04.01.</td>
</tr>
<tr>
<td>17</td>
<td>Relative permittivity at film’s “back” (for channel modulation)</td>
<td>(\varepsilon_B)</td>
<td>numeric</td>
<td>2</td>
<td>200</td>
<td>200</td>
<td>High values, indicating SCLC origin of channel modulation [3].</td>
</tr>
<tr>
<td>18</td>
<td>Relative permittivity at film’s “back” (for channel leakage)</td>
<td>(\varepsilon_{Bleak})</td>
<td>numeric</td>
<td>0.5</td>
<td>0</td>
<td>0</td>
<td>Low leakage in experimental data in [7].</td>
</tr>
<tr>
<td>19</td>
<td>Threshold voltage for non-linear leakage</td>
<td>V_TV</td>
<td>V</td>
<td>0 V</td>
<td>-1.04 V</td>
<td>-0.9 V</td>
<td>Using V_TV = V_T (irrelevant, since (\varepsilon_{Bleak}=0)).</td>
</tr>
<tr>
<td>20</td>
<td>Sheet resistance of the bulk of the semiconducting film</td>
<td>R_(BS)</td>
<td>Ω</td>
<td>(10^{12}\Omega/□)</td>
<td>(10\Omega/□)</td>
<td>(2Ω/□)</td>
<td>(2Ω/□)</td>
</tr>
<tr>
<td>21</td>
<td>Selector for quasi-static model</td>
<td>selectQS</td>
<td>[0,1]</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Using default in oTFT 2.04.01.</td>
</tr>
<tr>
<td>22</td>
<td>Drain/source length overlapping the gate</td>
<td>L_OV</td>
<td>m</td>
<td>30 µm</td>
<td>(\geq10) µm</td>
<td>(\geq10) µm</td>
<td>10 µm from [7]. Varied in simulation to match oscillation frequency</td>
</tr>
<tr>
<td>23</td>
<td>Relative permittivity at film’s “back” (for geometric capacitance)</td>
<td>(\varepsilon_{Bov})</td>
<td>numeric</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Using default in oTFT 2.04.01.</td>
</tr>
<tr>
<td>24</td>
<td>Minimum non-zero voltage difference</td>
<td>V_(min)</td>
<td>V</td>
<td>10 µV</td>
<td>10 µV</td>
<td>10 µV</td>
<td>Using default in oTFT 2.04.01.</td>
</tr>
</tbody>
</table>

Interconnect resistance | R_(icon) | Ω | \(-(3-6)R_C\) | > 0Ω | < 1 MΩ | Varied in simulation to match oscillation frequency |
Figure 25. I-V curves measured in [7] (symbols) and simulated (lines) with oTFT 2.04.01 compact model. Numerical data in file “(005)oTFT_2.04.01_pTFT_lowV_pentacene.xls”.

7.2. Simulation of inverter circuit with oTFT 2.04.01 compact model

Using the TFT models of the load and inverting transistors from the previous sec. 7.1, the circuit of the inverter is arranged as shown in Figure 26. The inverter circuit has input (IN), output (OUT) and bias terminals for positive supply (Vplus) and negative supply (Vminus). Since the pentacene OTFTs are with p-type (hole) conduction, the circuit is flipped inside the symbol, so that Vplus is above Vminus. Consequently, the inverting transistor is above the loading transistor, as illustrated in the third sub-figure in Figure 26.

From functional perspective, the inverting transistor acts as switch, while the load transistor acts as diode. Two possible connections of loads to the inverter output are possible. One connection is pull-up load (Z_{pull-up}) and second connection is pull-down load (Z_{pull-down}), as indicated in Figure 26. Assume that the inverting transistor is “strong” enough to drive the loads, so that OUT≈Vplus, when inverting transistor is switched on. However, when switched off, OUT≈Vminus only for pull-down load (since the inverter output is de-energized), whereas for pull-up load OUT≈V_T of the load transistor, since the current of Z_{pull-up} flows through the load.
transistor in diode connection. Thus, one expects OUT to swing between Vplus and Vminus for pull-down load and smaller swing for pull-up load of the inverter.

![Inverter circuit](image)

Figure 26. Inverter circuit, its schematic symbol with input, output and supply terminals, and possible connections of pull-up (Zpull-up) and pull-down (Zpull-down) loads. The switch and diode represent the functions of the inverting and load transistors.

The effect of the load connection to inverter output is simulated using the circuit in Figure 27. The upper half of the test circuit is for inverter with pull-down load. The lower half of the circuit is for inverter with pull-up load. Since the load in a circuit is normally connected to ground, then the supply is positive for the upper half and negative for the lower half of the test circuit. The load impedances R1||C1 and R2||C2 represent a typical 10:1 oscilloscope probe that has input impedance 10MΩ||10pF.

![Test circuit](image)

Figure 27. Test circuit for simulation of the effect of the load connection to inverter output. Numerical data in file “(006)oTFT_2.04.01_pTFT_lowV_pentacene_inverter.xls”.
In Figure 27, the source VGpulse cycles invIN between zero and $V_{Ddc}$ with repetition rate $f_{Hz}$ and half-sinusoidal rise and fall times $<0.01/f_{Hz}$. (See sec. 6.1 for details using a half-sinusoidal stimulus in transient simulations.) The constant voltage source VG2 shifts down invIN with the supply $V_{Ddc}$, so that invIN2 cycles between $-V_{Ddc}$ and zero. For DC analyses, VGpulse=0 and source VGdc ac is swept from 0 to $V_{Ddc}$, in order to obtain the static voltage transfer characteristics (VTC) of the inverters. (VG2=$V_{Ddc}$ in the VTC simulation is again shifting down invIN to invIN2 with the supply $V_{Ddc}$, as in the transient simulation.)

![Figure 28. Voltage transfer characteristics (VTC) of inverter with pull-down and pull-up loading.](image)

Figure 28 compares VTCs of the inverters with pull-down and pull-up loading at the inverter output. As expected from above discussion, the VTCs for invOUT of the inverter with pull-down load have larger swing ~60%−90% of the supply voltage, comparing with the smaller swing ~20%−45% for invOUT2 of the inverter with pull-up load. Thus, one may probably consider that pull-down loading is better.

However, looking at transient responses, the observations are different. In Figure 29, the waveform of the inverter with pull-up loading is with better-shaped plateaus, whereas the low-level plateau is mostly lacking in the inverter with pull-down loading (although the swing is still larger). Increasing the repetition rate to $f_{Hz}=10$kHz, peaks due to capacitive currents also emerge, as shown in Figure 30. The peaks have been clearly observed experimentally in [7]. However, close inspection between simulation and experimental data also indicates that the experimental peaks are larger and the transition from low to high is slower than in the simulation. The former is possibly due to higher overlap capacitances, and the latter is perhaps due to interconnect resistance ignored in the simulation. Therefore, these two factors will be considered by fitting the oscillation frequency of the ring oscillator in the next section. Indeed, the authors of [7] have observed 5-fold slower oscillation, compared to theoretical predictions, the simulation of the oscillator without overlap capacitances in [4] has confirmed the calculations in [7], and the
dominance of overlap capacitances in ring oscillators has been elaborated in [4] to explain the discrepancy between predictions and experiments.

Figure 29. Transient response of inverter with pull-down and pull-up loading at low repetition rate of $f_{Hz}=400\text{Hz}$. Numerical data in sheet “Transient transfer” of file “(006)oTFT_2.04.01_pTFT_lowV_pentacene_inverter.xls”.

Figure 30. Transient response of inverter with pull-down and pull-up loading at high repetition rate of $f_{Hz}=10\text{kHz}$. Numerical data in sheet “Transient transfer” of file “(006)oTFT_2.04.01_pTFT_lowV_pentacene_inverter.xls”. The bottom panel shows experimental data from [7] at supply bias 5V and same $f_{Hz}=10\text{kHz}$. 
7.3. Simulation of ring oscillator circuit with oTFT 2.04.01 compact model

The oTFT 2.04.01 compact models of the transistors in the circuit of the ring oscillator have been obtained in sec. 7.1 and summarized in Table 5. Using these models, the model of the inverters in the ring oscillator has been obtained in sec. 7.2, where also it has been noted that interconnect resistances and larger overlap capacitances should be considered by the simulation of the ring oscillator. Experimental data for the ring oscillator are available from [7]. Thus, one can proceed to simulation of the ring oscillator circuit.

The circuit of the ring oscillator is shown in Figure 31. This is a 5-stage ring oscillator with a chain of 5 inverters in the loop, and an output buffer. The circuit is repeated in two variants with pull-down and pull-up loading by an impedance $1 \Omega \parallel 150 \text{pF}$, which corresponds to 1:1 oscilloscope probe. Inspecting the layout in [7], the inverters are in proximity and resistors $R\text{icon}$ represent interconnection between two inverters. The trace closing the loop in the ring oscillator is long, and $3R\text{icon}$ is attributed to this interconnection. The buffer output is directly connected to a contact pad. Therefore, the interconnection resistance is lower from the output of the buffer to the contact pad, and a value of $\frac{1}{2}R\text{icon}$ is considered for this interconnection.

![Figure 31. Circuit of the ring oscillator deduced from information and layout in [7]. Numerical data from measurements and simulation are recorded in the sheets of file “(007)oTFT_2.04.01_pTFT_lowV_pentacene_ring_oscillator.xls”. The bottom panel shows the layout of the ring oscillator in [7].](image_url)

The ring oscillator is simulated by transient simulation, varying the supply bias $V\text{Ddc}$, gate–drain/source overlap varLOV and interconnect resistance $R\text{icon}$. The simulation schedule is summarized in Table 6. The results for the oscillation frequency, amplitudes and waveforms at the outputs $R\text{ObuffOUT}$ for pull-down loading and $R\text{ObuffOUT2}$ for pull-up loading are documented in file “(007)oTFT_2.04.01_pTFT_lowV_pentacene_ring_oscillator.xls”. The data
in this file are organized in several sheets for different overlap (varLov) and interconnect resistance (Ricon), as listed in Table 6.

Table 6. Conditions for transient simulation of ring oscillators with schematics in Figure 31

<table>
<thead>
<tr>
<th>sweep conditions</th>
<th>Parameter</th>
<th>[From : To, Step] or {list}</th>
<th>Record at conditions</th>
<th>Sheet name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient vs. time</td>
<td>Parameter</td>
<td>[0 : 11/fHz] record window with fHz ≈ oscillation frequency</td>
<td>[1/fHz : 11/fHz] frequency</td>
<td></td>
</tr>
<tr>
<td>Primary sweep</td>
<td>Time, t</td>
<td>[0 : 11/fHz] record window with fHz ≈ oscillation frequency</td>
<td>[1/fHz : 11/fHz] frequency</td>
<td></td>
</tr>
<tr>
<td>Secondary sweep</td>
<td>Vd (supply)</td>
<td>[2.5 : 5, 0.5] V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other sweep</td>
<td>varLov</td>
<td>{10, 30, 50}µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other sweep</td>
<td>Ricon</td>
<td>{0, 200, 820}kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Constants</td>
<td>RpullDown, RpullUp</td>
<td>1 MΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=10µm, Ricon=0kΩ</td>
<td>LOV=10u, Ricon=0k</td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=30µm, Ricon=0kΩ</td>
<td>LOV=30u, Ricon=0k</td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=50µm, Ricon=0kΩ</td>
<td>LOV=50u, Ricon=0k</td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=10µm, Ricon=200kΩ</td>
<td>LOV=10u, Ricon=200k</td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=30µm, Ricon=200kΩ</td>
<td>LOV=30u, Ricon=200k</td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=50µm, Ricon=200kΩ</td>
<td>LOV=50u, Ricon=200k</td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=10µm, Ricon=820kΩ</td>
<td>LOV=10u, Ricon=820k</td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=30µm, Ricon=820kΩ</td>
<td>LOV=30u, Ricon=820k</td>
</tr>
<tr>
<td>Output waveforms</td>
<td>RObufOUT(t)</td>
<td>RObufOUT2(t)</td>
<td>LOV=50µm, Ricon=820kΩ</td>
<td>LOV=50u, Ricon=820k</td>
</tr>
<tr>
<td>Compare to</td>
<td>experiment</td>
<td>osc.Hz, outVpk-pk, waveform</td>
<td>CompareExperiments</td>
<td></td>
</tr>
</tbody>
</table>

Two additional considerations have to be accounted for transient simulations of ring oscillators. One consideration is that the loop of 5 inverters comprises a circuit with negative feedback, which is stable at static condition (DC), and the ring oscillator circuits have to be “pushed” to begin oscillating. Therefore, the supply bias sources Vpositive and Vnegative in the circuit of Figure 31 are made to make steps from zero to Vd and –Vd, respectively, in the beginning of the transient simulation. Second consideration is that the primary sweep is time in transient simulations, while the oscillation frequency and the transient process in the beginning of the oscillation depend on the settings for supply and other parameters. Therefore, a timescaling variable fHz is used to set the duration of the simulation window [0:11/fHz] (time from 0 to 11/fHz), and the onset of the simulation in the time interval [0:1/fHz] is not recorded. The value of fHz was varied and chosen so that fHz is approximately equal to the oscillation frequency and the waveform records for the time windows [1/fHz:11/fHz] contain 8-15 periods of the oscillation.

The results for oscillation frequency (osc.Hz) and peak-to-peak amplitude of the voltage at the buffer output (outVpk-pk) of the ring oscillator are shown in Figure 32. Variations of overlap Lov and Ricon cause pronounced variations in osc.Hz and outVpk-pk. For example, taking Lov=10µm and Ricon=0kΩ, osc.Hz (thin black curve) is approximately one decade above the experimental data (circles) in the left-hand plot of Figure 32. Among all cases for Lov, Ricon and loading, the best fit to experimental data is at Lov=30µm, Ricon=820kΩ and pull-up loading (solid curve, red color). Reasonable fit is present also for {Lov=50µm, Ricon=200kΩ and pull-up load} (thin curve, green color) and {Lov=50µm, Ricon=0kΩ and pull-up load} (thin curve, blue color). The experimental data from [7] for amplitude is a single point (circle in the right-hand plot of Figure 32), and all cases for pull-up load coincide with experiment, while all cases for pull-down load have considerably larger amplitudes. Overall, the comparison between simulation cases and experiment implies that the gate-drain/source overlap Lov≈30µm (3 times larger than
the geometrical overlap $L_{OV} \approx 10\mu m$ reported in [7]), and the interconnect resistance is also large, $R_{icon}=(0.8-1.0)M\Omega$. As rules of thumb, the “electrical” overlap in organic inverter is 3 times the geometric overlap in OTFTs and the interconnect resistance in the inverter is 3 times the contact resistance of the OTFTs in the inverter.

Comparison of waveforms from simulation of the ring oscillator to experimentally measured waveform [7] is given in Figure 33. The four plots from simulation are chosen from all plots in the sheets of file “(007)oTFT_2.04.01_pTFT_lowV_pentacene_ring_oscillator.xls” to correspond to the black, blue, green and red color curves in Figure 32. Clockwise from the top-left plot, the overlap $L_{OV}$ and interconnect resistance $R_{icon}$ are increased to better match the experimentally observed oscillation frequency at supply bias $V_{Ddc}=5V$. The waveforms also evolve in this order. For minimum $L_{OV}=10\mu m$ and $R_{icon}=0k\Omega$, the waveforms are almost sinusoidal. Increasing $L_{OV}$, the waveforms for pull-down loading tend to triangular shape, and the waveforms for pull-up loading tend to have tilted plateaus. Increasing $R_{icon}$, the triangular shape for pull-down loading skews to saw-tooth shapes, and the shapes for pull-up loading become more trapezoidal. Scaling the almost sinusoidal experimental waveform to the axes scales of the plots of the simulated waveforms, one observes that amplitudes and periods match well, but there are differences in the waveform shapes. Thus, the simulation of the ring oscillator is consistent for amplitudes and frequency, but less reliable for waveform shapes. The reason is that there are details not attended in the modeling of the transistors and interconnects. Therefore, for precise simulation of organic circuits, one has to have elaborated models for all layout components. The oTFT 2.04.01 is good for the TFT, but certainly, the circuit simulation needs same-quality models for all other components in the circuit. The representation of interconnects sole by resistance perhaps is oversimplification in the simulation of the ring oscillator.
Figure 33. Waveforms at the outputs (OUT) of the ring oscillators with pull-down and pull-up loads from simulation with oTFT 2.04.01 compact model, compared to experimental data from [7] (bottom-right plot). Clockwise from top-left plot: gray, blue, green and red colors of backgrounds correspond to colors of curves in Figure 32. Numerical data from simulation are recorded in the sheets of file “(007)oTFT_2.04.01_pTFT_lowV_pentacene_ring_oscillator.xls”.

8. Summarizing comments

This manual presented the implementation of oTFT 2.04.01 compact model in a Verilog-A code. The model is aimed to support device and circuit simulations of thin-film transistors (TFTs) that have bias enhancement of charge carrier mobility and significant contact resistances. These two effects are typically present in organic thin-film transistors (OTFTs).

The modular and hierarchical structure of oTFT 2.04.01 compact model “mirrors” the TFT structure, having sub-models for DC current, contact resistance, channel modulation, leakage, quasi-static charge and geometrical overlap capacitances, as explained in Secs. 1 and 2. The modular structure of oTFT 2.04.01 compact model fully complies with the requirements [1] for behavioral consistency, upgradability and reducibility and other requirements, having “rails” for device terminals, intrinsic nodes and control of the sub-models connected between the “rails”. All sub-models can be suppressed, as the need for modeling of OTFTs evolves, although the DC sub-model (generic TFT charge drift DC model) should be always kept, since it determines the overall behavior of oTFT 2.04.01 compact model. The Verilog-A code also contains a monitor for internal quantities, which is not part of the oTFT compact models, but it is a useful feature for debugging and detailed investigation of behaviors of sub-models, e.g., for contacts. Sec. 3 explains implementation details that allow operation in extreme conditions, such as very high or zero biasing. Secs. 4, 5, 6 and 7 provide for installation, customization and verification of the Verilog-A code, and for device and circuit simulation with oTFT 2.04.01 compact model.
9. References


