A Verilog-A Compact Model for Negative Capacitance FET

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1. Introduction

Continuous downscaling of the physical dimensions of MOSFET has helped to increase the transistor density, and improved the performance of the integrated circuit (IC). It has been difficult however to reduce the supply voltage ($V_{DD}$) significantly below 1V without sacrificing the ON current and the ON/OFF ratio, making it difficult to reduce the power density [1], [2]. The increasing thermal resistance of the novel transistors (FINFET, SOI-FET, or Gate-all-around (GAA) FET has further acerbated the problem. Indeed, temperature rise due to self–heating ($\Delta T = P \times R_{TH}$) affects the reliability of the transistors [3], [4]. Therefore, any scheme to scale down the bias voltage has the potential to reduce power consumption and self-heating significantly. One of the options to reduce $V_{DD}$ involves improving the sub-threshold slope ($S$) of a transistor by overcoming Boltzmann limit ($S=60$ mV/dec). Negative capacitance (NC) dielectric such as ferroelectric (FE) material improves $S$ through amplification of gate bias [5]–[12] in a NC-FET (Fig. 1(a)). In this work, we develop a verilog-A compact model of a generic NC-FET [11], [12]. This manual discusses the theoretical model, the circuit representation, and results through illustrative examples of the NC-FET.

2. Terminal Voltages and Parameters List

![Diagram of NC-FET](image)

Fig. 1 (a) The schematic diagram describes the geometry of the NC-FET. (b) Symbolic representation of the NMOS NC-FET. (c) The NC dielectric is represented as a dependent voltage source ($V_{FE}$) for HSPICE simulation. The NC-FET is represented by two series-connected components, i.e., the NC dielectric and the MOSFET.

![Diagram of Parasitic Components](image)

Fig. 2 (a) Ferroelectric acts as an additional gate dielectric capacitor with the conventional MOSFET. (b) All the parasitic components: source resistance ($R_S$), drain resistance ($R_D$), gate-
source overlap and fringing capacitance ($C_{ov}$) and gate-drain overlap and fringing capacitance ($C_{ov}$) are included in the analysis.

2.1. Terminal Voltages

The NC-FET has two components: (i) NC dielectric and (ii) the conventional MOSFET.

(i) **NC dielectric**: The NC dielectric is treated as an external capacitor connected in series to the gate of the conventional MOSFET. For the DC analysis, the inclusion of a capacitor in the gate terminal as an external element cannot provide meaningful results. Therefore, in HSPICE simulation, NC dielectric element is represented as a dependent voltage source which is a function of gate charge. The inclusion of the NC dielectric as a voltage source enables circuit simulation. Using the same concept multiple layers of NC dielectric as dielectric stack can be considered in the model.

(ii) **Conventional MOSFET**: The second element is a conventional MOSFET transistor with drain, gate, source, and body terminals. This model and method work for any structure (planar, double gate, FinFET, SOI FET, GAA-FET, etc) and model (MVS/BSIM4/BSIM-CMG/etc) of the MOSFET so long it is supported by the circuit simulator.

In addition to the standard elements, we introduce a dummy node to both the NC dielectric and the Conventional MOSFET. Therefore, the NC dielectric is now represented by 3 terminals and the MOSFET by 5 terminals. The dummy node (as a voltage terminal) exchanges information regarding the gate charge between the two elements. HSPICE solves the circuit of the NC-FET self-consistently to compute the unknown variables (voltages, currents, etc). The introduction of the dummy node for the MOSFET requires access to the source code. The modified source code of BSIM4 and MVS are provided along with the source code of NC dielectric.

The nodes and corresponding node voltages of the NC dielectric and conventional MOSFET are defined as follows:

**NC dielectric:**

<table>
<thead>
<tr>
<th>Node</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>ncp</td>
<td>Electrode with positive bias</td>
<td>V(ncp)</td>
</tr>
<tr>
<td>ncn</td>
<td>Electrode with negative (or zero bias)</td>
<td>V(ncn)</td>
</tr>
<tr>
<td>qg_as_v</td>
<td>Dummy node to input the gate charge</td>
<td>V(qg_as_v)</td>
</tr>
</tbody>
</table>

**Conventional MOSFET (MVS/BSIM/etc):**

<table>
<thead>
<tr>
<th>Node</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>drain</td>
<td>Drain voltage</td>
<td>V(drain)</td>
</tr>
<tr>
<td>gate</td>
<td>Gate voltage</td>
<td>V(gate)</td>
</tr>
<tr>
<td>source</td>
<td>Source voltage</td>
<td>V(source)</td>
</tr>
<tr>
<td>bulk</td>
<td>Bulk voltage</td>
<td>V(bulk)</td>
</tr>
</tbody>
</table>
2.2. Parameters List

Parameters used in the negative capacitance FET model are listed below. Table also lists the physical meaning of each parameter.

<table>
<thead>
<tr>
<th>Math Symbol</th>
<th>Verilog-A Symbol</th>
<th>Description</th>
<th>Default</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha_{FE}$</td>
<td>alpha</td>
<td>Alpha coefficient of the ferroelectric</td>
<td>$-1.8 \times 10^{11}$</td>
<td>cm/F</td>
</tr>
<tr>
<td>$\beta_{FE}$</td>
<td>beta</td>
<td>Beta coefficient of the ferroelectric</td>
<td>$5.8 \times 10^{22}$</td>
<td>cm$^5$/F/Coul$^2$</td>
</tr>
<tr>
<td>$t_{FE}$</td>
<td>tFE</td>
<td>Thickness of the ferroelectric dielectric</td>
<td>$10 \times 10^{-7}$</td>
<td>cm</td>
</tr>
</tbody>
</table>

For details regarding the physical interpretation of the model parameters, see Ref. [6]–[9].

3. Model System and Equations

We develop the model of the NC-FET [11], [12] by integrating the BSIM4/MVS model [13] of the conventional short channel MOSFET with the Landau theory of negative capacitor [5]. The subthreshold swing of a MOSFET is defined as

$$S = \frac{dV_{GS}}{d\log_{10}(I_D)} = \left(\frac{dV_{GS}}{d\psi_S}\right)\left(\frac{d\psi_S}{d\log_{10}(I_D)}\right) = m \times p$$  \hspace{1cm} (1)

where, $V_{GS}$ is the applied gate bias, for NC-FET it is $V_{G(\text{NC})}$. $I_D$ is the drain current, $\psi_S$ is the surface potential. The body-factor $m$ can be obtained from the voltage divider rule assuming the gate-source and gate-drain overlap capacitances ($C_{OV}$) have negligible effect on gate charge ($Q_G$).

$$m = \left(\frac{dV_{GS}}{d\psi_S}\right) = \left(1 + \frac{1}{C_{S}}\frac{1}{C_{OX}} + \frac{1}{C_{FE}}\right)$$  \hspace{1cm} (2)

**Landau model for the negative capacitor**: The Gibb’s free energy of a ferroelectric material is represented by a two well energy landscape, as follows,

$$U = \alpha_{FE}Q_G^2 + \beta_{FE}Q_G^4 - \frac{V_{FE}Q_G}{t_{FE}}.$$  \hspace{1cm} (3)
The potential \( V_{FE} \) - charge \( Q_G \) relation of the ferroelectric material is represented from eq (3) as

\[
V_{FE} = 2\alpha_{FE} t_{FE} Q_G + 4\beta_{FE} t_{FE} Q_G^3
\]  

(4)

From eq (4) we can write the capacitance \( C_{FE} \) - charge \( Q_G \) relation of the ferroelectric material as

\[
C_{FE} = \frac{1}{2\alpha_{FE} t_{FE} + 12\beta_{FE} t_{FE} Q_G^2}
\]  

(5)

In this work, negative capacitance dielectric and conventional MOSFET are represented as two different components. The I-V and C-V of the NC-FET are computed through charge and potential balance in HSPICE. We represented the ferroelectric dielectric as a dependent voltage source which is a function of \( Q_G \). To account this dependency we modified the available verilog-A models of MVS/BSIM4.
4. Device Characteristics

To illustrate the model of the NC-FET, we simulate the performance of the conventional MOSFET (NCFET with $t_{FE}$=0 nm) and the behavior of the NC dielectric capacitor in Fig. 3. Then we evaluated the characteristics of the NMOS NC-FET, PMOS NC-FET, NC-FET CMOS inverter in Figs. 4, 5, and 6, respectively. The improved performance of the NC-FET sustains for different gate lengths (Fig. 7). The transient performance of the NC-FET CMOS inverter is evaluated in Fig. 8 (in Appendix).

Fig. 3 (a) C-V characteristics of the conventional MOSFET. At $V_{GS}$=0 V, gate capacitance is dominated by the gate-source ($C_{OV}$) and gate-drain ($C_{OV}$) overlap and parasitic capacitances. (b) Polarization ($P$) vs applied bias ($V_{FE}$) of the ferroelectric dielectric $P$(VDF-TrFE). $\alpha_{FE}$ and $\beta_{FE}$ coefficients of the ferroelectric dielectric are extracted through fitting of eq (4) with experiment (from Ref. [10], [14]). (c) Energy landscape for different applied bias ($V_{FE}$) (eq (3)).
polarization \( (P) \) vs applied bias \((V_{FE})\) (eq 4), and polarization \( (P) \) vs capacitance \((C_{FE})\) (eq 5) of the ferroelectric dielectric.

\[
L_g = 32 \text{ nm} \quad V_D = 1 \text{ V} \quad \text{BSIM4} \quad P(VDF-TrFE)
\]

\[
dV_{FE} = \frac{C_G}{C_G + C_{FE}} dV_{G(NC)}
\]

Fig. 4 (a) \( I_D - V_{GS} \) and (b) Gate charge \((Q_G)\) vs \( V_{GS} \) characteristics of the NMOS NC-FET for different \( t_{FE} \) using BSIM4 and Landau theory. (c) Different potential components of the NC-FET: applied gate bias \((V_{G(NC)})\), voltage across the ferroelectric dielectric \((V_{FE})\), and voltage in the intermediate node \( G(MOS), V_{G(MOS)} \). (d) Subthreshold slope \((S)\) vs \( V_{GS} \) for different \( t_{FE} \). (e) \( Q_G \) vs \( V_{FE} \) profile from the circuit simulation (red) and from eq (4) (blue).
Fig. 5 (a) Symbolic representation of the PMOS NC-FET. (b) $I_D$-$V_{GS}$ and (c) Gate charge ($Q_G$) vs $V_{GS}$ characteristics of the PMOS NC-FET for different $t_{FE}$ using BSIM4 and Landau theory. (d) Different potential components of the NC-FET: applied gate bias ($V_{G(NC)}$), voltage across the ferroelectric dielectric ($V_{FE}$), and voltage in the intermediate node $G$ (MOS), $V_{G(MOS)}$. (e) Subthreshold slope ($S$) vs $V_{GS}$ for different $t_{FE}$.

Fig. 6 (a) Symbolic representation of the NC-FET CMOS inverter. (b) Performance comparison of the different CMOS inverters. With the incorporation of NC dielectric, NMOS (black arrow) and PMOS (magenta arrow) are turning-on at lower effective threshold voltage compared to conventional counterpart.
Fig. 7 $I_D$ vs $V_{GS}$ characteristics of the NMOS NC-FET from (a) BSIM4 and Landau theory and (b) MVS and Landau theory for 45 nm technology node. Subthreshold slope ($S$) vs $V_{GS}$ of the NMOS NC-FET from (a) BSIM4 and Landau theory and (b) MVS and Landau theory for 45 nm technology node.

5. Summary

The manual describes the electrical model of the NC-FET by integrating MVS/BSIM4 model with Landau theory. Future work involves improving the physics of the model and inclusion of the transient response of the ferroelectric material. Please contact Muhammad A. Wahab (mwahab@purdue.edu) regarding any questions/comments about the negative capacitance FET compact model.

References


M. A. Alam, P. Dak, M. A. Wahab, and X. Sun, “Physics-Based Compact Models for Insulated-Gate Field-Effect Biosensors, Landau Transistors, and Thin-Film Solar Cells,” in *IEEE Custom Integrated Circuits Conference (CICC)*, September 28-30, 2015, San Jose, CA, USA.

S. Rakheja and D. Antoniadis, “MVS Nanotransistor Model (Silicon),” nanoHUB.

Appendix

A. Transient performance

Fig. 8 Our developed NC-FET model can be used for transient simulation of CMOS circuits. Results of the transient simulation of the NCFET CMOS inverter of Fig. 6(a). (a) Input gate pulse ($V_{in}$) vs time ($t$). (b) Inverter output ($V_{out}$) vs t. (c) Zoomed version of a cycle from (b) highlights the effect of the negative capacitor on performance of NC-FET inverter. Slow response of the ferroelectric material is neglected in the transient simulation. In practical device material response can be a limiting factor and therefore, must be accounted. Also, the representation of the negative capacitor as dependent source cannot account the transient behavior accurately.
B. Parameters of Conventional MOSFET

Conventional MOSFET parameters are directly collected or extracted from the predictive technology model (http://ptm.asu.edu/). A sample set of parameters for NMOS device is provided below as an illustration.

<table>
<thead>
<tr>
<th>Math Symbol</th>
<th>Description</th>
<th>$L_G = 45$ nm (Default value)</th>
<th>$L_G = 32$ nm (Default value)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W$</td>
<td>Channel width</td>
<td>1</td>
<td>1</td>
<td>μm</td>
</tr>
<tr>
<td>$EOT$</td>
<td>Effective oxide thickness</td>
<td>0.9</td>
<td>0.75</td>
<td>nm</td>
</tr>
<tr>
<td>$\varepsilon_{OX}$</td>
<td>Oxide dielectric constant</td>
<td>3.9</td>
<td>3.9</td>
<td></td>
</tr>
<tr>
<td>$\varepsilon_0$</td>
<td>Free space permittivity</td>
<td></td>
<td></td>
<td>F/cm</td>
</tr>
<tr>
<td>$N_{Sub}$</td>
<td>Substrate doping density</td>
<td>$6.5 \times 10^{18}$</td>
<td>$8.7 \times 10^{18}$</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$V_{T0}$</td>
<td>Threshold voltage</td>
<td>0.3423</td>
<td>0.3558</td>
<td></td>
</tr>
<tr>
<td>$\mu$</td>
<td>Carrier mobility</td>
<td>295</td>
<td>238</td>
<td>cm$^2$/V$S$</td>
</tr>
<tr>
<td>$v_{s0}$</td>
<td>Saturation velocity</td>
<td>$1.595 \times 10^7$</td>
<td>$1.821 \times 10^7$</td>
<td>cm/$S$</td>
</tr>
<tr>
<td>$R_S = R_D$</td>
<td>Source/Drain resistance</td>
<td>52.5</td>
<td>40</td>
<td>Ω &amp; μm</td>
</tr>
<tr>
<td>$C_{GSOV} = C_{GDOV}$</td>
<td>Source/Drain overlap capacitance</td>
<td>$2.1 \times 10^{12}$</td>
<td>$2 \times 10^{12}$</td>
<td>F/cm</td>
</tr>
<tr>
<td>$n$</td>
<td>Subthreshold coefficient</td>
<td>1.15</td>
<td>1.15</td>
<td></td>
</tr>
<tr>
<td>$\delta$</td>
<td>DIBL factor</td>
<td>0.0332</td>
<td>0.0424</td>
<td>V/V</td>
</tr>
<tr>
<td>$\beta$</td>
<td></td>
<td>1.8</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>$\alpha$</td>
<td></td>
<td>3.5</td>
<td>3.5</td>
<td></td>
</tr>
<tr>
<td>$\gamma$</td>
<td></td>
<td>0.1</td>
<td>0.1</td>
<td>$\sqrt{V}$</td>
</tr>
</tbody>
</table>

C. HSPICE toolkit

In order to analyze the HSPICE output data, HSPICE toolkit available in Matlab is used. This can be downloaded from http://www.cppsim.com/InstallFiles/hspice_toolbox.tar.gz. Make sure to add it in the Matlab path. You can use the following Matlab command to add this to the default path: `addpath(location_of_hspice_toolbox_folder)`.

D. Simulating HSPICE netlist

HSPICE code can be run on file “filename.sp” using following command: `hspice filename.sp`

E. Checklist for model analysis

1. Install the HSPICE toolkit to enable data extraction from HSPICE files.
2. Download the complete package in folder NCFET. Compile the following HSPICE files

   NCFET\Negative Capacitance FET Model 1.0.0 HSPICE
   Netlists\ncfet_nmos_bsim4_Lg32nm\ncfet_nmos.sp

   NCFET\Negative Capacitance FET Model 1.0.0 HSPICE
   Netlists\ncfet_pmos_bsim4_Lg32nm\ncfet_pmos.sp
3. Compilation of the files will generate the filename.sw0 and filename.tr0 files for dc and transient simulations respectively. These files can be analyzed using the perform_analysis.m file.

4. Go to the folder containing the “perform_analysis.m” file and run it.