# A Verilog-A Compact Model for Negative Capacitance FET

**Version 1.1.1**

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## Table of Contents

1. Introduction........................................................................................................................................3
2. Terminal Voltages and Parameters List............................................................................................3
   2.1. Terminal Voltages ....................................................................................................................4
   2.2. Parameters List .......................................................................................................................5
3. Model System and Equations .............................................................................................................6
4. Device Characteristics .......................................................................................................................7
5. Summary ...........................................................................................................................................12

References............................................................................................................................................13

Appendix............................................................................................................................................15
   A. Transient performance ..................................................................................................................15
   B. Parameters of Conventional MOSFET ......................................................................................16
   C. HSPICE toolkit ............................................................................................................................16
   D. Simulating HSPICE netlist ...........................................................................................................16
   E. Checklist for model analysis ........................................................................................................16
Update notes

(3/10/2017)

Added the following text regarding difference between Purdue and MIT models:

“The Purdue NC-FET model is modular with separate implementations for the FE model and for the MOSFET model (either MVS or BSIM). With slight modifications to the MOSFET models, it is possible to hook the modules together and have a composite NC-FET model. MVSNC on the other hand is integrated, i.e. there are no extra nodes for the NC-FET model. The integration may make MVSNC run faster for large circuits.”

Also updated author contact information
1. Introduction

Continuous downscaling of the physical dimensions of MOSFET has helped increase transistor density and improved the performance of the integrated circuit (IC). It has been difficult however to reduce the supply voltage ($V_{DD}$) significantly below 1 V without sacrificing the ON current and the ON/OFF ratio. This “1V-limit” translates to a floor for minimum power consumption ($P_{min}$) [1], [2]. The increasing thermal resistance ($R_{TH}$) of the novel transistors (FINFET, SOI-FET, or Gate-all-around (GAA) FET) has further acerbated the problem. Indeed, temperature rise due to self-heating ($\Delta T = P \times R_{TH}$) affects the reliability of the transistors [3], [4]. Therefore, any scheme that reduces $V_{DD}$ will also reduce power consumption and self-heating. One option to reduce $V_{DD}$ involve improving the sub-threshold slope ($S$) of a transistor by overcoming Boltzmann limit ($S=60$ mV/dec). Negative capacitance (NC) dielectric such as ferroelectric (FE) material improves $S$ through amplification of gate bias [5]–[13] in a NC-FET (Fig. 1(a)). In this work, we developed a verilog-A compact model of a generic NC-FET [11], [12]. In the model, NC dielectric is integrated as gate dielectric stack with conventional MOSFET. The model deployed involves a two-component circuit: we used MVS and BSIM4 for classical MOSFET and a non-linear voltage source for NC dielectric. The MOSFET model and Landau theory work self-consistently to provide the characteristics of NC-FET. This manual discusses the theoretical model, the circuit representation, and results through illustrative examples of the NC-FET.

The Purdue NC-FET model is modular with separate implementations for the FE model and for the MOSFET model (either MVS or BSIM). With slight modifications to the MOSFET models, it is possible to hook the modules together and have a composite NC-FET model. MVSNC on the other hand is integrated, i.e. there are no extra nodes for the NC-FET model. The integration may make MVSNC run faster for large circuits.

For someone new to NC-FET, a tutorial (https://nanohub.org/resources/23157) from Purdue University provides a helpful resource [14]. Beside verilog-A, we separately deployed the MATLAB model of NC-FET (https://nanohub.org/resources/23185) [15]. This revised verilog-A version (1.1.0) of NC-FET includes (i) dipole response of the NC dielectric in transient simulation, (ii) explicit definition of all variables (1.0.0), and (iii) a modified expression for $I_D$ leakage to ensure that MVS model produces $I_D=0$ µA/µm at $V_D=0$ V. The selector ‘leak_select’ allows the user to include or exclude the $I_D$ leakage current.

2. Terminal Voltages and Parameters List
Fig. 1 (a) The schematic diagram describes the geometry of the NC-FET. (b) Symbolic representation of the NMOS NC-FET. (c) The NC dielectric is represented as a dependent voltage source \( V_{FE} \) for HSPICE simulation. The NC-FET is represented by two series-connected components, i.e., the NC dielectric and the MOSFET.

![Schematic Diagram](image)

Fig. 2 (a) Ferroelectric acts as an additional gate dielectric capacitor with the conventional MOSFET. (b) All the parasitic components: source resistance \( R_S \), drain resistance \( R_D \), gate-source overlap and fringing capacitance \( C_{OV} \) and gate-drain overlap and fringing capacitance \( C_{OV} \) are included in the analysis.

### 2.1. Terminal Voltages

The NC-FET has two components: (i) NC dielectric and (ii) the conventional MOSFET.

(i) **NC dielectric:** The NC dielectric is treated as an external capacitor connected in series to the gate of the conventional MOSFET. For the DC analysis, the inclusion of a capacitor in the gate terminal as an external element cannot provide meaningful results. Therefore, in HSPICE simulation, NC dielectric element is represented as a dependent voltage source which is a function of gate charge. The inclusion of the NC dielectric as a voltage source enables circuit simulation. *Using the same concept multiple layers of NC dielectric as dielectric stack can be considered in the model.*

(ii) **Conventional MOSFET:** The second element is a conventional MOSFET transistor with drain, gate, source, and body terminals. This model and method work for any structure (planar, double gate, FinFET, SOI FET, GAA-FET, etc) and model (MVS/BSIM4/BSIM-CMG/etc) of the MOSFET so long it is supported by the circuit simulator.

In addition to the standard elements, we introduce a *dummy node* to facilitate exchange of information between the NC dielectric and the conventional MOSFET. In other words, the NC dielectric is now represented by 3 terminals and the MOSFET by 5 terminals. The dummy node (as a voltage terminal) exchanges information regarding the gate charge between the two elements. HSPICE solves the circuit of the NC-FET self-consistently to compute the unknown variables (voltages, currents, etc). The introduction of the dummy node for the MOSFET requires access to the source code. *The modified source codes of BSIM4 and MVS are provided along with the source code of NC dielectric.*
The nodes and corresponding node voltages of the NC dielectric and conventional MOSFET are defined as follows:

**NC dielectric:**

<table>
<thead>
<tr>
<th>Node</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>ncp</td>
<td>Electrode with positive bias</td>
<td>V(ncp)</td>
</tr>
<tr>
<td>ncn</td>
<td>Electrode with negative (or zero bias)</td>
<td>V(ncn)</td>
</tr>
<tr>
<td>qg_as_v</td>
<td>Dummy node to input the gate charge</td>
<td>V(qg_as_v)</td>
</tr>
</tbody>
</table>

**Conventional MOSFET (MVS/BSIM/etc):**

<table>
<thead>
<tr>
<th>Node</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>drain</td>
<td>Drain voltage</td>
<td>V(drain)</td>
</tr>
<tr>
<td>gate</td>
<td>Gate voltage</td>
<td>V(gate)</td>
</tr>
<tr>
<td>source</td>
<td>Source voltage</td>
<td>V(source)</td>
</tr>
<tr>
<td>bulk</td>
<td>Bulk voltage</td>
<td>V(bulk)</td>
</tr>
<tr>
<td>qg_as_v</td>
<td>Dummy node to output the gate charge</td>
<td>V(qg_as_v)</td>
</tr>
</tbody>
</table>

### 2.2. Parameters List

Parameters used in the negative capacitance FET model are listed below. Table also lists the physical meaning of each parameter.

<table>
<thead>
<tr>
<th>Math Symbol</th>
<th>Verilog-A Symbol</th>
<th>Description</th>
<th>Default</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha_{FE}$</td>
<td>alpha</td>
<td>Alpha coefficient of the ferroelectric</td>
<td>$-1.8 \times 10^{11}$</td>
<td>cm/$F$</td>
</tr>
<tr>
<td>$\beta_{FE}$</td>
<td>beta</td>
<td>Beta coefficient of the ferroelectric</td>
<td>$5.8 \times 10^{22}$</td>
<td>cm$^5/F/Coul^2$</td>
</tr>
<tr>
<td>$\gamma_{FE}$</td>
<td>gamma</td>
<td>Gamma coefficient of the ferroelectric</td>
<td>0</td>
<td>cm$^9/F/Coul^4$</td>
</tr>
<tr>
<td>$\rho_{FE}$</td>
<td>rho</td>
<td>Rho coefficient of the ferroelectric</td>
<td>9</td>
<td>cm$ - s/F$</td>
</tr>
<tr>
<td>$t_{FE}$</td>
<td>tFE</td>
<td>Thickness of the ferroelectric dielectric</td>
<td>$10 \times 10^{-7}$</td>
<td>cm</td>
</tr>
</tbody>
</table>

For details regarding the physical interpretation of the model parameters, see Ref. [6]–[9].
3. Model System and Equations

We develop the model of the NC-FET [11], [12] by integrating the BSIM4/MVS model [16] of the conventional short channel MOSFET with the Landau theory of negative capacitor [5]. The subthreshold swing of a MOSFET is defined as

$$ S = \frac{dV_{GS}}{d\log_{10}(I_D)} = \left( \frac{dV_{GS}}{d\psi_S} \right) \left( \frac{d\psi_S}{d\log_{10}(I_D)} \right) = m \times p $$

where, $V_{GS}$ is the applied gate bias, for NC-FET it is $V_{G(NC)}$. $I_D$ is the drain current, $\psi_S$ is the surface potential. The body-factor $m$ can be obtained from the voltage divider rule assuming the gate-source and gate-drain overlap capacitances ($C_{OV}$) have negligible effect on gate charge ($Q_g$).

$$ m = \left( \frac{dV_{GS}}{d\psi_S} \right) = \left( 1 + C_S \left( \frac{1}{C_{OX}} + \frac{1}{C_{FE}} \right) \right) $$

Landau model for the negative capacitor: Ferroelectric (FE) material exhibits negative capacitance [5]. The dynamic of FE capacitor can be explained by Landau Khalatnikov (LK) equation

$$ \rho_{FE} \frac{dQ_g}{dt} + \nabla Q_g U = 0 $$

The Gibb’s free energy of a ferroelectric material is represented by a two well energy landscape, as follows,

$$ U = \alpha_{FE} Q_G^2 + \beta_{FE} Q_G^4 + \gamma_{FE} Q_G^6 - \frac{V_{FE}}{\tau_{FE}} Q_G. $$

The potential ($V_{FE}$) - charge ($Q_G$) relation of the ferroelectric material is represented from eq (4) as

$$ V_{FE} = 2\alpha_{FE} t_{FE} Q_G + 4\beta_{FE} t_{FE} Q_G^3 + 6\gamma_{FE} t_{FE} Q_G^5 + \rho_{FE} t_{FE} \frac{dQ_g}{dt} $$

From eq (5) we can write the capacitance ($C_{FE}$) - charge ($Q_G$) relation of the ferroelectric material, in steady-state, as

$$ C_{FE} = \frac{1}{2\alpha_{FE} t_{FE} + 12\beta_{FE} t_{FE} Q_G^2 + 30\gamma_{FE} t_{FE} Q_G^4} $$
In this work, negative capacitance dielectric and conventional MOSFET are represented as two different components. The I-V and C-V of the NC-FET are computed through charge and potential balance in HSPICE. We represented the ferroelectric dielectric as a dependent voltage source which is a function of $Q_G$. To account this dependency we modified the available verilog-A models of MVS/BSIM4.

4. Device Characteristics

We introduced dummy nodes in both NC dielectric and the MOSFET model to exchange information of gate charge ($Q_G$) between them (Fig. 3(a)). We modified the source code of MVS model to take the gate charge out through dummy node and use that charge as input to the negative capacitor (Fig. 3(b)). We illustrated this for MVS model in Fig. 3. We followed similar approach for BSIM4 model. We can use this approach for other MOSFET models such as BSIM-CMG, BSIM-IMG, BSIM-SOI, etc.
Fig. 3 (a) Two elements (MOSFET and negative capacitor) depend on each other through gate charge \((Q_G)\). Dummy voltage nodes connect the MOSFET and negative capacitor self-consistently through \(Q_G\). (b) Verilog-a codes of the MVS model and negative capacitor explain the inclusion dummy nodes.

To illustrate the model of the NC-FET, we simulate the performance of the conventional MOSFET (NCFET with \(t_{FE}=0\) nm) and the behavior of the NC dielectric capacitor in Fig. 4. Then we evaluated the characteristics of the NMOS NC-FET, PMOS NC-FET, NC-FET CMOS inverter in Figs. 5, 6, and 7, respectively. The improved performance of the NC-FET sustains for different gate lengths (Fig. 8). The transient performance of the NC-FET CMOS inverter is evaluated in Fig. 9 (in Appendix).
Fig. 4 (a) C-V characteristics of the conventional MOSFET (using BSIM4). At $V_{GS}=0$ V, gate capacitance is dominated by the gate-source ($C_{OV}$) and gate-drain ($C_{OV}$) overlap and parasitic capacitances. (b) Polarization ($P$) vs applied bias ($V_{FE}$) of the ferroelectric dielectric P(VDF-TrFE). $\alpha_{FE}$ and $\beta_{FE}$ coefficients of the ferroelectric dielectric are extracted through fitting of eq (5) with experiment (from Ref. [10], [17]). We neglect the 5th order term of $Q_G$ and dipole response to extract the coefficients of ferroelectric. (c) Energy landscape for different applied bias ($V_{FE}$) (eq (4)), polarization ($P$) vs applied bias ($V_{FE}$) (eq 5), and polarization ($P$) vs capacitance ($C_{FE}$) (eq 6) of the ferroelectric dielectric.
Fig. 5 (a) $I_D$-$V_{GS}$ and (b) Gate charge ($Q_G$) vs $V_{GS}$ characteristics of the NMOS NC-FET for different $t_{FE}$ using BSIM4 and Landau theory. (c) Different potential components of the NC-FET: applied gate bias ($V_{G(NC)}$), voltage across the ferroelectric dielectric ($V_{FE}$), and voltage in the intermediate node G(MOS), $V_{G(MOS)}$. (d) Subthreshold slope ($S$) vs $V_{GS}$ for different $t_{FE}$. (e) $Q_G$ vs $V_{FE}$ profile from the circuit simulation (red) and from eq (5) (blue).
Fig. 6 (a) Symbolic representation of the PMOS NC-FET. (b) $I_D-V_{GS}$ and (c) Gate charge ($Q_G$) vs $V_{GS}$ characteristics of the PMOS NC-FET for different $t_{FE}$ using BSIM4 and Landau theory. (d) Different potential components of the NC-FET: applied gate bias ($V_{G(NC)}$), voltage across the ferroelectric dielectric ($V_{FE}$), and voltage in the intermediate node G(MOS), $V_{G(MOS)}$. (e) Subthreshold slope ($S$) vs $V_{GS}$ for different $t_{FE}$.

Fig. 7 (a) Symbolic representation of the NC-FET CMOS inverter. (b) Performance comparison of the different CMOS inverters. With the incorporation of NC dielectric, NMOS (black arrow) and PMOS (magenta arrow) are turning-on at lower effective threshold voltage compared to conventional counterpart.
Fig. 8 $I_D$ vs $V_G$ characteristics of the NMOS NC-FET from (a) BSIM4 and Landau theory and (b) MVS and Landau theory for 45 nm technology node. Subthreshold slope ($S$) vs $V_G$ of the NMOS NC-FET from (a) BSIM4 and Landau theory and (b) MVS and Landau theory for 45 nm technology node. We compared the $I_D$-$V_{G(MOS)}$ of the conventional MVS and BSIM4 MOSFET models. Unlike MVS, the $I_D$ in BSIM4 model saturates with $V_{G(MOS)}$ beyond off-states while moving toward the accumulation region. Saturation in $I_D$-$V_{G(MOS)}$ results U-shaped $S$ vs $V_{G(MOS)}$, whereas conventional MVS model provides mirrored L-shape. To improve the matching of the simulated results of the two models, we added a leakage current component ($I_D(@V_{G(MOS)}=0)$) to $I_D$-$V_{G(MOS)}$ in the source code of MVS model. In version 1.0.0 of the NCFET model, this leakage current component was independent of $V_D$. We corrected this in the revised version 1.1.0 by multiplying the leakage current with $(V_D/V_{DSAT})/(1+ (V_D/V_{DSAT})^\beta)^{1/\beta}$. $V_{DSAT}$ is the saturation drain bias and $\beta$ is the saturation-transition-region fitting parameter [16], [18]. In version 1.1.0, $I_D=0$ at $V_{G(MOS)}=V_D=0$. In addition, in version 1.1.0, we added a selector ‘leak_select’ to include and exclude the $I_D(@V_{G(MOS)}=0)$. leak_select=1 includes $I_D(@V_{G(MOS)}=0)$.

5. Summary

The manual describes the electrical model of the NC-FET by integrating MVS/BSIM4 model with Landau theory. Please contact Dr. Muhammad A. Wahab (mwahab@purdue.edu) and Professor Alam (alam@purdue.edu) regarding any questions/comments about the negative capacitance FET compact model.
References


[16] S. Rakheja and D. Antoniadis, “MVS Nanotransistor Model (Silicon).” NEEDS nanoHUB.


A. Transient performance

Our developed NC-FET model can be used for transient simulation of CMOS circuits. Results of the transient simulation of the NC-FET CMOS inverter of Fig. 7(a). Ferroelectric material HfSiO ($\alpha_{FE} = -8.7 \times 10^{10}$ cm/F, $\beta_{FE} = 1.92 \times 10^{20}$ cm$^5$/F/Cout$^2$, $\gamma_{FE} = 0$ cm$^9$/F/Cout$^4$, and $t_{FE} = 15 \times 10^{-7}$ cm) is used as NC dielectric in the gate dielectric stack [9], [19].

- (a) with MOSFET
- (b) with NC-FET ($\rho_{FE}=0$ cm-s/F)
- (c) with NC-FET ($\rho_{FE}=9$ cm-s/F)

Fig. 9 Our developed NC-FET model can be used for transient simulation of CMOS circuits. Results of the transient simulation of the NC-FET CMOS inverter of Fig. 7(a). Ferroelectric material HfSiO ($\alpha_{FE} = -8.7 \times 10^{10}$ cm/F, $\beta_{FE} = 1.92 \times 10^{20}$ cm$^5$/F/Cout$^2$, $\gamma_{FE} = 0$ cm$^9$/F/Cout$^4$, and $t_{FE} = 15 \times 10^{-7}$ cm) is used as NC dielectric in the gate dielectric stack [9], [19]. (a) Input gate pulse ($V_{in}$) and output ($V_{out}$) vs time ($t$) of the conventional MOSFET CMOS Inverter. (b) $V_{in}$ and $V_{out}$ vs $t$ of the NC-FET CMOS Inverter neglecting dipole response of the ferroelectric ($\rho_{FE} = 0$ cm $-s$/F). (c) $V_{in}$ and $V_{out}$ vs $t$ of the NC-FET CMOS Inverter accounting dipole response of the ferroelectric ($\rho_{FE} = 9$ cm $-s$/F). Dipole response slows down the performance of the NC-FET and their circuits. The value of $\rho_{FE} = 9$ cm $-s$/F is assumed in this work and not necessarily the parameter of HfSiO.
B. Parameters of Conventional MOSFET

Conventional MOSFET parameters are directly collected or extracted from the predictive technology model (http://ptm.asu.edu/). A sample set of parameters for NMOS device is provided below as an illustration.

<table>
<thead>
<tr>
<th>Math Symbol</th>
<th>Description</th>
<th>( L_G = 45 \text{ nm} ) (Default value)</th>
<th>( L_G = 32 \text{ nm} ) (Default value)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W )</td>
<td>Channel width</td>
<td>1</td>
<td>1</td>
<td>( \mu m )</td>
</tr>
<tr>
<td>( EOT )</td>
<td>Effective oxide thickness</td>
<td>0.9</td>
<td>0.75</td>
<td>( nm )</td>
</tr>
<tr>
<td>( \varepsilon_{OX} )</td>
<td>Oxide dielectric constant</td>
<td>3.9</td>
<td>3.9</td>
<td></td>
</tr>
<tr>
<td>( \varepsilon_0 )</td>
<td>Free space permittivity</td>
<td>( 8.854 \times 10^{-14} )</td>
<td>( 8.854 \times 10^{-14} )</td>
<td>( F/cm )</td>
</tr>
<tr>
<td>( N_{Sub} )</td>
<td>Substrate doping density</td>
<td>( 6.5 \times 10^{18} )</td>
<td>( 8.7 \times 10^{18} )</td>
<td>( cm^{-3} )</td>
</tr>
<tr>
<td>( V_{T0} )</td>
<td>Threshold voltage</td>
<td>0.3423</td>
<td>0.3558</td>
<td>( V )</td>
</tr>
<tr>
<td>( \mu )</td>
<td>Carrier mobility</td>
<td>295</td>
<td>238</td>
<td>( cm^2/VS )</td>
</tr>
<tr>
<td>( v_{x0} )</td>
<td>Saturation velocity</td>
<td>( 1.595 \times 10^7 )</td>
<td>( 1.821 \times 10^7 )</td>
<td>( cm/S )</td>
</tr>
<tr>
<td>( R_S = R_D )</td>
<td>Source/Drain resistance</td>
<td>52.5</td>
<td>40</td>
<td>( \Omega - \mu m )</td>
</tr>
<tr>
<td>( C_{GSOV} = C_{GD0V} )</td>
<td>Source/Drain overlap capacitance</td>
<td>( 2.1 \times 10^{12} )</td>
<td>( 2 \times 10^{12} )</td>
<td>( F/cm )</td>
</tr>
<tr>
<td>( n )</td>
<td>Subthreshold coefficient</td>
<td>1.15</td>
<td>1.15</td>
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<tr>
<td>( \delta )</td>
<td>DIBL factor</td>
<td>0.0332</td>
<td>0.0424</td>
<td>( V/V )</td>
</tr>
<tr>
<td>( \beta )</td>
<td>Saturation-transition-region fitting parameter</td>
<td>1.8</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>( \alpha )</td>
<td>Body factor</td>
<td>3.5</td>
<td>3.5</td>
<td></td>
</tr>
<tr>
<td>( \gamma )</td>
<td>Body factor</td>
<td>0.1</td>
<td>0.1</td>
<td>( \sqrt{V} )</td>
</tr>
</tbody>
</table>

C. HSPICE toolkit

In order to analyze the HSPICE output data, HSPICE toolkit available in Matlab is used. This can be downloaded from http://www.cppsim.com/InstallFiles/hspice_toolbox.tar.gz. Make sure to add it in the Matlab path. You can use the following Matlab command to add this to the default path: `addpath(location_of_hspice_toolbox_folder)`.

D. Simulating HSPICE netlist

HSPICE code can be run on file “filename.sp” using following command: `hspice filename.sp`

E. Checklist for model analysis

1. Install the HSPICE toolkit to enable data extraction from HSPICE files.

2. Download the complete package in folder NCFET. Compile the following HSPICE files

   NCFET\Negative Capacitance FET Model 1.1.0 HSPICE
   Netlists\ncfet_nmos_bsim4_Lg32nm\ncfet_nmos.sp

   NCFET\Negative Capacitance FET Model 1.1.0 HSPICE
   Netlists\ncfet_pmos_bsim4_Lg32nm\ncfet_pmos.sp
3. Compilation of the files will generate the filename.sw0 and filename.tr0 files for dc and transient simulations respectively. These files can be analyzed using the perform_analysis.m file.

4. Go to the folder containing the “perform_analysis.m” file and run it.

Usage Notes and Known Issues

1. The MVS model produces identically zero drain current at zero voltage when simulated by HSpice and Spectre. When the Negative capacitor is included, the combined model still produces the zero drain-current at zero voltage in Spectre, but the current is small (but non-zero) for Hspice simulation, see Fig. 10(a). Apparently, this is a numerical issue, but none of the results will be substantially affected by the numerical issue.

2. We find the BSIM4 model produces a small but non-zero current even as a standalone model, see Fig. 10(b). The effect propagates into the NC-FET. Again, the current is too small to affect any result in any meaningful way.
Fig. 10 (a) $I_D$ vs $V_{GS}$ characteristics of the NMOS NC-FET from MVS and Landau theory at $V_D=0$ V. (b) $I_D$ vs $V_{GS}$ characteristics of the NMOS MOSFET from BSIM4 at $V_D=0$ V.