NCN Nanotechnology 101 Series

Moore's Law Forever?

Mark Lundstrom
Purdue University
Network for Computational Nanotechnology
West Lafayette, IN USA

1) Background
2) Transistors
3) CMOS
4) Beyond CMOS

NCN

www.nanohub.org

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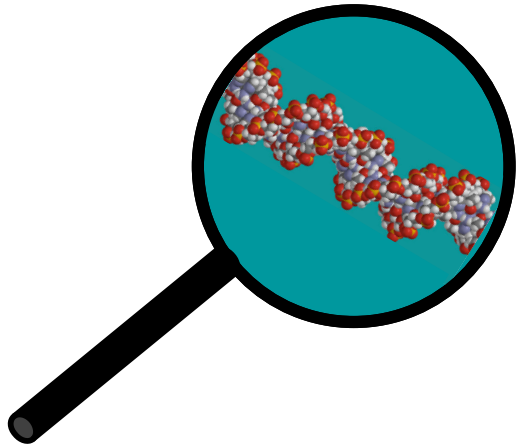
1. The scale of things

1 meter
(1 billion nm)

1 millimeter
(1 million nm)

1 micrometer
(1 thousand nm)

1 nanometer



people

things

ants

dust

cells

molecules

(e.g. DNA)

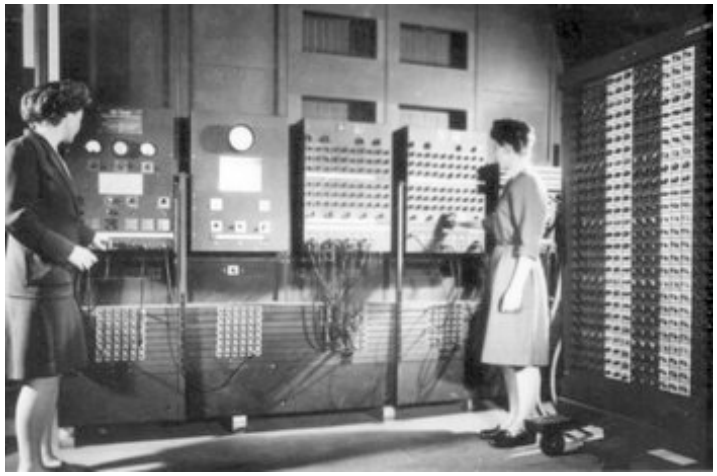
1. Vacuum tube electronics

Vacuum Tube

Edison effect (Edison, 1883)
cathode rays (Thompson, 1897)
diode (Fleming, ~1900)
triode (De Forest, 1906)

ENIAC

(1945, Mauchly and Echkert, U Penn)

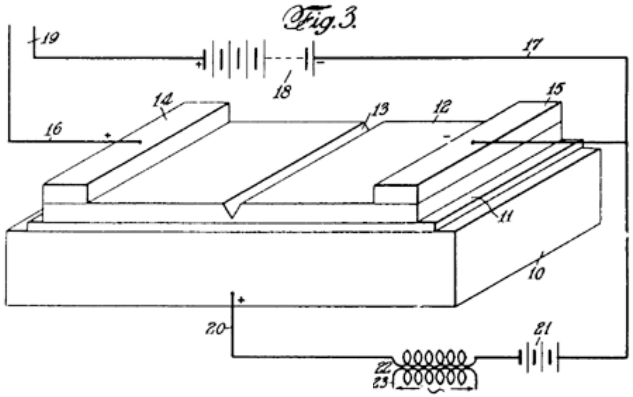


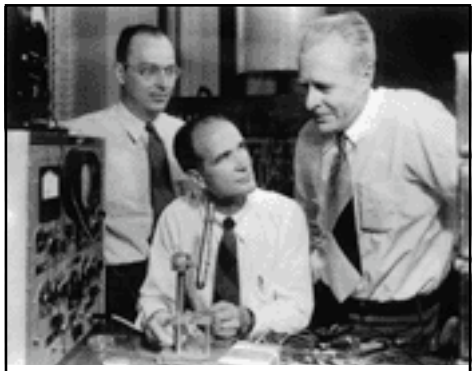
http://en.wikipedia.org

18,000 vacuum tubes
1000 sq. feet of floor space
30 tons
150 KW
~50 vacuum tubes / day

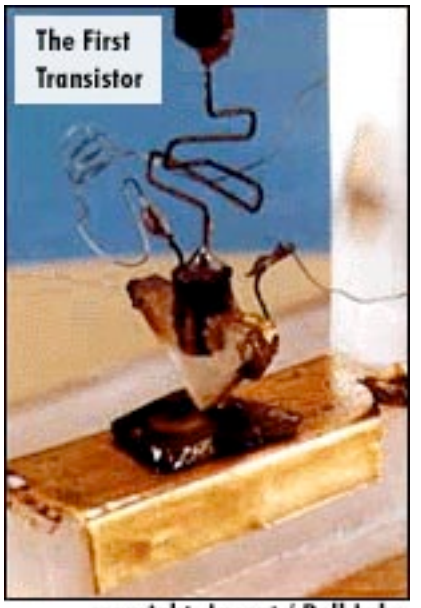
1. Transistors

Field-Effect Transistor
Lillienfield, 1925
Heil, 1935





Bardeen, Schockley, and Brattain, 1947



copyright: Lucent / Bell Labs

"The transistor was probably the most important invention of the 20th century,"

Ira Flatow, Transistorized!
www.pbs.org/transistor

1. Transistors

transistors

Sony TR-63
6-transistor
shirt pocket radio
1957

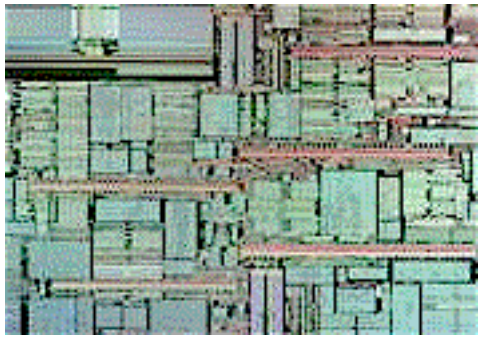
http://www.etedeschi.ndirect.co.uk/early.sony.htm

1. Integrated circuits

integrated circuit

Kilby and Noyce (1958, 1959)

Intel 4004



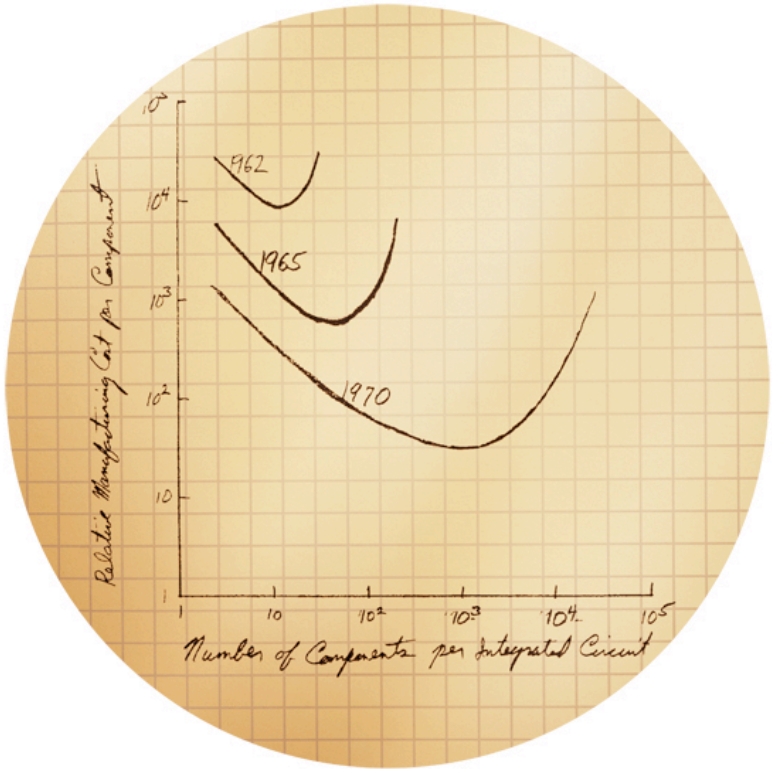
Hoff and Faggin (1971)

~2200 transistors

1. Moore's Law

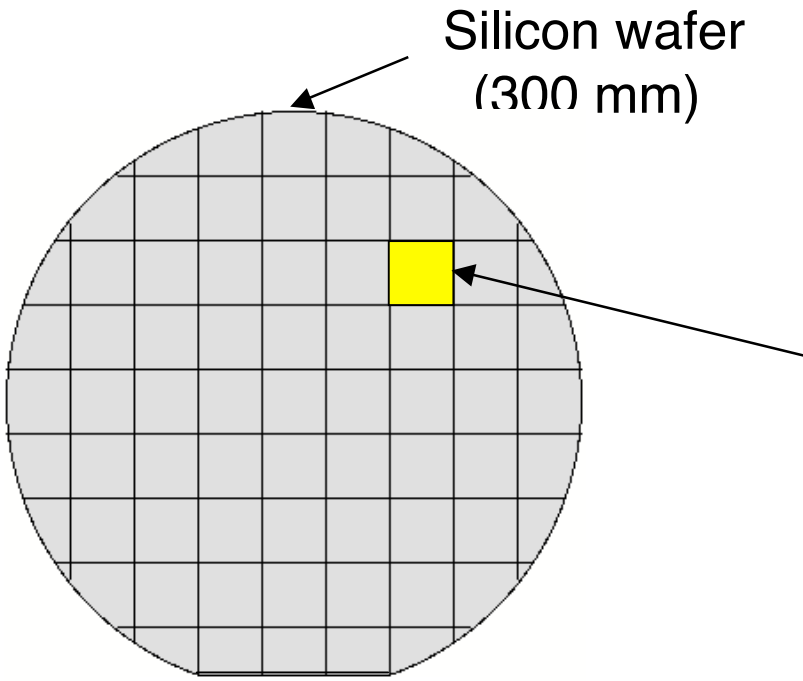
Gordon E. Moore
Co-founder, Intel Corporation

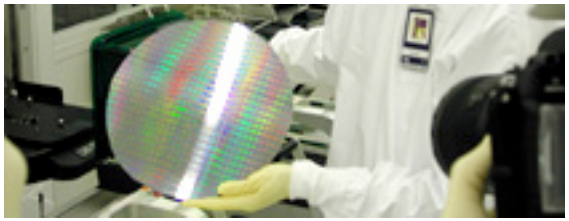
1965



In 1965, Gordon Moore sketched out his prediction of the pace of silicon technology. Decades later, Moore's Law remains true,driven largely by Intel's unparalleled silicon expertise.

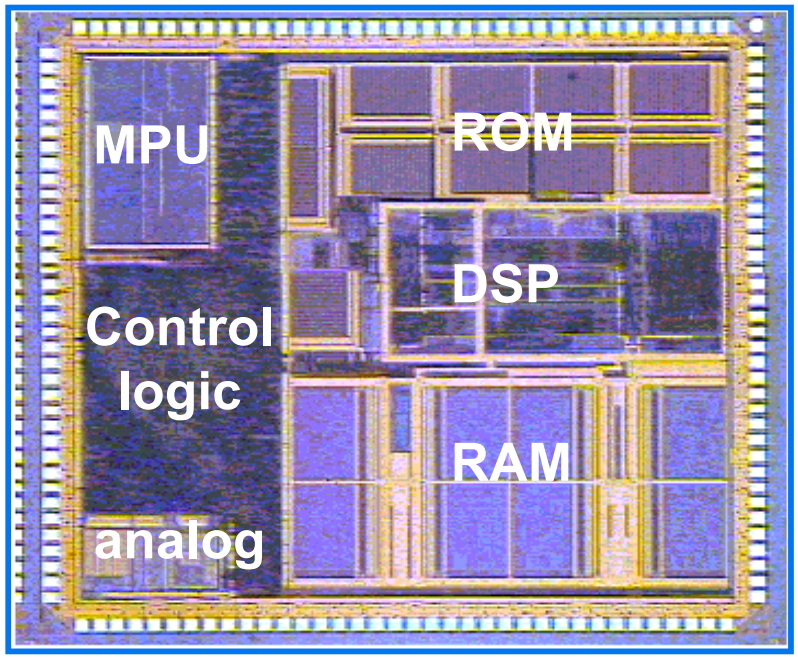
1. Microelectronics





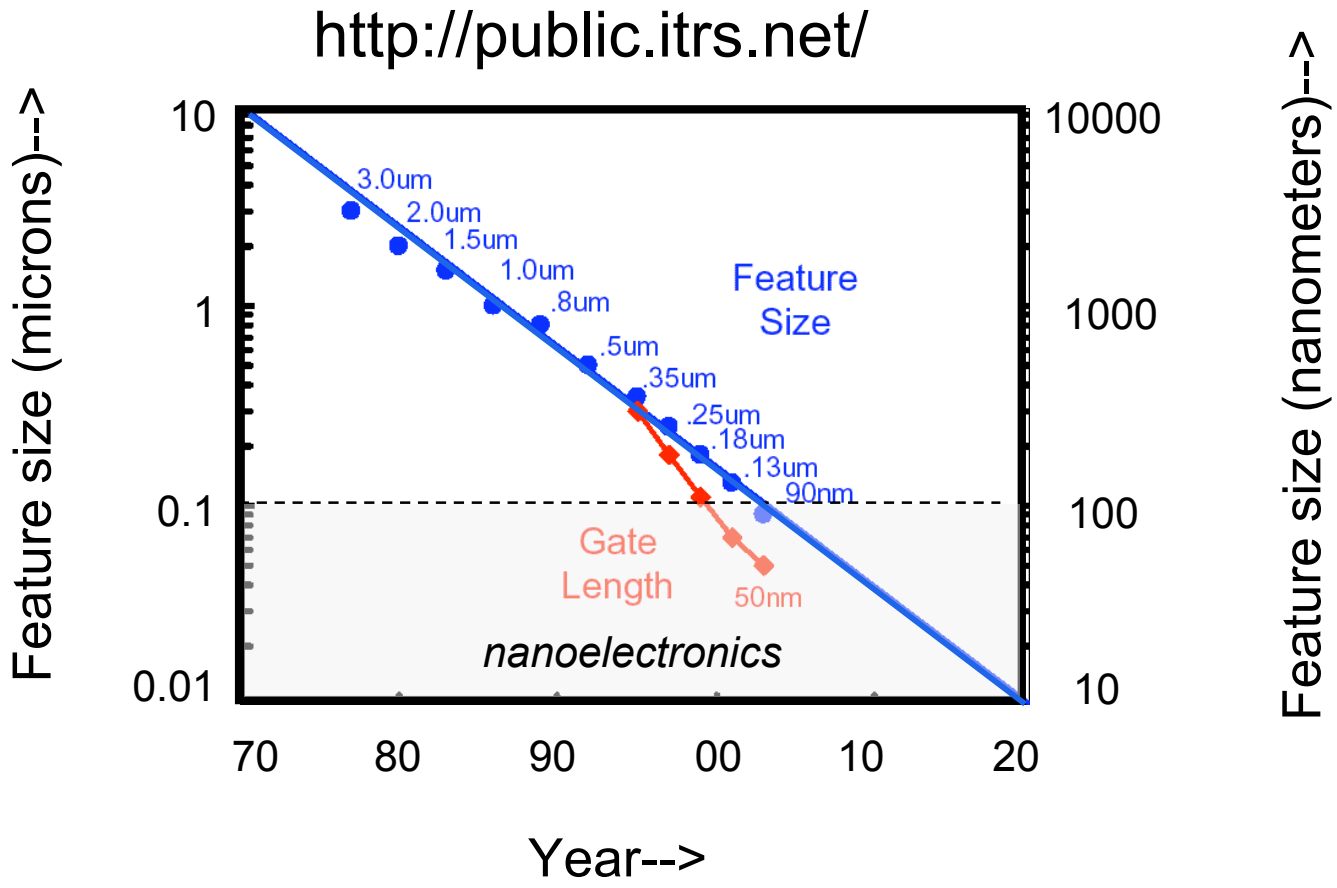
Intel

Silicon “chip”
(~ 2 cm x 2 cm)



TI cell phone chip

1. The ITRS



By 2003, the number of transistors manufactured per year (10^{18}), was 100 times greater than the estimated number of ants in the world.

1. Nanoelectronics

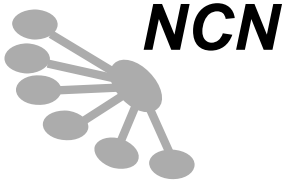
Working at the length scale of 1-100 nm in order to create materials, devices, and systems ***with fundamentally new*** *properties and functions because of their nanoscale size.*

paraphrased from www.nano.gov

1. Exponential Growth

1	90 nm	1B/chip
2		2B
3		4B
4		8B
5		16B
6		32B
7		64B
8		128B
10		256B
11		512B
12		**1T**

1) Background
2) Transistors
3) CMOS
4) Beyond CMOS?



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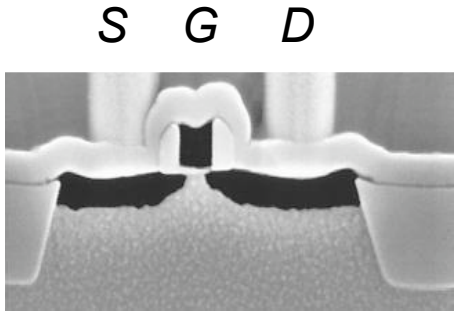
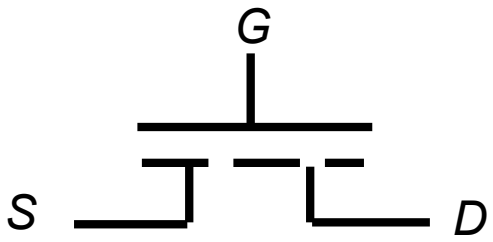
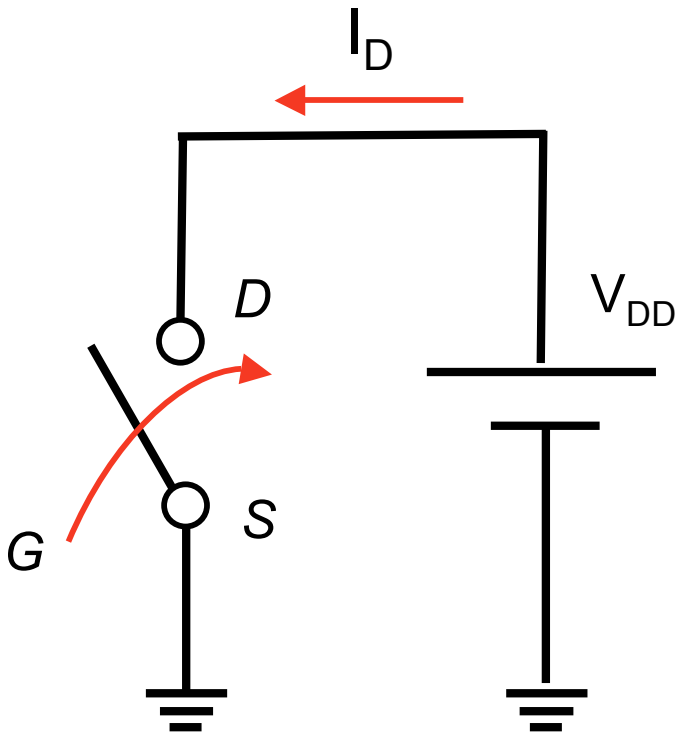
2. MOSFETs



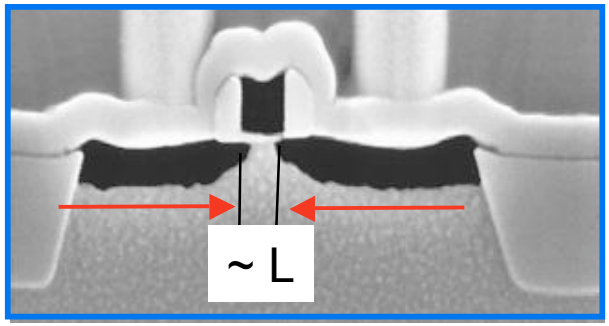




$V_G > V_T$: I_D ---> ∞ "on-current"

$V_G < V_T$: $I_D = 0$ "off-current"

2. Transistor Scaling



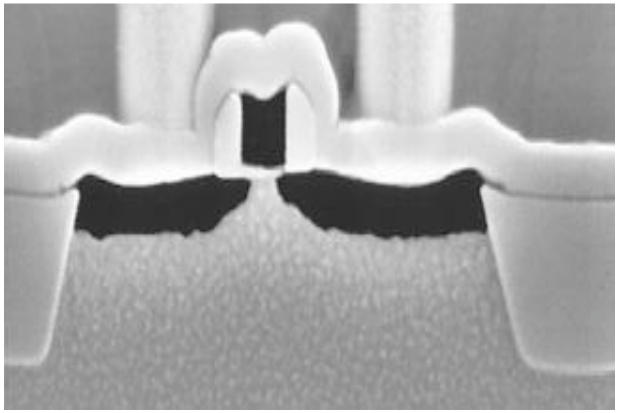
Each technology generation: **(device scaling)**

$$L \rightarrow L/\sqrt{2} \qquad A \rightarrow A/2$$

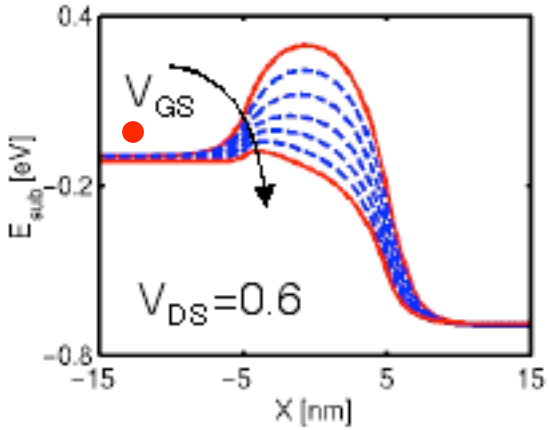
Number of transistors per chip doubles **(Moore's Law)**

2. Transistor Physics

S *G* *D*



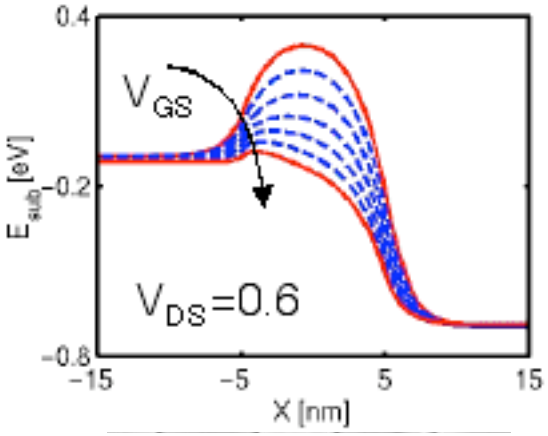
electron energy vs. position



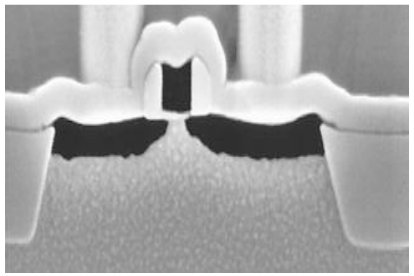
energy = -q x voltage

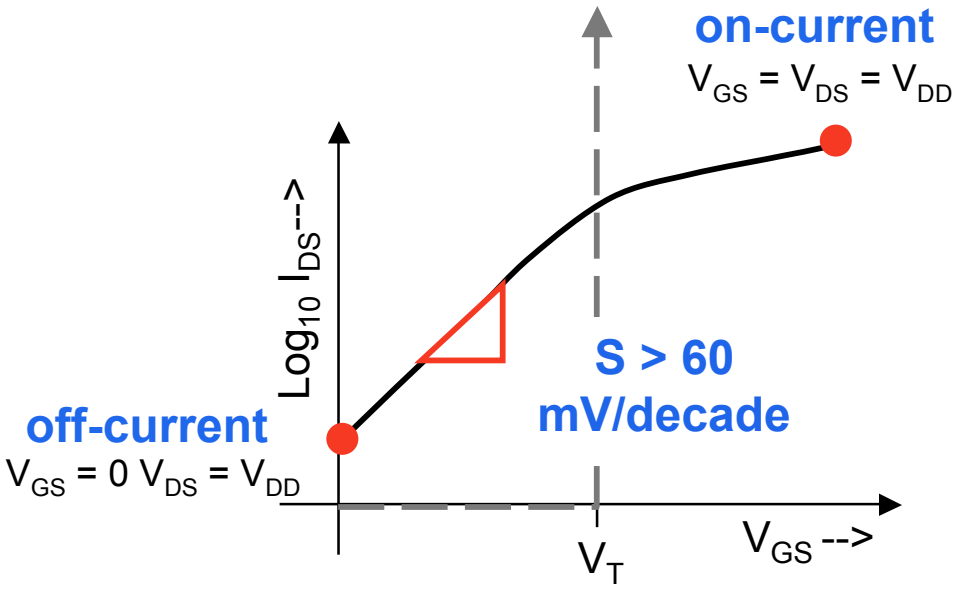
2. Real MOSFETs

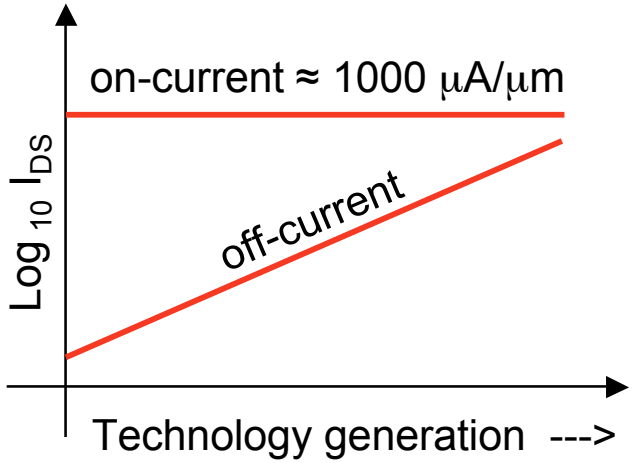
electron energy vs. position



S G D







2. Device challenges

1) low voltage operation (power = voltage x current)
2) high on-current (speed)
3) low off-current (standby power)
4) series resistance
5) device variability

2. Transistors

for a tutorial on transistors, see:

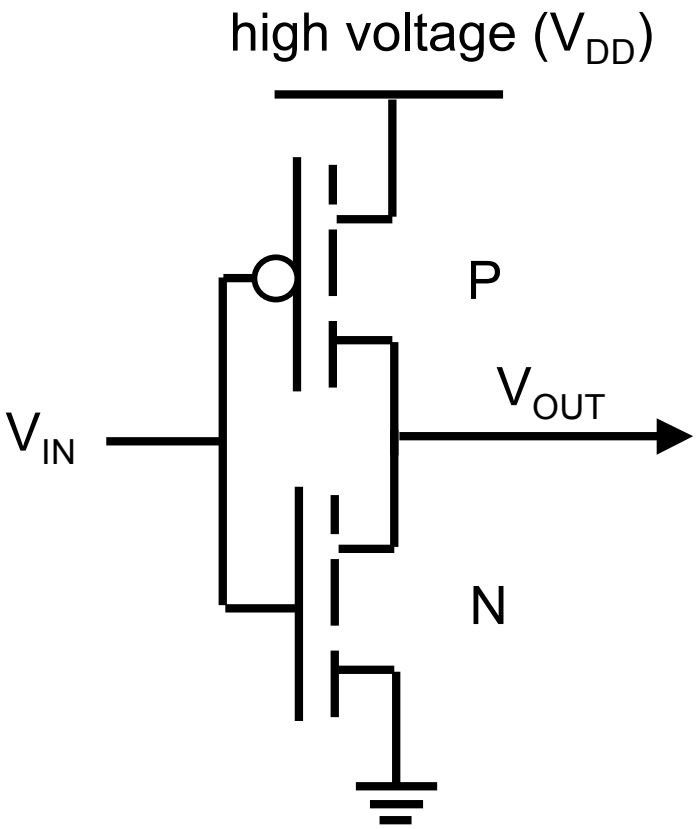
"Transistors 101"

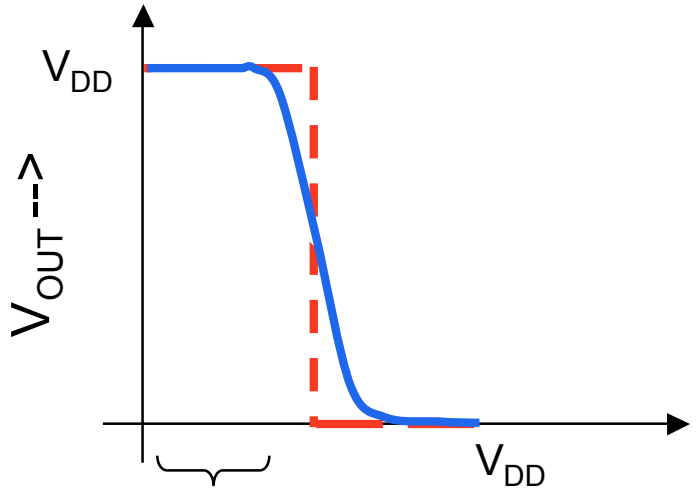
under "Nanotechnology 101"

at www.nanohub.org

1) Background
2) Transistors
3) CMOS
4) Beyond CMOS?

3. CMOS inverter

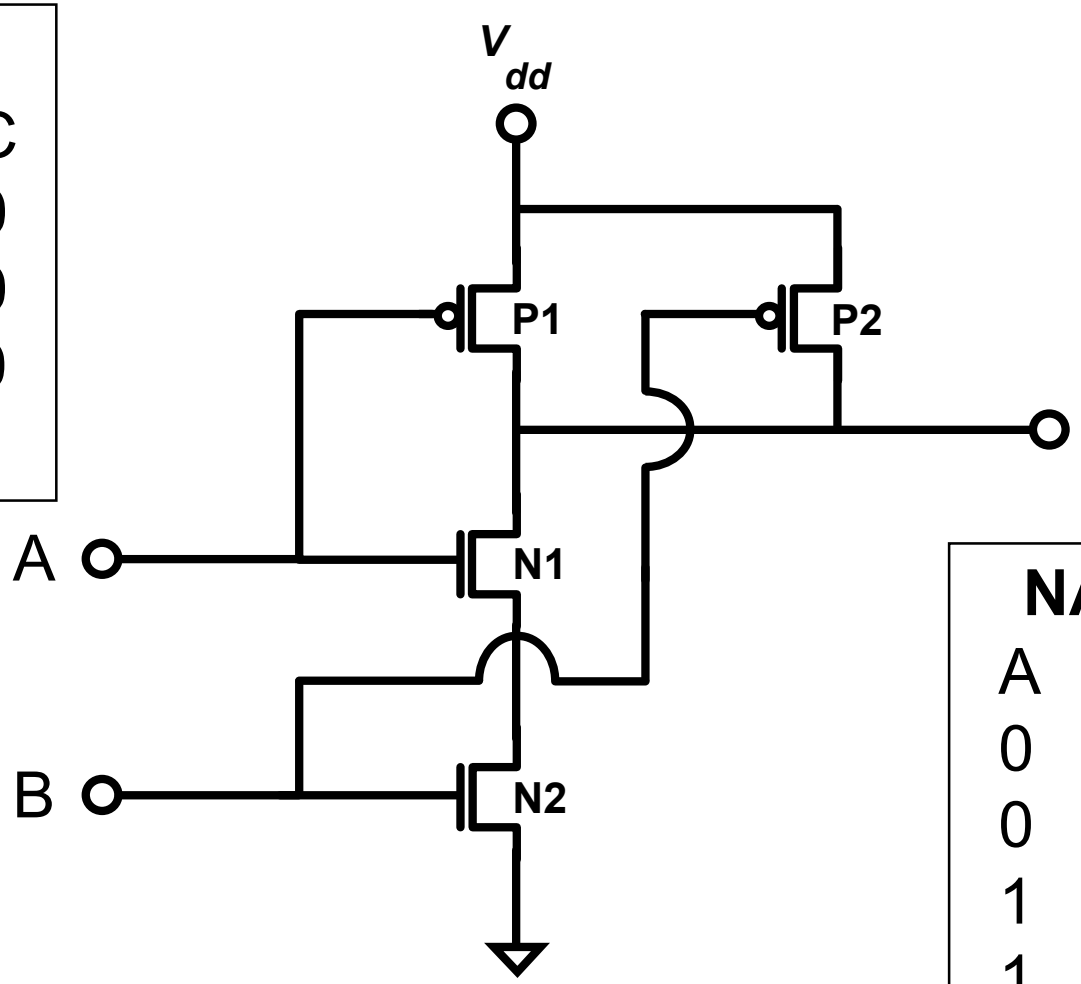




noise margin!

3. Two input NAND gate

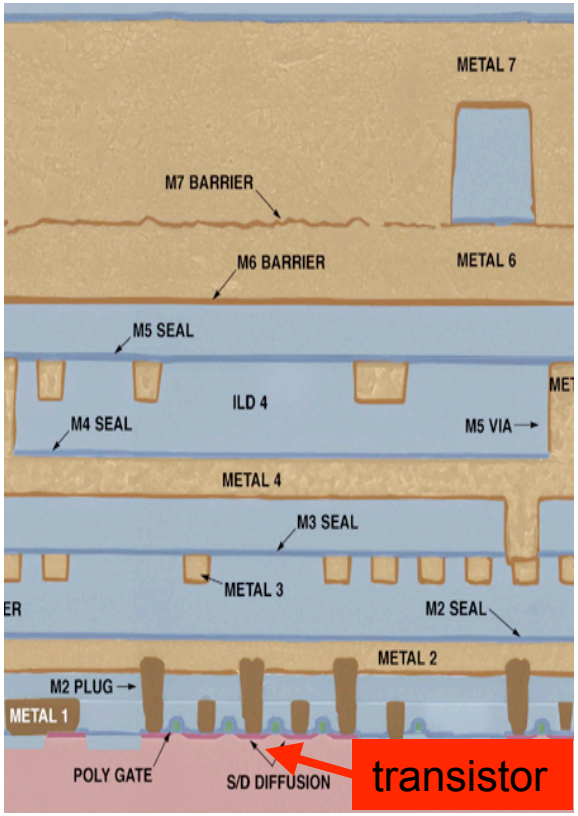
AND		
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



NAND		
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

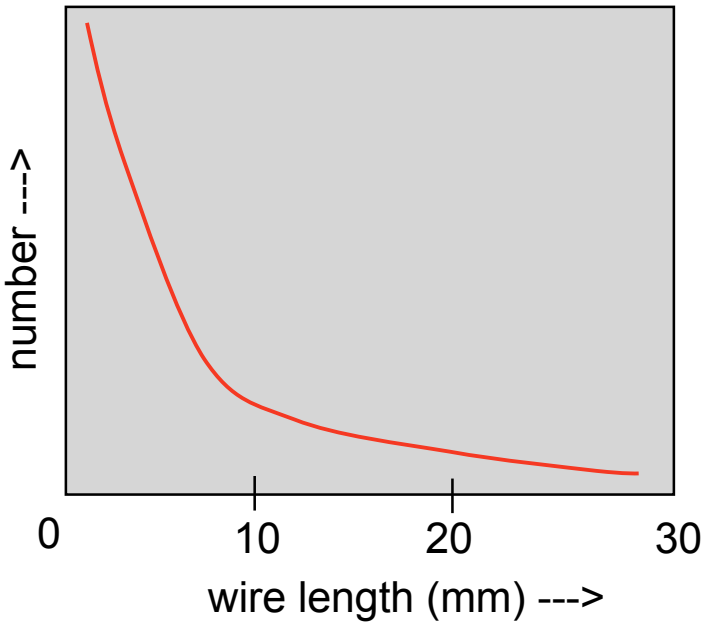
2. Wires

Metal 7
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1



Silicon wafer

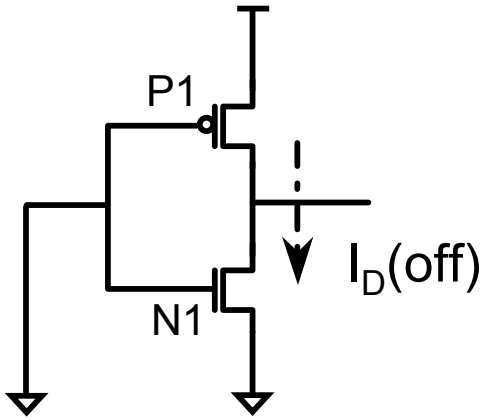
Rent's Rule



$$\tau_{global} \approx r_{\text{int}} c_{\text{int}} \sim \ell^2 \approx 100 \text{ ps}$$

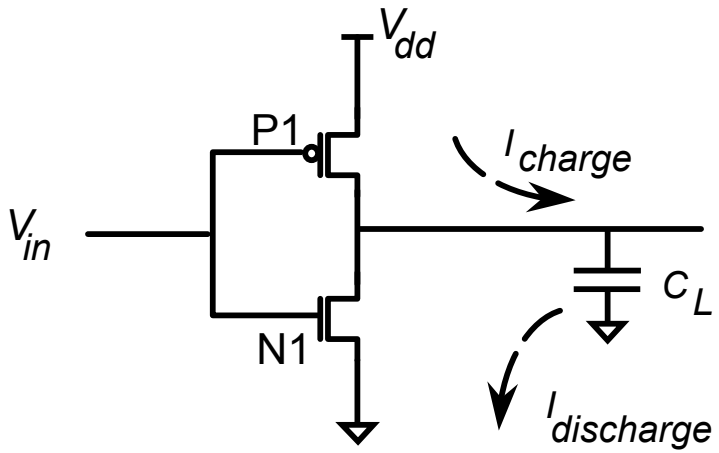
(90 nm technology node)

2. Power



1) standby power:

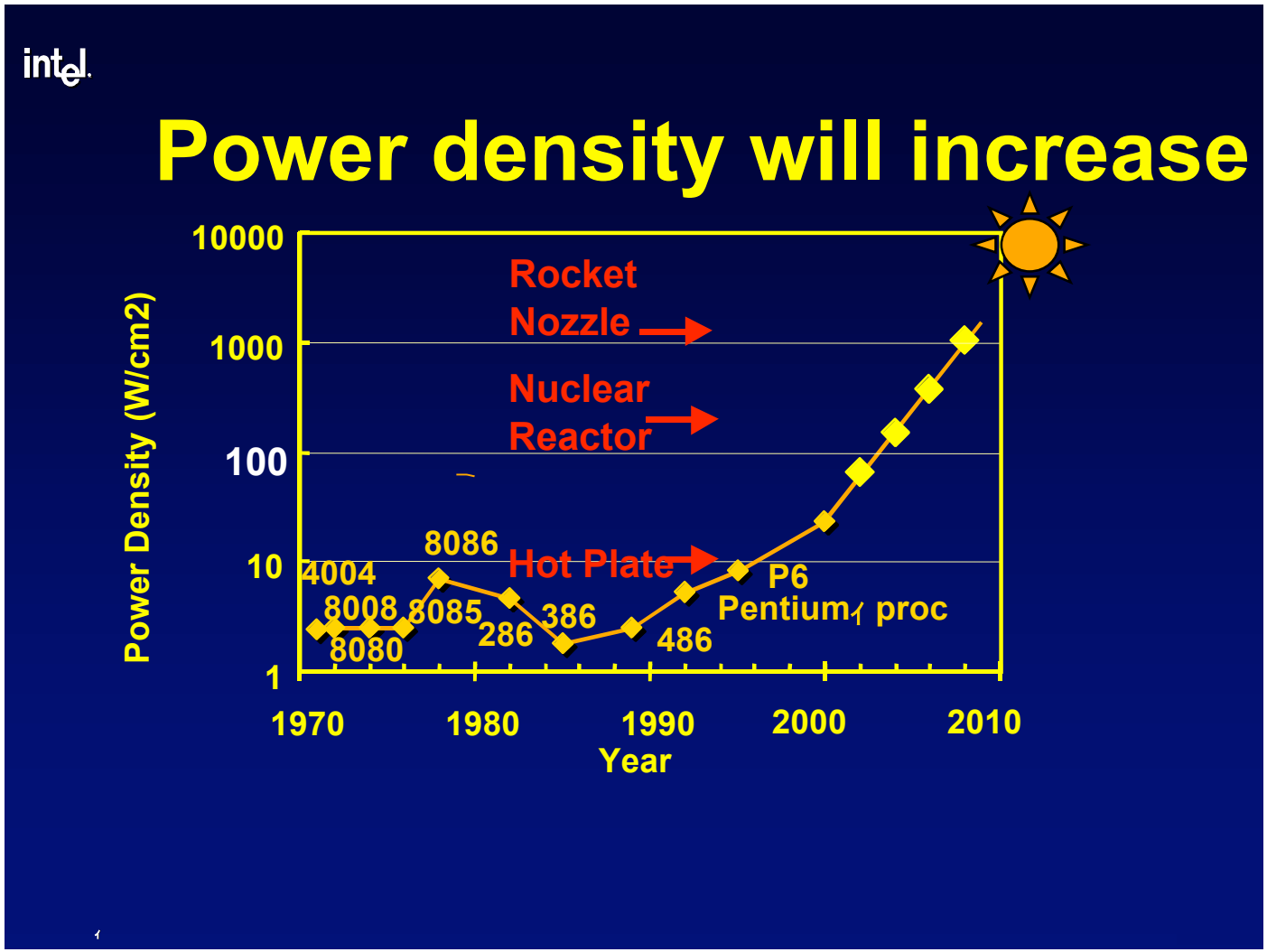
$$P_{off} = N_G I_D(off) V_{DD}$$



2) dynamic power:

$$P_{on} \approx f C_{TOT} V_{DD}^2$$

2. The power crises



2. Design challenges

1) power
2) interconnects
3) device variability
4) reliability
5) complexity

3. CMOS Technology

for a tutorial on CMOS, see:

"CMOS Nanotechnology 101"

under "Nanotechnology 101"

at www.nanohub.org

1) Background
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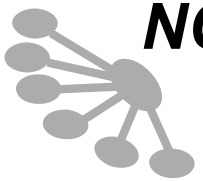
4) Beyond CMOS?



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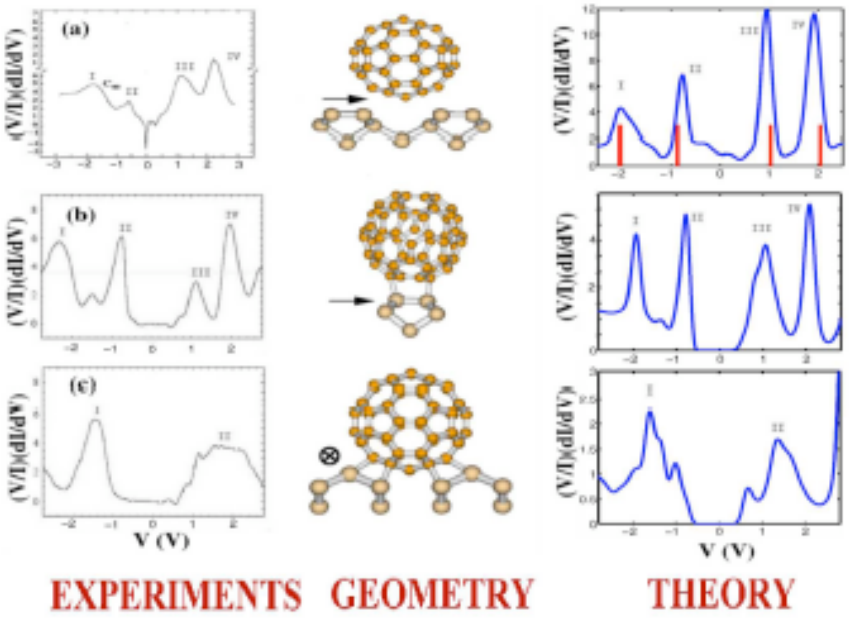
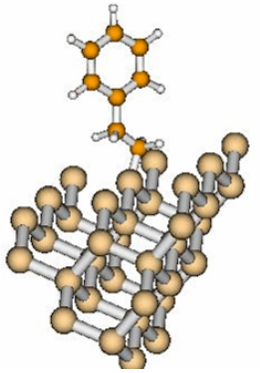
4. Molecular electronics?

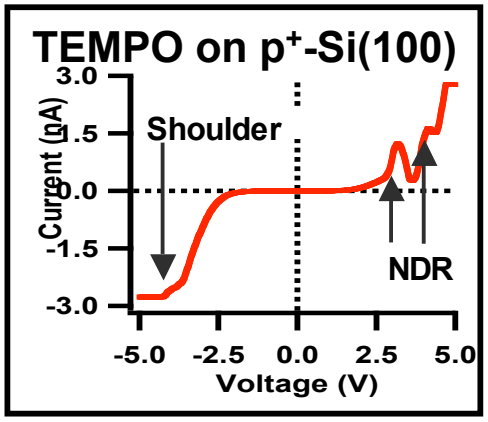
C_{60} on Si(100) 2x1



(Liang and Ghosh)

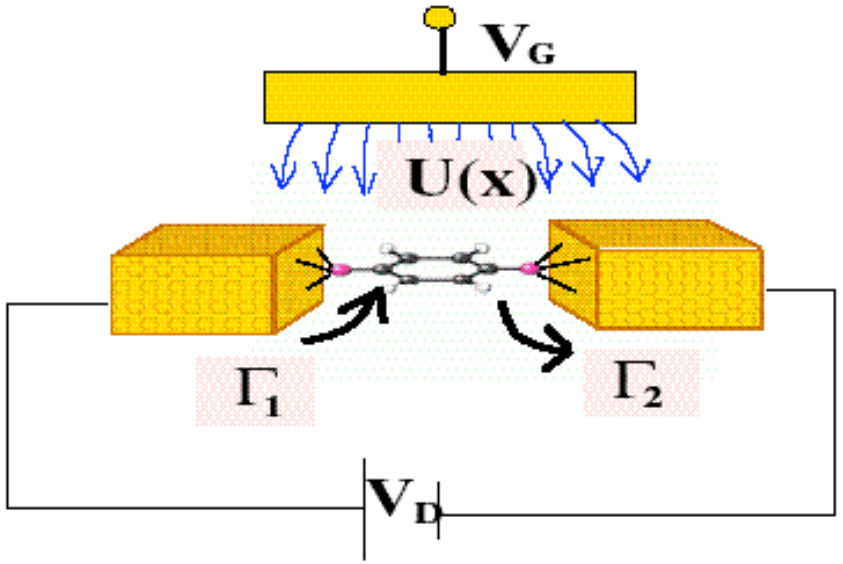
STM

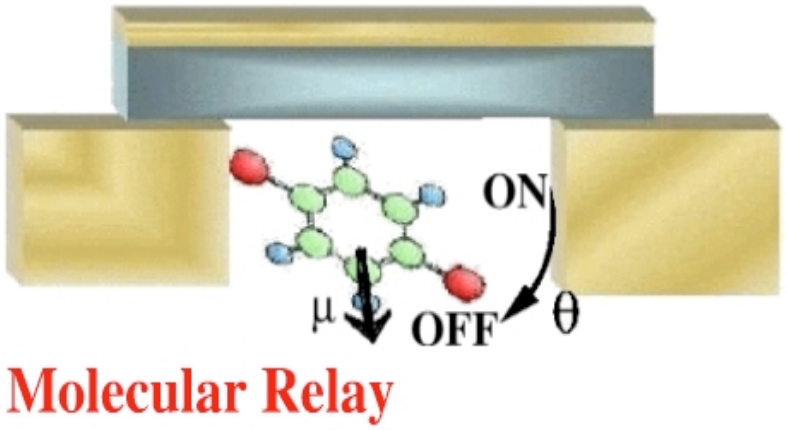




Hersam, Datta, Purdue

4. Molecular transistors?

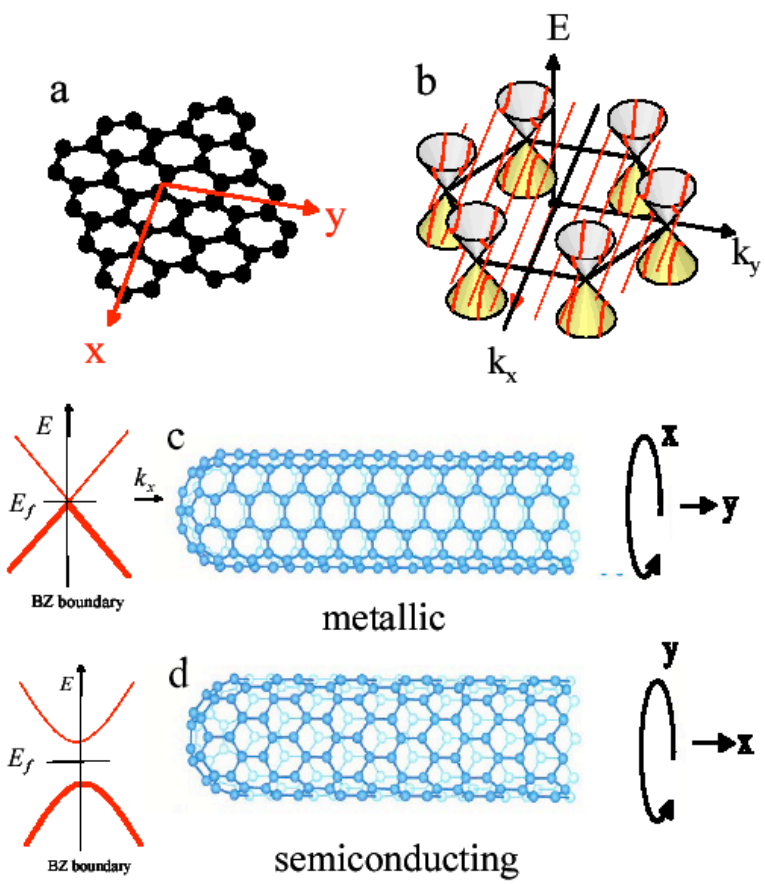




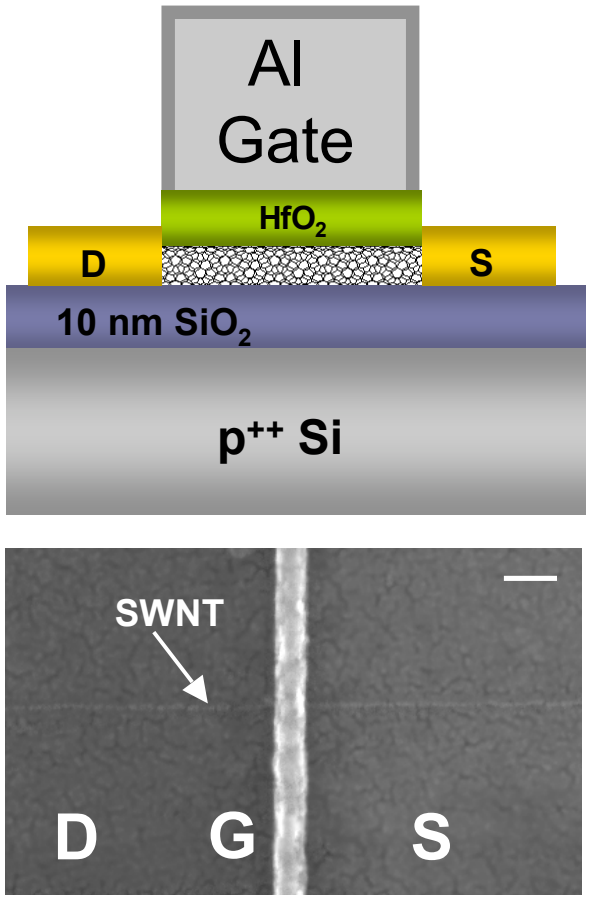
S. Datta, A. Ghosh, P. Damle, T. Rakshit

Ghosh, Rakshit, Datta,
Nanoletters **4**, 565, 2004

4. Carbon nanotube transistors?

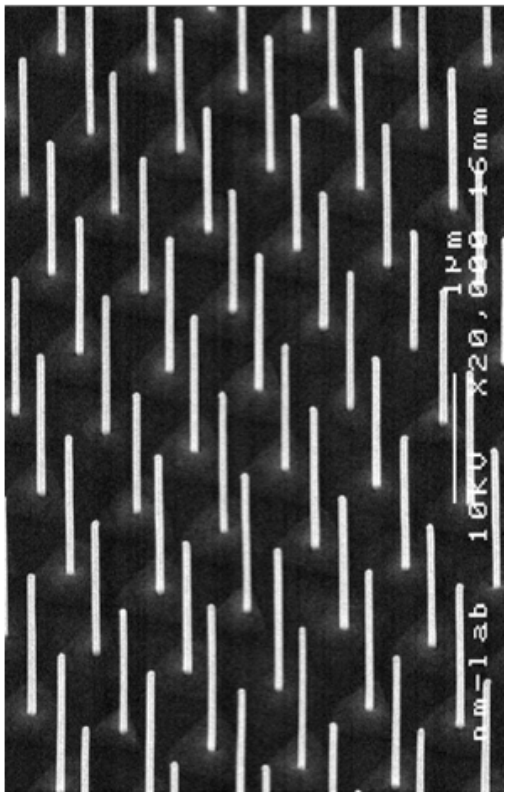


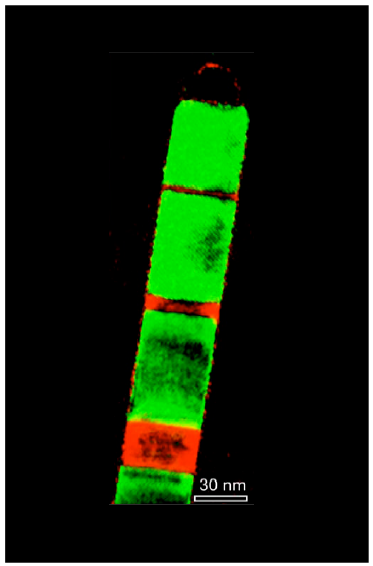
McEuen et al., *IEEE Trans. Nanotech.*, **1** , 78, 2002.



Hongjie Dai group, Stanford

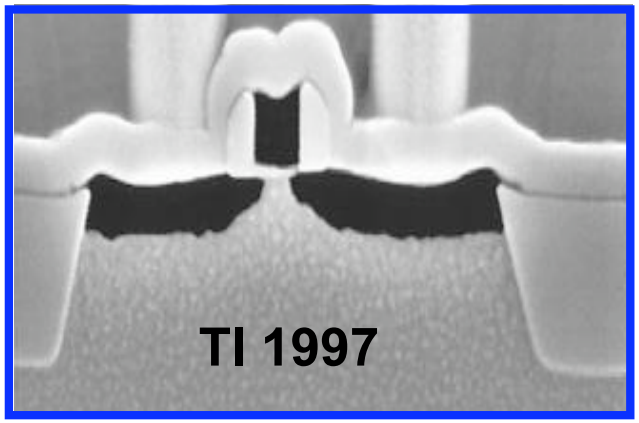
4. Nanowire transistors?

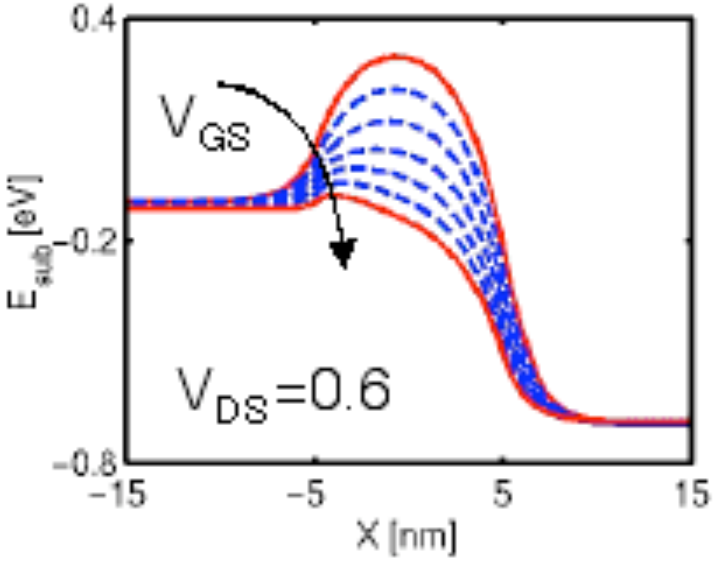




Samuelson Group
Lund

4. Limits of transistors





Limits

$$E_S\big|_{\min} = \ln(2)\, k_B T$$

$$L_{\min} \approx \hbar \Big/ \sqrt{2m\, E_S\big|_{\min}}$$

$$\tau_{\min} \approx \hbar \Big/ E_S\big|_{\min}$$

$$\left(\Delta p \Delta x = \hbar\right)$$

$$\left(\Delta E\, \Delta t = \hbar\right)$$

Zhirnov, et al., *Proc. IEEE*, Nov. 2004

4. Transistors and limits

90 nm node
(ITRS 2004 ed.)

$$E_S \approx 35{,}000 \times E_S\big|_{\min}$$

$$L \approx 25 \times L_{\min}$$

$$\tau \approx 24 \times \tau_{\min}$$

$$n = 0.2 \text{ B/cm}^2$$

18 nm node
(ITRS 2004 ed.)

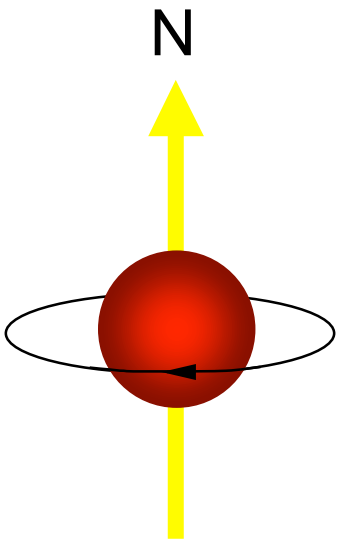
$$E_S \approx 4200 \times E_S\big|_{\min}$$

$$L \approx 5 \times L_{\min}$$

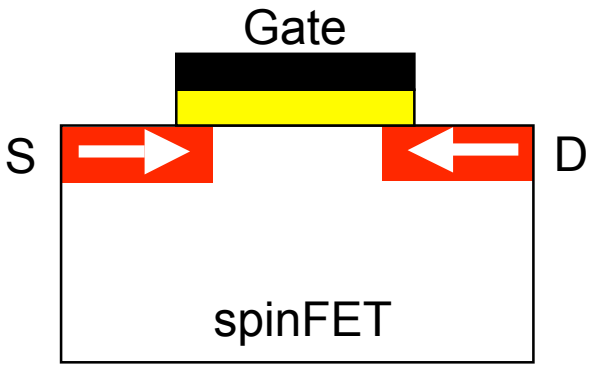
$$\tau \approx 3 \times \tau_{\min}$$

$$n = 3.5 \text{ B/cm}^2$$

4. The Future: spintronics, quantum computing, bio-inspired



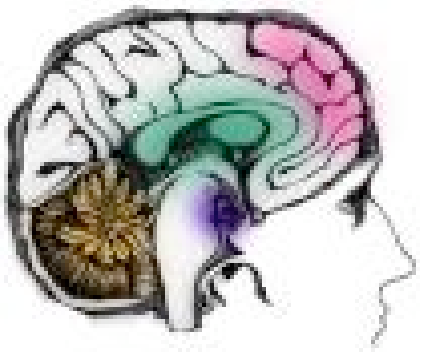
spin



qubit

$$|\uparrow\rangle + |\downarrow\rangle$$

quantum computing



4. The future of CMOS

1) CMOS devices face serious challenges

leakage, variations, interconnects, …

2) Power dissipation limits device density

not our ability to make devices small

3) CMOS will operate near ultimate limits

no transistor can be fundamentally better

4) CMOS will provide more devices than can be used

increasingly, design will drive progress

4. Beyond CMOS

5) New tools, assembly techniques, and understanding *will help push CMOS to its limits*

6) Beyond CMOS devices will add functionality to CMOS
non-volitile memory, opto-electronics, sensing….

7) Beyond CMOS technology will address new markets
macroelectronics, bio-medical devices, …

8) Biology may provide inspiration for new technologies
bottom-up assembly, human intelligence

4. Moore's Law Forever?

Moore's Law is really about reducing cost per function.

Device scaling will slow down, but cost per function can continue to decrease indefinitely.