Moore’s Law Forever?

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1) Background
2) Transistors
3) CMOS
4) Beyond CMOS

www.nanohub.org
1. The scale of things

<table>
<thead>
<tr>
<th>1 meter</th>
<th>1 millimeter</th>
<th>1 micrometer</th>
<th>1 nanometer</th>
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<tbody>
<tr>
<td>(1 billion nm)</td>
<td>(1 million nm)</td>
<td>(1 thousand nm)</td>
<td></td>
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</tbody>
</table>

- people
- things
- ants
- dust
- cells
- molecules (e.g. DNA)
1. Vacuum tube electronics

Vacuum Tube

Edison effect (Edison, 1883)
cathode rays (Thompson, 1897)
diode (Fleming, ~1900)
triode (De Forest, 1906)

ENIAC
(1945, Mauchly and Echkert, U Penn)

18,000 vacuum tubes
1000 sq. feet of floor space
30 tons
150 KW
~50 vacuum tubes / day

http://en.wikipedia.org
1. Transistors

Field-Effect Transistor
Lillienfield, 1925
Heil, 1935

“The transistor was probably the most important invention of the 20th century,”

Ira Flatow, Transistorized!
www.pbs.org/transistor
1. Transistors

transistors

Sony TR-63
6-transistor
shirt pocket radio
1957

http://www.etedeschi.ndirect.co.uk/early.sony.htm
1. Integrated circuits

integrated circuit

Kilby and Noyce (1958, 1959)

Intel 4004

Hoff and Faggin (1971)

~2200 transistors
1. Moore’s Law

In 1965, Gordon Moore sketched out his prediction of the pace of silicon technology. Decades later, Moore’s Law remains true, driven largely by Intel’s unparalleled silicon expertise. Copyright ©2005 Intel Corporation.
1. Microelectronics

- Silicon wafer (300 mm)
- Silicon "chip" (~ 2 cm x 2 cm)

Intel

TI cell phone chip
1. The ITRS

By 2003, the number of transistors manufactured per year ($10^{18}$), was 100 times greater than the estimated number of ants in the world.
1. Nanoelectronics

*Working at the length scale of 1-100 nm in order to create materials, devices, and systems with fundamentally new properties and functions because of their nanoscale size.*

paraphrased from [www.nano.gov](http://www.nano.gov)
1. Exponential Growth

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<tbody>
<tr>
<td>1</td>
<td>90 nm</td>
<td>1B/chip</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>2B</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>4B</td>
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<td>4</td>
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<td>128B</td>
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<tr>
<td>10</td>
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<td>256B</td>
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<tr>
<td>11</td>
<td></td>
<td>512B</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td><strong>1T</strong></td>
</tr>
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</table>
2. MOSFETs

\[ V_G > V_T: \quad I_D \rightarrow \infty \quad \text{“on-current”} \]

\[ V_G < V_T: \quad I_D = 0 \quad \text{“off-current”} \]
Each technology generation: \( \text{(device scaling)} \)

\[
L \rightarrow L/\sqrt{2} \quad A \rightarrow A/2
\]

Number of transistors per chip doubles \( \text{(Moore’s Law)} \)
2. Transistor Physics

energy = -q x voltage
2. Real MOSFETs

*electron energy vs. position*

- **on-current**: $V_{GS} = V_{DS} = V_{DD}$
  - $S > 60$ mV/decade
- **off-current**: $V_{GS} = 0, V_{DS} = V_{DD}$
  - $S > 60$ mV/decade

- $V_{DS} = 0.6$

- **on-current**: $\approx 1000 \mu A/\mu m$

- **Technology generation**: $\rightarrow$

- **Log$_{10} I_{DS}$**

- **Technology generation**: $\rightarrow$

- **Log$_{10} I_{DS}$**
2. Device challenges

1) low voltage operation \((\text{power} = \text{voltage} \times \text{current})\)
2) high on-current \((\text{speed})\)
3) low off-current \((\text{standby power})\)
4) series resistance
5) device variability
2. Transistors

for a tutorial on transistors, see:

“Transistors 101”
under “Nanotechnology 101”
at www.nanohub.org
1) Background
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3. CMOS inverter

- high voltage ($V_{DD}$)
- zero voltage (ground)

noise margin!
3. Two input NAND gate

<table>
<thead>
<tr>
<th>AND</th>
<th>A</th>
<th>B</th>
<th>C</th>
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<tbody>
<tr>
<td></td>
<td>0</td>
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NAND gate schematic with truth tables for AND and NAND.
2. Wires

Rent’s Rule

\( \tau_{\text{global}} \approx r_{\text{int}} c_{\text{int}} \sim \ell^2 \approx 100 \text{ ps} \)

(90 nm technology node)
2. Power

1) standby power:

\[ P_{\text{off}} = N_G I_{D\text{(off)}} V_{\text{DD}} \]

2) dynamic power:

\[ P_{\text{on}} \approx f C_{\text{TOT}} V_{\text{DD}}^2 \]
2. The power crises

![Power density will increase graph]
2. Design challenges

1) power
2) interconnects
3) device variability
4) reliability
5) complexity
3. CMOS Technology

for a tutorial on CMOS, see:

“CMOS Nanotechnology 101”
under “Nanotechnology 101”
at www.nanohub.org
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4. Molecular electronics?

C$_{60}$ on Si(100) 2x1

(Liang and Ghosh)

Hersam, Datta, Purdue
4. Molecular transistors?

S. Datta, A. Ghosh, P. Damle, T. Rakshit

Molecular Relay

Ghosh, Rakshit, Datta, *Nanoletters* 4, 565, 2004
4. Carbon nanotube transistors?


Hongjie Dai group, Stanford
4. Nanowire transistors?

Samuelson Group
Lund
4. Limits of transistors

\[ E_S|_{\text{min}} = \ln(2) k_B T \]

\[ L_{\text{min}} \approx \frac{\hbar}{\sqrt{2m E_S|_{\text{min}}}} \]

\[ \tau_{\text{min}} \approx \frac{\hbar}{E_S|_{\text{min}}} \]

\[ (\Delta p \Delta x = \hbar) \]

\[ (\Delta E \Delta t = \hbar) \]

4. Transistors and limits

**90 nm node**  
(ITRS 2004 ed.)

\[ E_S \approx 35,000 \times E_S \bigg|_{\text{min}} \]

\[ L \approx 25 \times L_{\text{min}} \]

\[ \tau \approx 24 \times \tau_{\text{min}} \]

\[ n = 0.2 \ \text{B/cm}^2 \]

**18 nm node**  
(ITRS 2004 ed.)

\[ E_S \approx 4200 \times E_S \bigg|_{\text{min}} \]

\[ L \approx 5 \times L_{\text{min}} \]

\[ \tau \approx 3 \times \tau_{\text{min}} \]

\[ n = 3.5 \ \text{B/cm}^2 \]
4. The Future: **spintronics, quantum computing, bio-inspired**
4. The future of CMOS

1) CMOS devices face serious challenges
   *leakage, variations, interconnects, …*

2) Power dissipation limits device density
   *not our ability to make devices small*

3) CMOS will operate near ultimate limits
   *no transistor can be fundamentally better*

4) CMOS will provide more devices than can be used
   *increasingly, design will drive progress*
4. Beyond CMOS

5) New tools, assembly techniques, and understanding will help push CMOS to its limits

6) Beyond CMOS devices will add functionality to CMOS non-volatile memory, opto-electronics, sensing, …

7) Beyond CMOS technology will address new markets macroelectronics, bio-medical devices, …

8) Biology may provide inspiration for new technologies bottom-up assembly, human intelligence
4. Moore’s Law Forever?

Moore’s Law is really about reducing cost per function.

Device scaling will slow down, but cost per function can continue to decrease indefinitely.