MOSET Lab – Worked out problems 1

(http://nanohub.org/tools/mosfet)

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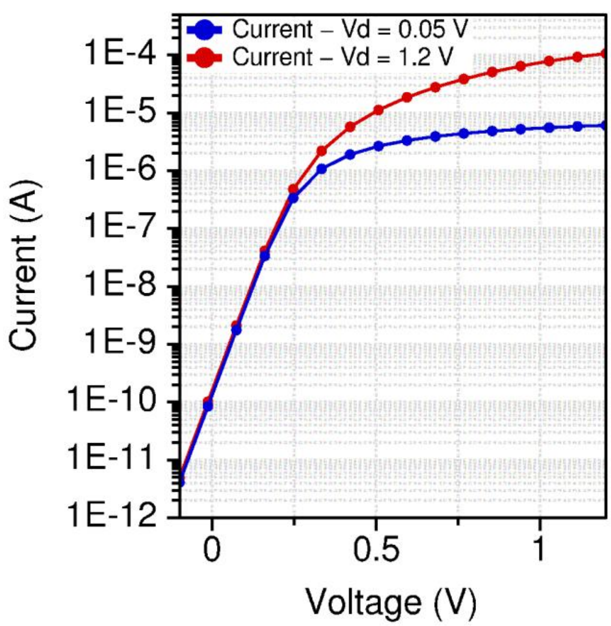
Q1) Reducing channel lengths (Lc) in MOSFET cause what is known short channel effect (SCE). We will see some of the consequences of SCE in a NMOS device. Consider a single gate (n+ poly) bulk type MOSFET with following parameters.

- Source/Drain length = 50 nm
- Oxide thickness = 2 nm
- Junction depth = 20 nm
- Source/Drain doping = 2e20 /cm^3
- Channel doping = 1e18 /cm^3

The operating voltage for the device is 1.2V (V_d=1.2V)

a) Plot Id-Vg for Lc=1000 nm and compute DIBL, threshold voltage (V_t), Subthreshold slope (SS) and I_{on}/I_{off} ratio.
b) Plot threshold voltage , V_t Vs Lc
c) Plot I_{on}/I_{off} Vs Lc
d) Plot SS Vs Lc. How small can the Lc be scaled such that SS ≤ 100 mV/dec?

A1)(a) Id-Vg plot for Lc=1000nm.



DIBL= 0.005/(1.2-0.05)= **4.3 mV/V**

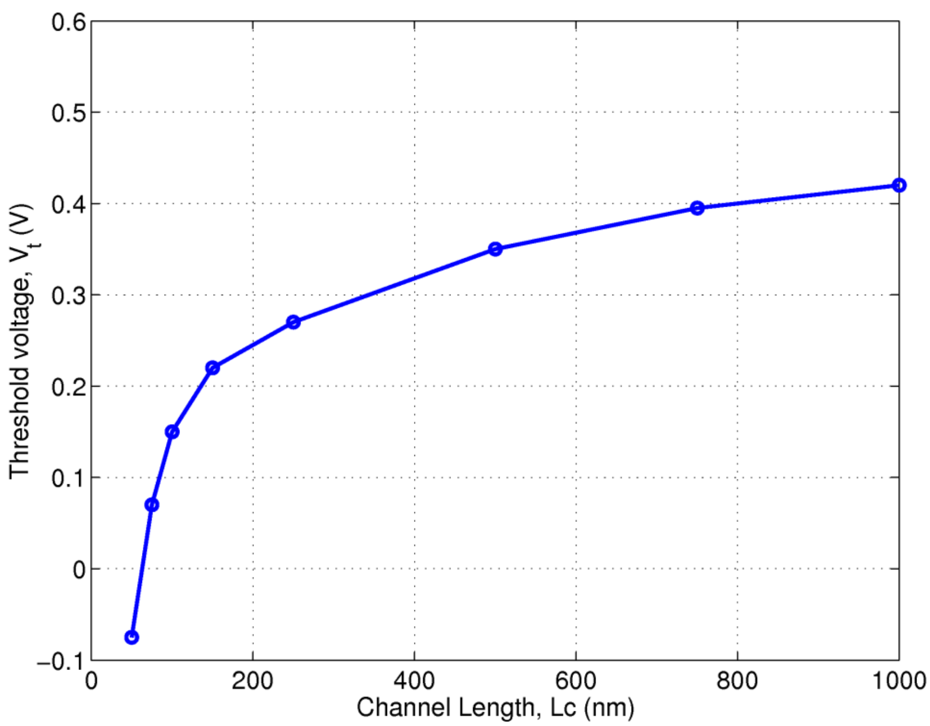
Threshold Voltage, $\mathbf{V_t}$ **=~ 0.33 V**

Subthreshold slope, SS= (.16-.07333)/log(4.147e-8/2.119e-9) **~ 67 mV/dec**

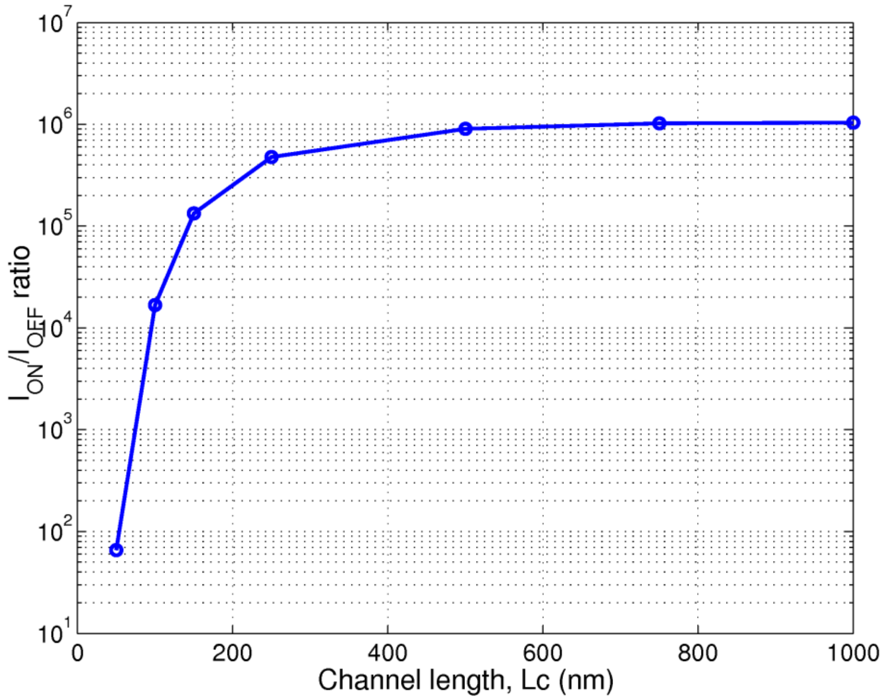
$I_{on}/I_{off} = I_{ds}(\text{at } V_g=V_d=1.2)/\ I_{ds}(\text{at } V_g=0, V_d=1.2)$=1.06e-4/1.62e-10=$\mathbf{6.5x10^5}$

(b) Defining $V_t=V_g$ (at I_d=5e-6 A)

One of the consequences of SCE is threshold voltage roll-off. For the device we are considering it exhibits severe V_t roll-off beyond Lc=200 nm.



(c) Shown below is the I_{on}/I_{off} Vs Lc plot. It can be seen that beyond 200 nm the ratio drops exponentially.



(d) The plot below show SS Vs Lc. It can be seen that SS degrades (increases) with reducing channel length especially below 200 nm.

Channel length can be scaled till **Lc=70 nm** till for SS<100 mV/dec.